DS28EA00

1-Wire Digital Thermometer with Sequence Detect and PIO

www.maxim-ic.com

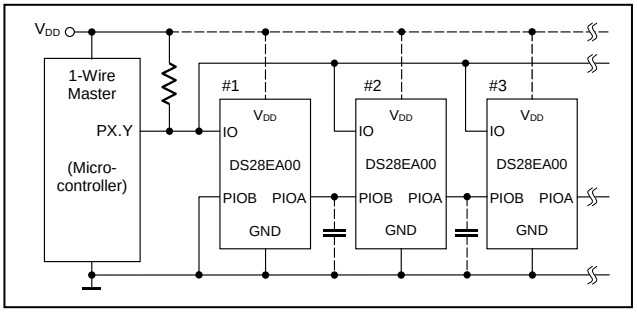
GENERAL DESCRIPTION

The DS28EA00 is a digital thermometer with 9-bit (0.5 °C) to 12-bit (1/16 °C) resolution and alarm function with nonvolatile (NV), user-programmable upper and lower trigger points. Each DS28EA00 has its unique 64-bit registration number that is factory-programmed into the chip. Data is transferred serially through the 1-Wire® protocol, which requires only one data line and a ground for communication. The improved 1-Wire front end with hysteresis and glitch filter enables the DS28EA00 to perform reliably in large 1-Wire networks. Unlike other 1-Wire thermometers, the DS28EA00 has two additional pins to implement a sequence detect function. This feature allows the user to discover the registration numbers according to the physical device location in a chain, e.g., to measure the temperature in a storage tower at different height. If the sequence detect function is not needed, these pins can be used as general-purpose input or output. The DS28EA00 can derive the power for its operation directly from the data line ("parasite power"), eliminating the need for an external power supply.

APPLICATIONS

Data Communication Equipment
Process Temperature Monitoring
HVAC Systems

TYPICAL OPERATING CIRCUIT



Schematic shows PIOs wired for sequence detect function.

Commands, Registers, and Modes are capitalized for clarity.

1-Wire is a registered trademark of Dallas Semiconductor.

SPECIAL FEATURES

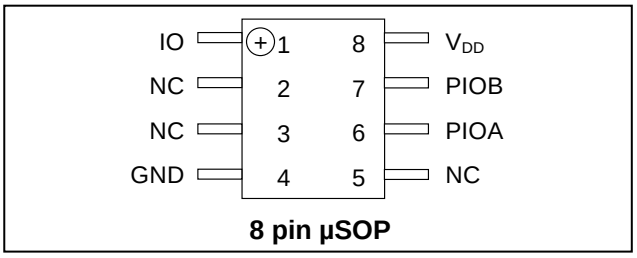
- **Digital Thermometer Measures Temperatures from -40°C to +85°C**
- **Thermometer Resolution is User-Selectable from 9 to 12 Bits**
- **Unique 1-Wire Interface Requires Only One Port Pin for Communication**
- **Each Device has a Unique 64-Bit Factory-Lasered Registration Number**
- **ROM Multidrop Capability Simplifies Distributed Temperature-Sensing Applications**
- **Improved 1-Wire Interface with Hysteresis and Glitch Filter**
- **User-Definable Nonvolatile (NV) Alarm Threshold Settings/User Bytes**
- **Alarm Search Command to Quickly Identify Devices Whose Temperature is Outside of Programmed Limits**
- **Standard and Overdrive 1-Wire Speed**
- **Two General-Purpose Programmable IO (PIO) Pins**
- **Chain Function Sharing the PIO Pins to Detect Physical Sequence of Devices in Network**
- **Operating Range: 3.0V to 5.5V, -40°C to +85°C**
- **Can be Powered from Data Line**
- **8-Pin µSOP Package**

ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
DS28EA00U+	-40 to +85°C	8-pin µSOP
DS28EA00U+T	-40 to +85°C	Tape & Reel

+ Denotes lead-free package.

PIN CONFIGURATION



8 pin µSOP

Package Outline Drawing 21-0036

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

ABSOLUTE MAXIMUM RATINGS

IO Voltage to GND	-0.5V, +6V
IO Sink Current	20mA
Maximum PIOA or PIOB Pin Current	20mA
Maximum Current Through GND Pin	40mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device.

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +85°C; see Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Supply Voltage	V_{DD}	(Note 2)	3.0		5.5	V
Supply Current (Note 5)	I_{DD}	V_{DD} = 5.5V			1.5	mA
Standby Current	I_{DDS}	V_{DD} = 5.5V			1.5	µA
IO Pin General Data						
1-Wire Pullup Voltage (Note 2)	V_{PUP}	Local power	3.0		V_{DD}	V
		Parasite power	3.0		5.5	
1-Wire Pullup Resistance	R_{PUP}	(Notes 2, 3)	0.3		2.2	kΩ
Input Capacitance	C_{IO}	(Notes 4, 5)			1000	pF
Input Load Current	I_L	IO pin at V_{PUP}	0.1		1.5	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 5, 6, 7)	0.46		V_{PUP} - 1.9V	V
Input Low Voltage (Notes 2, 8)	V_{IL}	Parasite powered			0.5	V
		V_{DD} powered (Note 5)			0.7	
Low-to-High Switching Threshold (Notes 5, 6, 9)	V_{TH}	Parasite power	1.0		V_{PUP} - 1.1V	V
Switching Hysteresis (Notes 5, 6, 10)	V_{HY}	Parasite power	0.21		1.7	V
Output Low Voltage (Note 11)	V_{OL}	At 4mA			0.4	V
Recovery Time (Notes 2, 12)	t_{REC}	Standard speed, R_{PUP} = 2.2kΩ	5			µs
		Overdrive speed, R_{PUP} = 2.2kΩ	2			
		Overdrive speed, directly prior to reset pulse; R_{PUP} = 2.2kΩ	5			
Rising-Edge Hold-Off Time (Notes 5, 13)	t_{REH}	Standard speed	0.5		5.0	µs
		Overdrive speed	Not applicable (0)			
Timeslot Duration (Notes 2, 14)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed	8			
IO Pin, 1-Wire Reset, Presence Detect Cycle						
Reset Low Time (Note 2)	t_{RSTL}	Standard speed	480		640	µs
		Overdrive speed	48		80	
Presence-Detect High Time	t_{PDH}	Standard speed	15		60	µs
		Overdrive speed	2		6	
Presence-Detect Fall Time (Notes 5, 15)	t_{FPD}	Standard speed	1.125		8.1	µs
		Overdrive speed	0		1.3	
Presence-Detect Low Time	t_{PDL}	Standard speed	60		240	µs
		Overdrive speed	8		24	
Presence-Detect Sample Time (Notes 2,16)	t_{MSP}	Standard speed	68.1		75	µs
		Overdrive speed	7.3		10	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO Pin, 1-Wire Write						
Write-0 Low Time (Notes 2, 17)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed	6		16	
Write-1 Low Time (Notes 2, 17)	t_{W1L}	Standard speed	5		15	µs
		Overdrive speed	1		2	
IO Pin, 1-Wire Read						
Read Low Time (Notes 2, 18)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	1		2 - δ	
Read Sample Time (Notes 2, 18)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		2	
PIO Pins						
Input Low Voltage	V_{ILP}	(Note 2)			0.3	V
Input High Voltage (Note 2)	V_{IHP}	V_X = max(V_{PUP}, V_{DD})	Vx-1.6			V
Input Load Current (Note 19)	I_{LP}	Pin at GND	-1.1			µA
Output Low Voltage (Note 11)	V_{OLP}	At 4mA			0.4	V
Chain-on Pullup Impedance	R_{CO}	(Note 5)	20	40	60	kΩ
EEPROM						
Programming Current	I_{PROG}	(Notes 5, 20)			1.5	mA
Programming Time	t_{PROG}	(Note 21)			10	ms
Write/Erase Cycles (Endurance) (Notes 22, 23)	N_{CY}	At +25°C	200k			—
		-40°C to +85°C	50k			
Data Retention (Notes 24, 25)	t_{DR}	At +85°C (worst case)	10			years
Temperature Converter						
Conversion Current	I_{CONV}	(Notes 5, 20)			1.5	mA
Conversion Time (Note 26)	t_{CONV}	12-bit resolution (1/16°C)			750	ms
		11-bit resolution (1/8°C)			375	
		10-bit resolution (1/4°C)			187.5	
		9-bit resolution (1/2°C)			93.75	
Conversion Error	$\Delta\vartheta$	-10°C to +85°C	-0.5		+0.5	°C
		below -10°C (Note 5)	-0.5		+2.0	
Converter Drift	ϑ_D	(Note 27)	-0.2		+0.2	°C

Note 1: Specifications at T_A = -40°C are guaranteed by design only and not production-tested.
Note 2: System requirement.
Note 3: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to **parasitically powered systems** with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, local power or an active pullup such as that found in the DS2482-x00, DS2480B, or DS2490 may be required. If longer t_{REC} is used, higher R_{PUP} values may be tolerable.
Note 4: Value is 25pF max. with local power. Maximum value represents the internal parasite capacitance when V_{PUP} is first applied. If R_{PUP} = 2.2kΩ, 2.5µs after V_{PUP} has been applied the parasite capacitance will not affect normal communications.
Note 5: Guaranteed by design, characterization, and/or simulation only. Not production tested.
Note 6: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is itself a function V_{DD}, V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on IO. Lower V_{DD}, V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.
Note 7: Voltage below which, during a falling edge on IO, a logic '0' is detected.
Note 8: The voltage on IO needs to be less than or equal to V_{ILMAX} at all times the master drives the line to a logic '0'.
Note 9: Voltage above which, during a rising edge on IO, a logic '1' is detected.
Note 10: After V_{TH} is crossed during a rising edge on IO, the voltage on IO has to drop by at least V_{HY} to be detected as logic '0'.
Note 11: The I-V characteristic is linear for voltages less than 1V.
Note 12: Applies to a **single parasitically powered DS28EA00** attached to a 1-Wire line. These values also apply to networks of **multiple DS28EA00 with local supply**.
Note 13: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been reached on the preceding rising edge.
Note 14: Defines maximum possible bit rate. Equal to $1/(t_{W0L(min)} + t_{REC(min)})$.
Note 15: Interval during the negative edge on IO at the beginning of a Presence-Detect pulse between the time at which the voltage is 80% of V_{PUP} and the time at which the voltage is 20% of V_{PUP}.
Note 16: Interval after t_{RSTL} during which a bus master is guaranteed to sample a logic '0' on IO if there is a DS28EA00 present. Minimum limit is $t_{PDH(max)} + t_{FPD(max)}$; maximum limit is $t_{PDH(min)} + t_{PDL(min)}$.
Note 17: ε in Figure 14 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1Lmax} + t_F - \varepsilon$ and $t_{W0Lmax} + t_F - \varepsilon$ respectively.

Note 18: δ in Figure 14 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLmax} + t_F$

Note 19: This load current is caused by the internal weak pullup, which asserts a logic '1' to the PIOB and PIOA pins. The logical state of PIOB must not change during the execution of the Conditional Read ROM command.

Note 20: Current drawn from IO during EEPROM programming or temperature conversion interval in parasite powered mode. The pullup circuit on IO during the programming or temperature conversion interval should be such that the voltage at IO is greater than or equal to $V_{PUP(min)}$. If V_{PUP} in the system is close to $V_{PUP(min)}$ then a low impedance bypass of R_{PUP}, which can be activated during programming or temperature conversions may need to be added. The bypass must be activated within 10µs from the beginning of the t_{PROG} or t_{CONV} interval, respectively.

Note 21: The t_{PROG} interval begins t_{REHmax} after the trailing rising edge on IO for the last time slot of the command byte for a valid **Copy Scratchpad** sequence. Interval ends once the device's self-timed EEPROM programming cycle is complete and the current drawn by the device has returned from I_{PROG} to I_L (parasite power) or I_{DDS} (local power).

Note 22: Write-cycle endurance is degraded as T_A increases.

Note 23: Not 100% production-tested; guaranteed by reliability monitor sampling.

Note 24: Data retention is degraded as T_A increases.

Note 25: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to data sheet limit at operating temperature range is established by reliability testing.

Note 26: The t_{CONV} interval begins t_{REHmax} after the trailing rising edge on IO for the last time slot of the command byte for a valid **Convert Temperature** sequence. Interval ends once the device's self-timed temperature conversion cycle is complete and the current drawn by the device has returned from I_{CONV} to I_L (parasite power) or I_{DDS} (local power).

Note 27: Drift data is preliminary and based on a 1000-hour stress test performed on another device with comparable design and fabricated in the same manufacturing process. This test was performed at greater than +85°C with V_{DD} = 5.5V. Confirmed thermal drift results for this device are pending the completion of a new 1000-hour stress test.

PIN DESCRIPTION

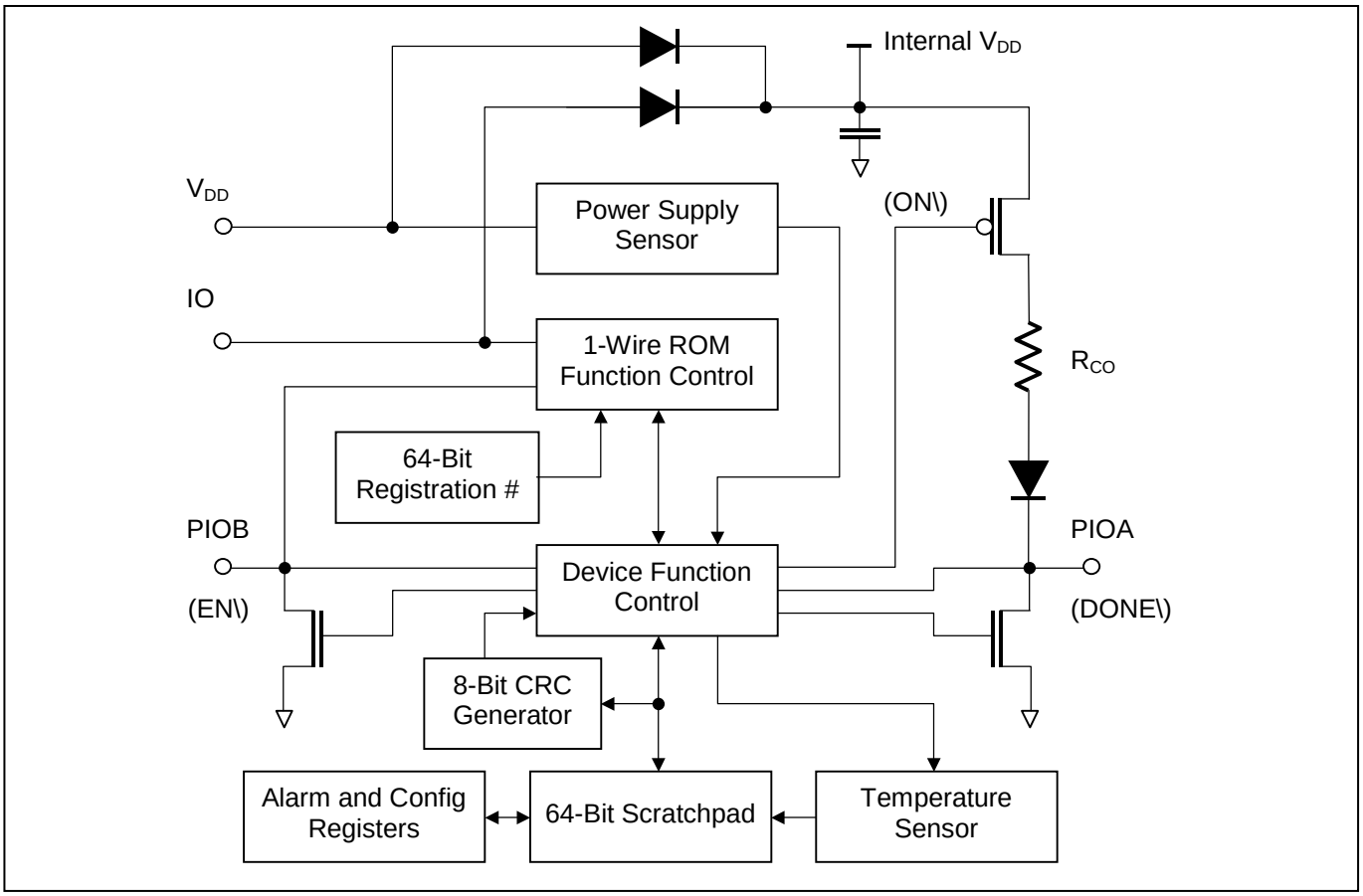
PIN	NAME	FUNCTION
1	IO	1-Wire Bus Interface and Parasitic Power Supply. Open-drain, requires external pullup resistor.
4	GND	Ground Supply
2, 3, 5	N.C.	No Connection
6	PIOA (DONE\)	Open-Drain PIOA Channel and Chain **Output**. For sequence detection, PIOA must be connected to PIOB of the next device in the chain; leave open or tie to GND for the last device in the chain.
7	PIOB (EN\)	Open-Drain PIOB Channel and Chain **Input**. For sequence detection, PIOB of the first device in the chain must be tied to GND.
8	V_{DD}	Power Supply Pin. Must be tied to GND for operation in parasite power mode.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major function blocks of the DS28EA00. The device has three main data components: 1) 64-bit Registration Number, 2) 64-bit scratchpad, and 3) alarm and configuration registers. The 1-Wire ROM Function control unit processes the ROM function commands that allow the device to function in a networked environment. The device function control unit implements the device-specific control functions, such as read/write, temperature conversion, setting the chain state for sequence detection, and PIO access. The CRC generator assists the master verifying data integrity when reading temperatures and memory data. In the sequence detect process, PIOB functions as an input, while PIOA provides the connection to the next device. The power supply sensor allows the master to remotely read whether the DS28EA00 has local power available.

Figure 2 shows the hierarchical structure of the 1-Wire protocol. The bus master must first provide one of the eight ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Conditional (“Alarm”) Search ROM, 5) Conditional Read ROM, 6) Skip ROM, 7) Overdrive-Skip ROM or 8) Overdrive-Match ROM. Upon completion of an Overdrive ROM command byte executed at standard speed, the device enters Overdrive mode, where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 12. After a ROM function command is successfully executed, the device-specific control functions become accessible and the master may provide any one of the nine available commands. The protocol for these control function commands is described in Figure 10. **All data is read and written least significant bit first.**

Figure 1. DS28EA00 Block Diagram



64-BIT REGISTRATION NUMBER

Each DS28EA00 contains a unique Registration Number that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. See Figure 3 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check (CRC) is available *in Application Note 27*.

The shift register bits are initialized to 0. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the 48-bit serial number is entered. After the last byte of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC returns the shift register to all 0s.

Figure 2. Hierachical Structure for 1-Wire Protocol

DS28EA00

Command Level:	Available Commands:	Data Field Affected:
1-Wire ROM Function Commands (see Figure 12)	Read ROM	64-bit Reg. #
	Match ROM	64-bit Reg. #
	Search ROM	64-bit Reg. #
	Conditional Search ROM	64-bit Reg. #, Temperature Alarm Registers, Scratchpad
	Conditional Read ROM	64-bit Reg. #, PIOB pin state, Chain state
	Skip ROM	(none)
	Overdrive Skip	64-bit Reg. #, OD-Flag
	Overdrive Match	64-bit Reg. #, OD-Flag
Device-Specific Control Function Commands (see Figure 10)	Write Scratchpad	Scratchpad
	Read Scratchpad	Scratchpad
	Copy Scratchpad	Temperature Alarm and Configuration Registers
	Convert Temperature	Scratchpad, Temperature Alarm Registers
	Read Power Mode	V_{DD} pin voltage
	Recall EEPROM	Scratchpad, Temperature Alarm and Configuration Registers
	PIO Access Read	PIO pins
	PIO Access Write	PIO pins
	Chain	Chain state, PIOA pin state

Figure 3. 64-Bit Registration Number

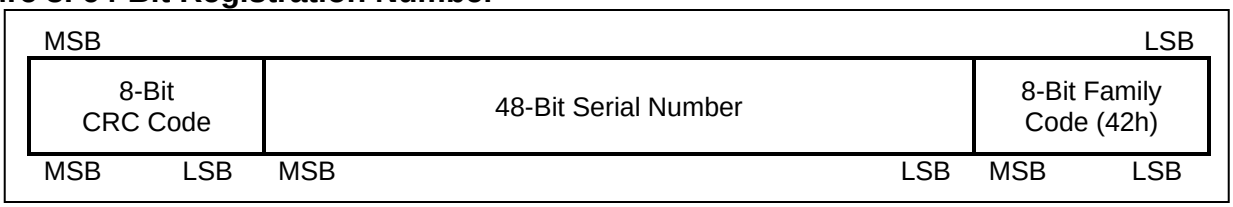
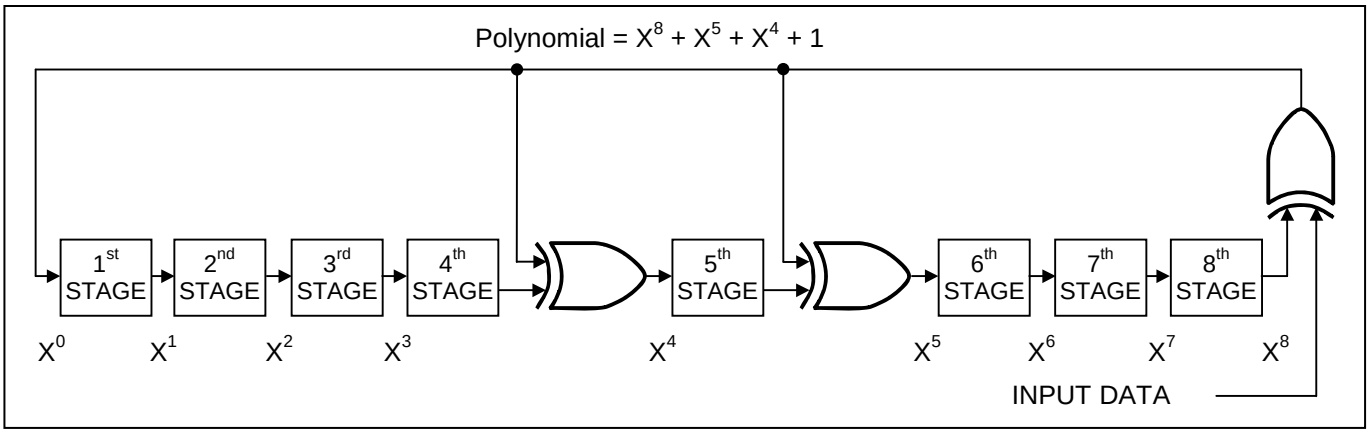


Figure 4. 1-Wire CRC Generator



Memory Description

The memory of the DS28EA00 is shown in Figure 5. It consists of an 8-byte scratchpad and 3 bytes of backup EEPROM. The first two bytes form the temperature readout register, which is updated after a temperature conversion and is read-only. The next 3 bytes are user-writeable; they contain the Temperature High (TH) and the Temperature Low (TL) alarm register and a configuration register. The remaining 3 bytes are "reserved". They power up with constant data and cannot be written by the user. The TH, TL, and configuration register data **in the scratchpad** control the resolution of a temperature conversion and decide whether a temperature is considered as "alarming". TH, TL, and configuration can be copied to the EEPROM to become nonvolatile (NV). The scratchpad is automatically loaded with EEPROM data when the DS28EA00 powers up.

Figure 5. Memory Map

BYTE ADDRESS	SCRATCHPAD *(POWER-UP STATE)*		BACKUP EEPROM
0	Temperature LSB *(50h)*		N/A
1	Temperature MSB *(05h)*		N/A
2	TH Register or User Byte 1*	<-------->	TH Register or User Byte 1
3	TL Register or User Byte 2*	<-------->	TL Register or User Byte 2
4	Configuration Register*	<-------->	Configuration Register
5	Reserved *(FFh)*		N/A
6	Reserved *(0Ch)*		N/A
7	Reserved *(10h)*		N/A

*Power-up state depends on value(s) stored in EEPROM.

Register Detailed Description

Temperature Readout Register

ADDR	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
0	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	**LS Byte**
1	S	S	S	S	S	2^6	2^5	2^4	**MS Byte**

The temperature reading is in °C using a 16-bit sign-extended two's complement format. Table 1 shows examples of temperature and the corresponding data for 12-bit resolution. With two's complement, the sign bit is set if the value is negative. If the device is configured for 12-bit resolution, all bits in the LS byte are valid; for a reduced resolution, bit 0 (11 bit mode), bits 0 to 1 (10 bit mode), and bits 0 to 2 (9 bit mode) are undefined.

Table 1. Temperature/Data Relationship

TEMPERATURE	DIGITAL OUTPUT (BINARY)	DIGITAL OUTPUT (HEX)
+85°C*	0000 0101 0101 0000	0550h
+25.0625°C	0000 0001 1001 0001	0191h
+10.125°C	0000 0000 1010 0010	00A2h
+0.5°C	0000 0000 0000 1000	0008h
0°C	0000 0000 0000 0000	0000h
-0.5°C	1111 1111 1111 1000	FFF8h
-10.125°C	1111 1111 0101 1110	FF5Eh
-25.0625°C	1111 1110 0110 1111	FE6Fh
-40°C	1111 1101 1000 0000	FD80h

*The power-on reset value of the temperature readout register is +85°C.

Temperature Alarm Registers

ADDR	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
2	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0	**High Alarm (TH)**
3	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0	**Low Alarm (TL)**

The result of a temperature conversion is automatically compared to the values in the alarm registers to determine whether an alarm condition exists. Alarm thresholds are represented as two's complement number. With 8 bits available for sign and value, alarm thresholds can be set in increments of 1°C. An alarm condition exists if a temperature conversion results in a value that is either **higher than or equal to** the value stored in the TH register or **lower than or equal to** the value stored in the TL register. If a temperature alarm condition exists, the device will respond to the Conditional Search command. The alarm condition is cleared if a subsequent temperature conversion results in a temperature reading **within** the boundaries defined by the data in the TH and TL registers.

Configuration Register

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
4	0	R1	R0	1	1	1	1	1

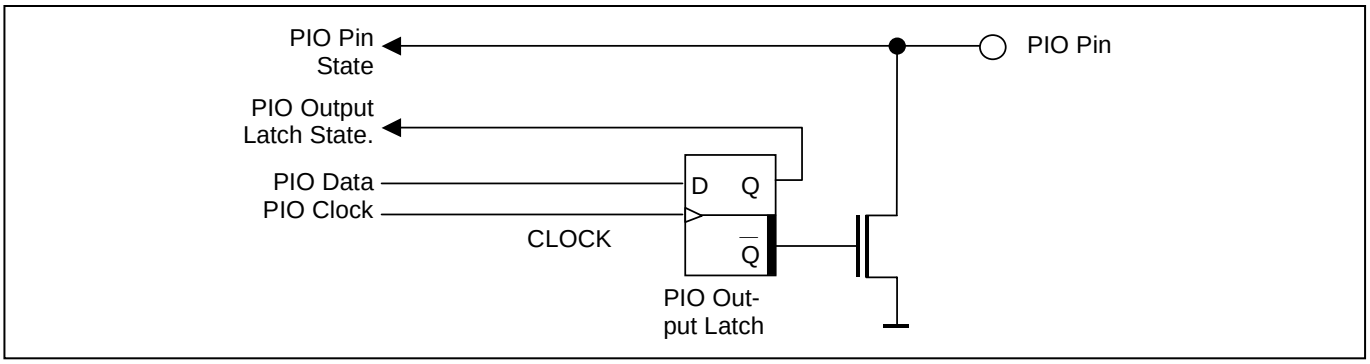
The functional assignments of the individual bits are explained in the table below. Bits 0 to 4 and bit 7 have no function; they cannot be changed by the user. As a factory default, the device operates in 12-bit resolution.

BIT DESCRIPTION	BIT(S)	DEFINITION
R0, R1: Temperature Converter Resolution	b5, b6	These bits control the resolution of the temperature converter. The codes are as follows: R1 R0 0 0 9 bits 0 1 10 bits 1 0 11 bits 1 1 12 bits

PIO Structure

Each PIO consists of an open-drain pulldown transistor and an input path to read the pin state. The transistor is controlled by the PIO Output Latch, as shown in Figure 6. The Device Function Control unit connects the PIOs logically to the 1-Wire interface. PIOA has a pullup path to internal V_{DD} to facilitate the sequence detect function (see Figure 1) in conjunction with the Chain command; PIOB is truely an open-drain structure. The power-on default state of the PIO output transistors is off; high-impedance on-chip resistors (not shown in the graphic) pull the PIO pins to internal V_{DD}.

Figure 6. PIO Simplified Logic Diagram



Chain Function

The chain function is a feature that allows the 1-Wire master to discover the physical sequence of devices that are wired as a linear network (“chain”). This is particularly convenient for devices that are installed at equal spacing along a long cable, e.g., to measure temperatures at different locations inside a storage tower or tank. Without chain function, the master needs a lookup table to correlate registration number to the physical location.

The chain function requires two pins, an input (EN\) to **enable** a device to respond during the discovery and an output (DONE\) to inform the next device in the chain that the discovery of its neighbor is **done**. The two general purpose ports of the DS28EA00 are re-used for the chain function. PIOB functions as EN\ input and PIOA generates the DONE\ signal, which is connected to the EN\ input of the next device, as shown in the typical operating circuit on page 1. The EN\ input of the first device in the chain needs to be hardwired to GND or logic ‘0’ must be applied for the duration of the sequence discovery process. Besides the two pins, the sequence discovery relies on the Conditional Read ROM command.

For the chain function and normal PIO operation to coexist, the DS28EA00 distinguishes three chain states, OFF, ON, and DONE. The transition from one chain state to another is controlled through the Chain command. Table 2 summarizes the chain states and the specific behavior of the PIO pins.

Table 2. Chain States

CHAIN STATE	DEVICE BEHAVIOR		
	PIOB (EN\)	**PIOA (DONE\)**	**Conditional Read ROM**
OFF (default)	PIO (high impedance)	PIO (high impedance)	Not recognized
ON	EN\ input	Pullup on	Recognized if EN\ is ‘0’
DONE	No function	Pulldown on (DO\ logic ‘0’)	Not recognized

The power-on default chain state is **OFF**, where PIOA and PIOB are solely controlled through the PIO Access Read and Write commands. In the chain **ON** state PIOA is pulled high to the device’s internal V_{DD} supply through a ~40kΩ resistor, applying a logic ‘1’ to the PIOB (EN\) pin of the next device. Only in the ON state does a DS28EA00 respond to the Conditional Read ROM command, provided its EN\ is at logic ‘0’. After a device’s ROM

Registration number is read, it is put into the chain **DONE** state, which enables the next device in the chain to respond to the Conditional Read ROM command.

At the beginning of the sequence discovery process all devices are put into the chain ON state. As the discovery progresses, one device after another is transitioned into the DONE state until all devices are identified. Finally, all devices are put into the chain OFF state, which releases the PIOs and restores their power-on default state.

CONTROL FUNCTION COMMANDS

The *Control Function Flow Chart* (Figure 10) describes the protocols necessary for measuring temperatures, accessing the memory and PIOs, and changing the chain state. Examples on how to use these and other functions are included at the end of this document. The communication between master and DS28EA00 takes place either at standard speed (default, OD = 0) or at Overdrive Speed (OD = 1). If not explicitly set into the Overdrive mode after power-up the DS28EA00 communicates at standard speed.

WRITE SCRATCHPAD [4Eh]

This command allows the master to write 3 bytes of data to the scratchpad of the DS28EA00. The first data byte is associated with the TH register (byte address 2), the second byte is associated with the TL register (byte address 3), and the third byte is associated with the configuration register (byte address 4). Data must be transmitted least significant bit first. All three bytes MUST be written before the master issues a reset, or the data may be corrupted.

READ SCRATCHPAD [BEh]

This command allows the master to read the contents of the scratchpad. The data transfer starts with the least significant bit of the temperature readout register at byte address 0 and continues through the remaining 7 bytes of the scratchpad. If the master continues reading, it gets a 9^{th} byte, which is an 8-bit CRC of all the data in the scratchpad. This CRC is generated by the DS28EA00 and uses the same polynomial function as is used with the ROM Registration Number. The CRC is transmitted in its true (non-inverted) form. The master may issue a reset to terminate the reading early if only part of the scratchpad data is needed.

COPY SCRATCHPAD [48h]

This command copies the contents of the scratchpad byte addresses 2 to 4 (TH, TL and configuration registers) to the back-up EEPROM. If the device has no V_{DD} power, the master must enable a strong pullup on the 1-Wire bus for the duration of $t_{PROGMAX}$ within 10µs after this command is issued. If the device is powered through the V_{DD} pin, the master may generate read time slots to monitor the copy process. Copy is completed when the master reads 1-bits instead of 0-bits.

CONVERT TEMPERATURE [44h]

This command initiates a temperature conversion. Following the conversion, the resulting thermal data is found in the temperature readout register in the scratchpad and the DS28EA00 returns to its low-power idle state. If the device has no V_{DD} power, the master must enable a strong pullup on the 1-Wire bus for the duration of the applicable resolution-dependent $t_{CONVMAX}$ within 10µs after this command is issued. If the device is powered through the V_{DD} pin, the master may generate read time slots to monitor the conversion process. The conversion is completed when the master reads 1-bits instead of 0-bits.

READ POWER MODE [B4h]

For Copy Scratchpad and Convert Temperature the master needs to know whether the DS28EA00 has V_{DD} power available. The Read Power Mode command is implemented to provide the master with this information. After the command code, the master issues read time slots. If the master reads 1's, the device is powered through the V_{DD} pin. If the device is powered through the 1-Wire line, the master will read 0's. The power supply sensor samples the state of the V_{DD} pin for every time slot that the master generates after the command code.

RECALL EEPROM [B8h]

This command recalls the TH and TL alarm trigger values and configuration data from backup EEPROM into their respective locations in the scratchpad. After having transmitted the command code, the master may issue read time slots to monitor the completion of the recall process. Recall is completed when the master reads 1-bits instead of 0-bits. The recall occurs automatically at power-up, not requiring any activity by the master.

PIO ACCESS READ [F5h]

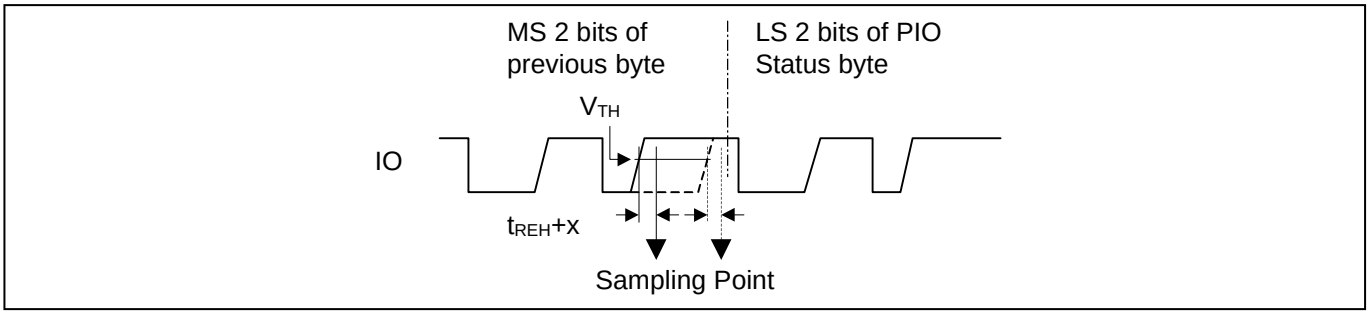
This command reads the PIO logical status and reports it together with the state of the PIO Output Latch in an endless loop. A PIO Access Read can be terminated at any time with a 1-Wire Reset. PIO Access Read can be executed in the Chain ON and Chain DONE state. While the device is in Chain ON or Chain DONE state, the PIO output latch states will always read out as 1s; the PIO pin state may not be reported correctly.

PIO Status Bit Assignment

b7	b6	b5	b4	b3	b2	b1	b0
Complement of b3 to b0				PIOB Output Latch State	PIOB Pin State	PIOA Output Latch State	PIOA Pin State

The state of both PIO channels is sampled at the same time. The first sampling occurs during the last (most significant) bit of the command code F5h. The PIO status is then reported to the bus master. While the master receives the last (most significant) bit of the PIO status byte, the next sampling occurs and so on until the master generates a 1-Wire Reset. The sampling occurs with a delay of t_{REH}+x from the rising edge of the MS bit of the previous byte, as shown in Figure 7. The value of "x" is approximately 0.2µs.

Figure 7. PIO Access Read Timing Diagram



Notes:

1 The "previous byte" could be the command code or the data byte resulting from the previous PIO sample.

2 The sample point timing also applies to the PIO Access Write command, with the "previous byte" being the write confirmation byte (AAh).

PIO ACCESS WRITE [A5h]

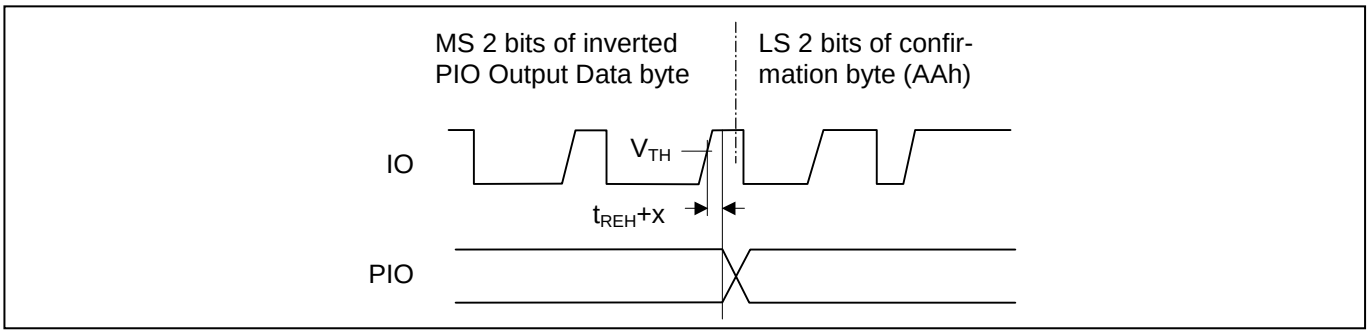
The PIO Access Write command writes to the PIO output latches, which control the pulldown transistors of the PIO channels. In an endless loop this command first writes new data to the PIO and then reads back the PIO status. This implicit read-after-write can be used by the master for status verification. A PIO Access Write can be terminated at any time with a 1-Wire Reset. The PIO Access Write command is ignored by the device while in Chain ON or Chain DONE state.

PIO Output Data Bit Assignment

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	PIOB	PIOA

After the command code the master transmits a PIO Output Data byte that determines the new state of the PIO output transistors. The first (least significant) bit is associated to PIOA; the next bit affects PIOB. The other 6 bits of the new state byte do not have corresponding PIO pins. These bits should always be transmitted as "1"s. To switch the output transistor on, the corresponding bit value is 0. To switch the output transistor off (non-conducting) the bit must be 1. This way the bit transmitted as the new PIO output state arrives in its true form at the PIO pin. To protect the transmission against data errors, the master must repeat the PIO Output Data byte in its inverted form. Only if the transmission was error-free will the PIO status change. The actual PIO transition to the new state occurs with a delay of t_{REH} + x from the rising edge of the MS bit of the inverted PIO byte, as shown in Figure 8. The value of "x" is approximately 0.2µs. To inform the master about the successful communication of the PIO byte, the DS28EA00 transmits a confirmation byte with the data pattern AAh. While the MS bit of the confirmation byte is transmitted, the DS28EA00 samples the state of the PIO pins, as shown in Figure 7, and sends it to the master. The master can either continue writing more data to the PIO or issue a 1-Wire Reset to end the command.

Figure 8. PIO Access Write Timing Diagram



CHAIN COMMAND [99h]

This command allows the master to put the DS28EA00 into one of the three Chain States, as shown in Figure 9. The device powers up in the Chain OFF state. To transition a DS28EA00 from one state to another, the master must send a suitable Chain Control byte after the Chain Command code. Only the codes 3Ch, 5Ah and 96h (true form) are valid, assigned to **OFF, ON,** and **DONE**, in this sequence. This control byte is first transmitted in its true form and then in its inverted form. If the Chain state change was successful, the master receives AAh confirmation bytes. If the change was not successful (control byte transmission error, invalid control byte) the master will read 00h bytes instead.

Figure 9. Chain State Transition Diagram

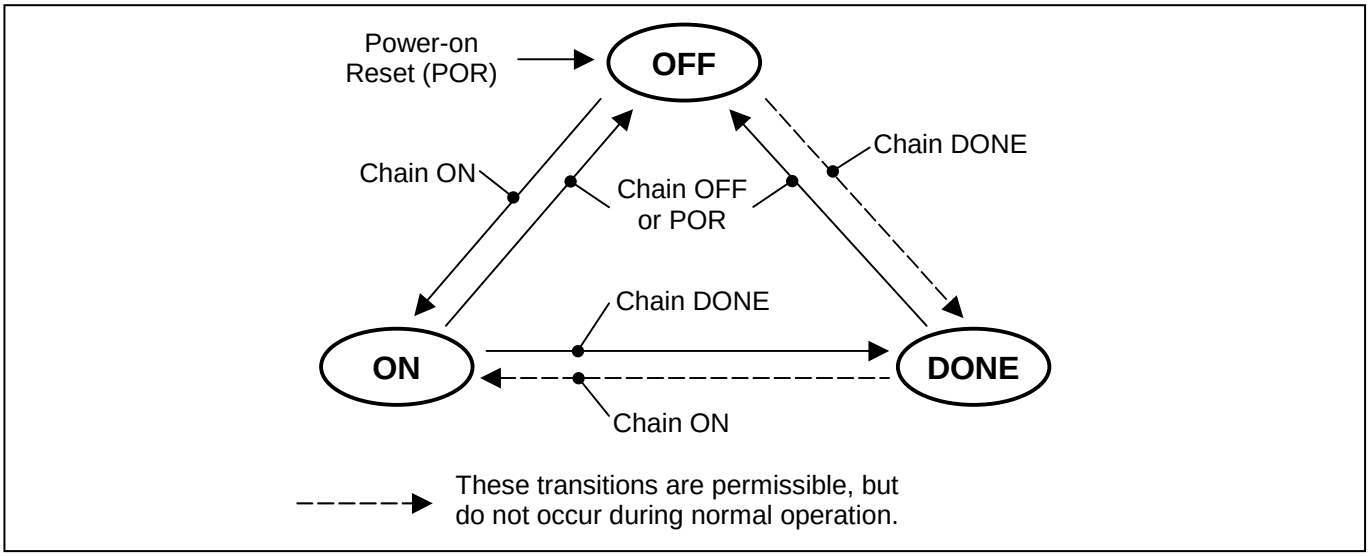


Figure 10-1. Control Function Flow Chart

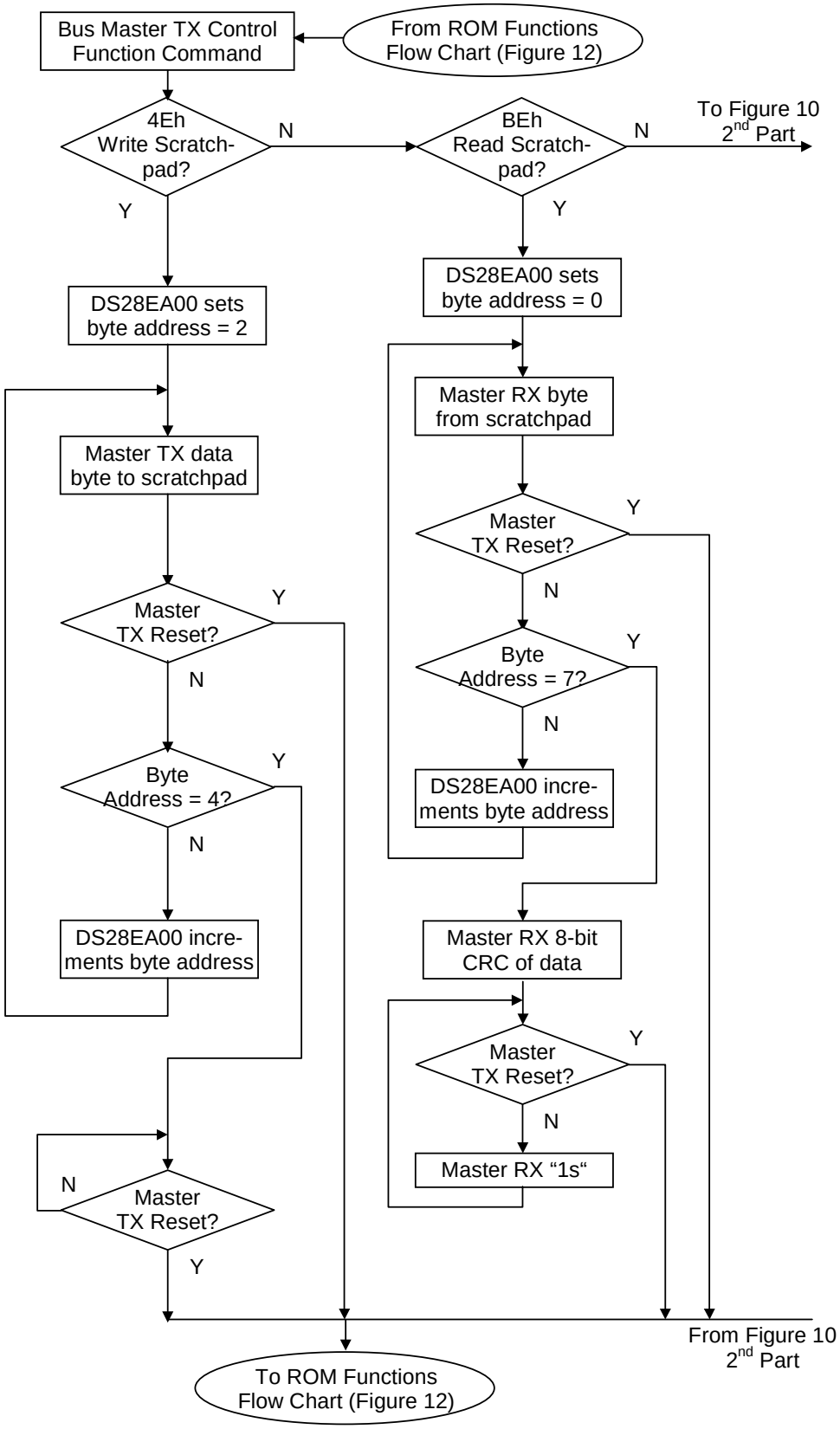


Figure 10-2. Control Function Flow Chart (continued)

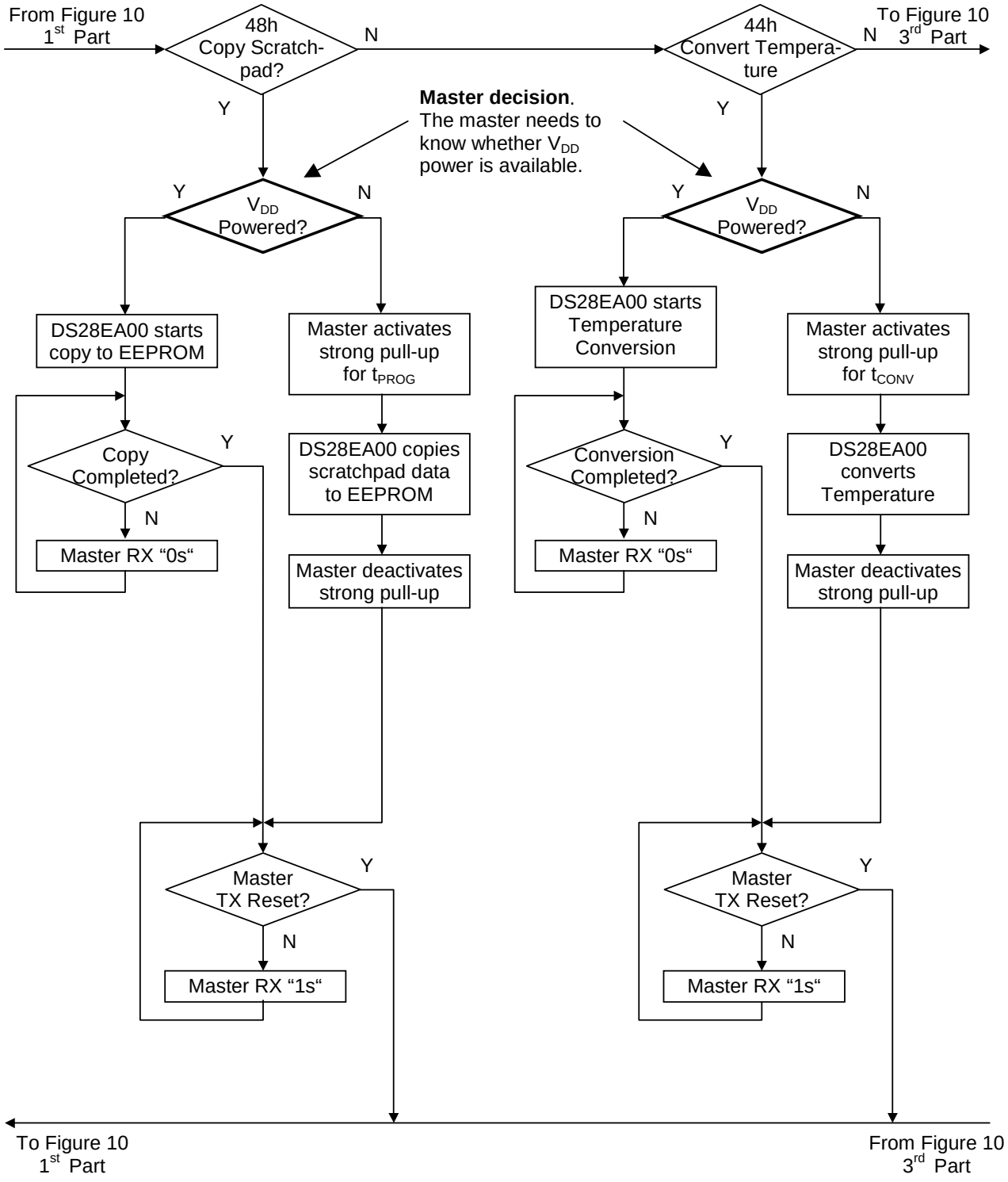


Figure 10-3. Control Function Flow Chart (continued)

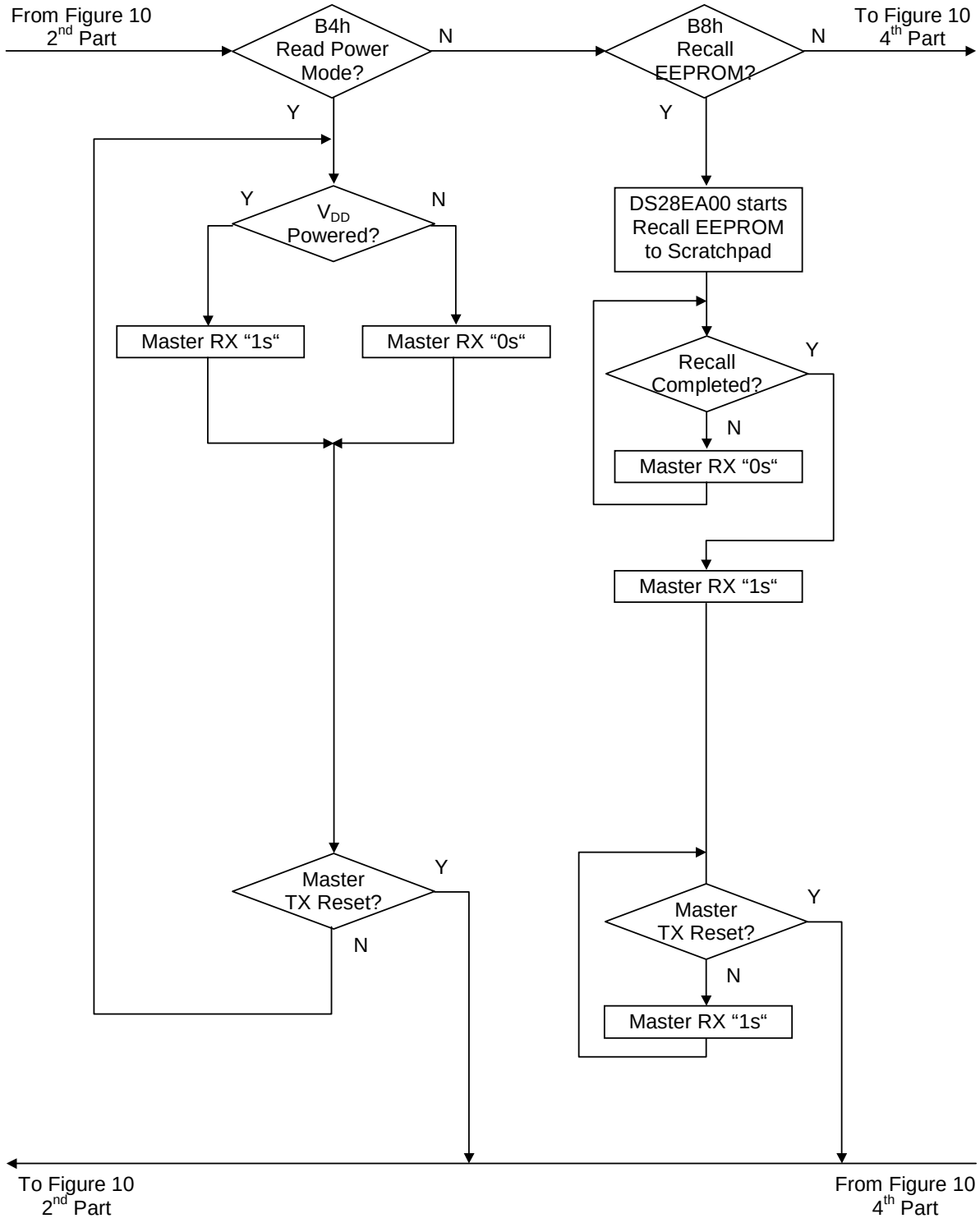


Figure 10-4. Control Function Flow Chart (continued)

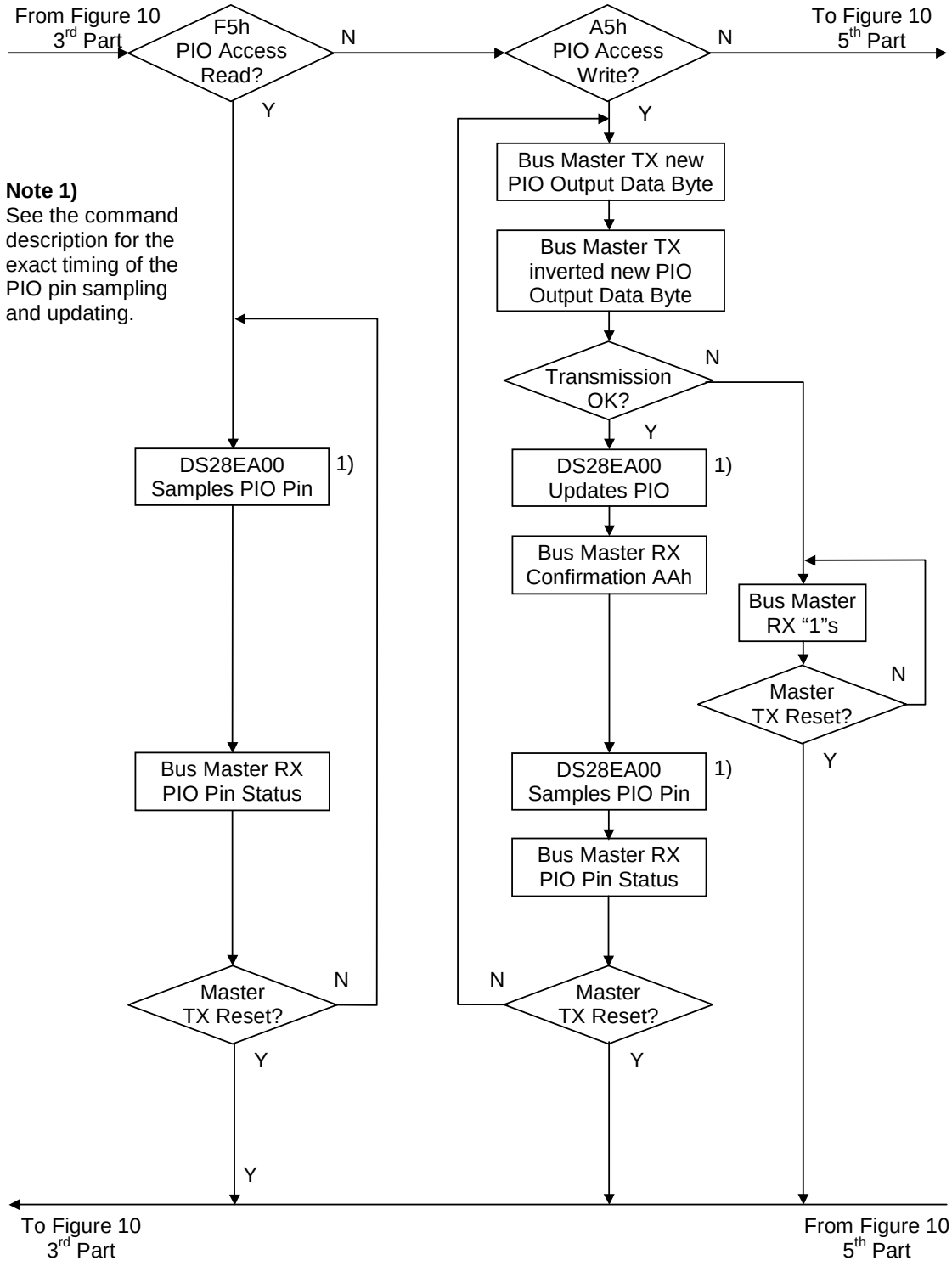
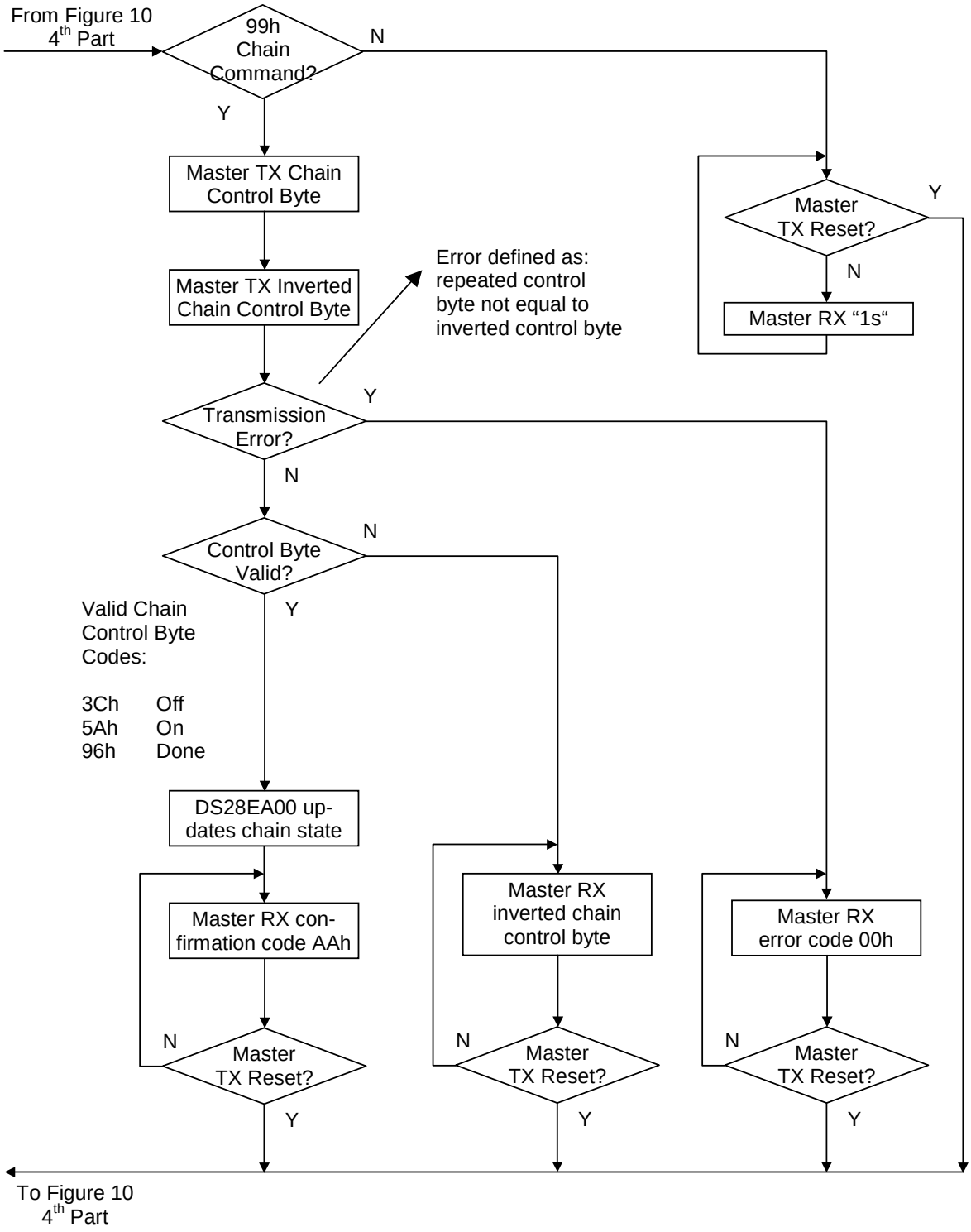


Figure 10-5. Control Function Flow Chart (continued)



1-Wire BUS SYSTEM

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS28EA00 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots, which are initiated on the falling edge of sync pulses from the bus master.

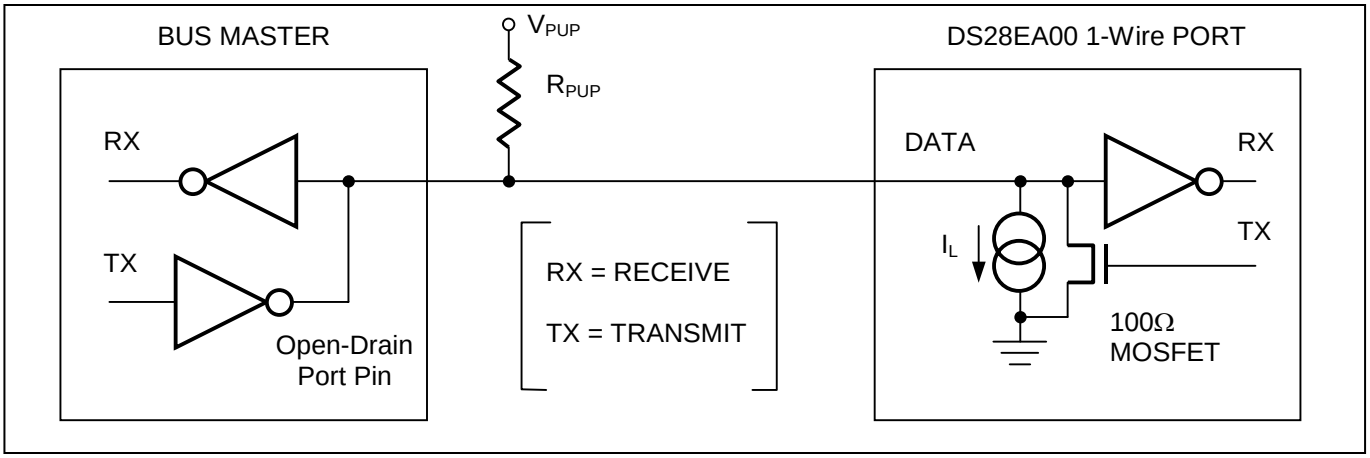
HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or tri-state outputs. The 1-Wire port of the DS28EA00 is open drain with an internal circuit equivalent to that shown in Figure 11.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The DS28EA00 supports both a Standard and Overdrive communication speed of 15.3kbps (max) and 125kbps (max), respectively. Note that legacy 1-Wire products support a standard communication speed of 16.3kbps and Overdrive of 142kbps. The slightly reduced rates for the DS28EA00 are a result of additional recovery times, which in turn were driven by a 1-Wire physical interface enhancement to improve noise immunity. The value of the pullup resistor primarily depends on the network size and load conditions. The DS28EA00 requires a pullup resistor of 2.2kΩ (max) at any speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (Overdrive speed) or more than 120µs (standard speed), one or more devices on the bus may be reset.

Figure 11. Hardware Configuration



TRANSACTION SEQUENCE

The protocol for accessing the DS28EA00 through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Control Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS28EA00 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

1-Wire ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the eight ROM function commands that the DS28EA00 supports. All ROM function commands are 8 bits long. A list of these commands follows (refer to the flow chart in Figure 12).

READ ROM [33h]

This command allows the bus master to read the DS28EA00's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

MATCH ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS28EA00 on a multidrop bus. Only the DS28EA00 that exactly matches the 64-bit ROM sequence responds to the following Control Function command. All other slaves wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

SEARCH ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their registration numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the registration numbers of all slave devices. For each bit of the registration number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its registration number bit. On the second slot, each slave device participating in the search outputs the complemented value of its registration number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the ROM code tree. After one complete pass, the bus master knows the registration number of a single device. Additional passes identify the registration numbers of the remaining devices. Refer to *Application Note 187: 1-Wire Search Algorithm* for a detailed discussion, including an example. The Search ROM command does not reveal any information about the location of a device in a network. If multiple DS28EA00 are wired as a linear network ("chain"), the device location can be detected using Conditional Read ROM in conjunction with the Chain function.

CONDITIONAL SEARCH ROM [ECh]

The Conditional Search ROM command operates similarly to the Search ROM command except that only those devices, which fulfill certain conditions, participates in the search. This function provides an efficient means for the bus master to identify devices on a multidrop system that have to signal an important event. After each pass of the conditional search that successfully determined the 64-bit ROM code for a specific device on the multidrop bus, that particular device can be individually accessed as if a Match ROM had been issued, since all other devices will have dropped out of the search process and will be waiting for a reset pulse. The DS28EA00 will respond to the conditional search if a temperature alarm condition exists. For more details see *Temperature Alarm Registers*.

CONDITIONAL READ ROM [0Fh]

This command is used in conjunction with the Chain function to detect the physical sequence of devices in a linear network ("chain"). A DS28EA00 responds to Conditional Read ROM if two conditions are met: a) the device is in chain ON state, and b) the EN\ input (PIOB) is at logic '0'. This condition is met by exactly one device during the sequence discovery process. Upon receiving the Conditional Read ROM command, this particular device transmits its 64-bit registration numberA device in chain ON state, but with a logic '1' level at EN\ does not respond to Conditional Read ROM. See *Sequence Discovery Procedure* for more details on the use of Conditional Read ROM and the Chain command.

SKIP ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the control functions without providing the 64-bit ROM code. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

OVERDRIVE SKIP ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus master to access the control functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command, the Overdrive Skip ROM sets the DS28EA00 in the Overdrive mode (OD = 1). All communication following this command has to occur at Overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all Overdrive-supporting devices into Overdrive mode. To subsequently address a specific Overdrive-supporting device, a reset pulse at Overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting Overdrive is present on the bus and the Overdrive Skip ROM command is followed by a Read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

OVERDRIVE MATCH ROM [69h]

The Overdrive Match ROM command followed by a 64-bit ROM sequence transmitted at Overdrive Speed allows the bus master to address a specific DS28EA00 on a multidrop bus and to simultaneously set it in Overdrive mode. Only the DS28EA00 that exactly matches the 64-bit ROM sequence responds to the subsequent control function command. Slaves already in Overdrive mode from a previous Overdrive Skip or successful Overdrive Match command remain in Overdrive mode. All overdrive-capable slaves return to standard speed at the next Reset Pulse of minimum 480µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

Figure 12-1. ROM Funtions Flow Chart

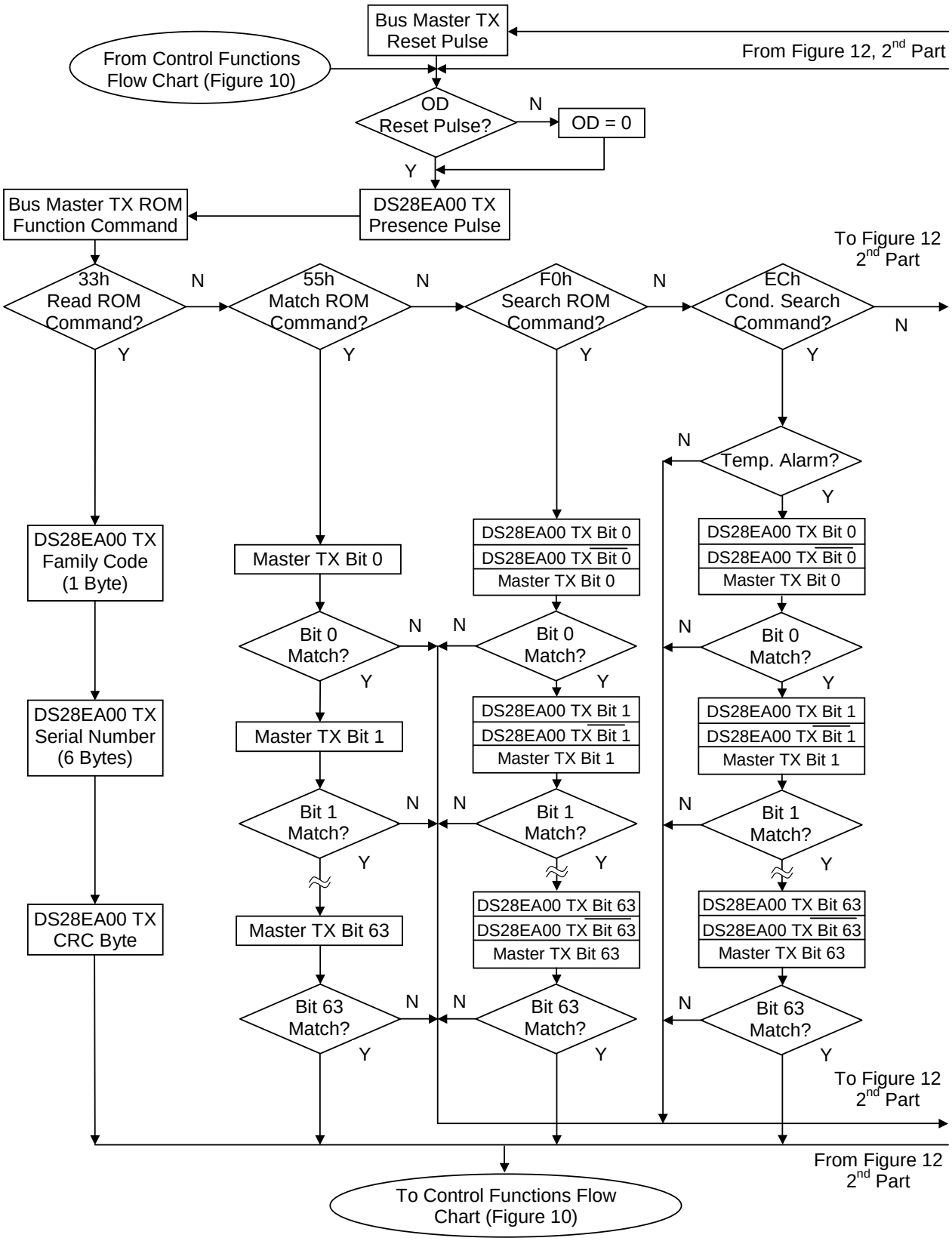
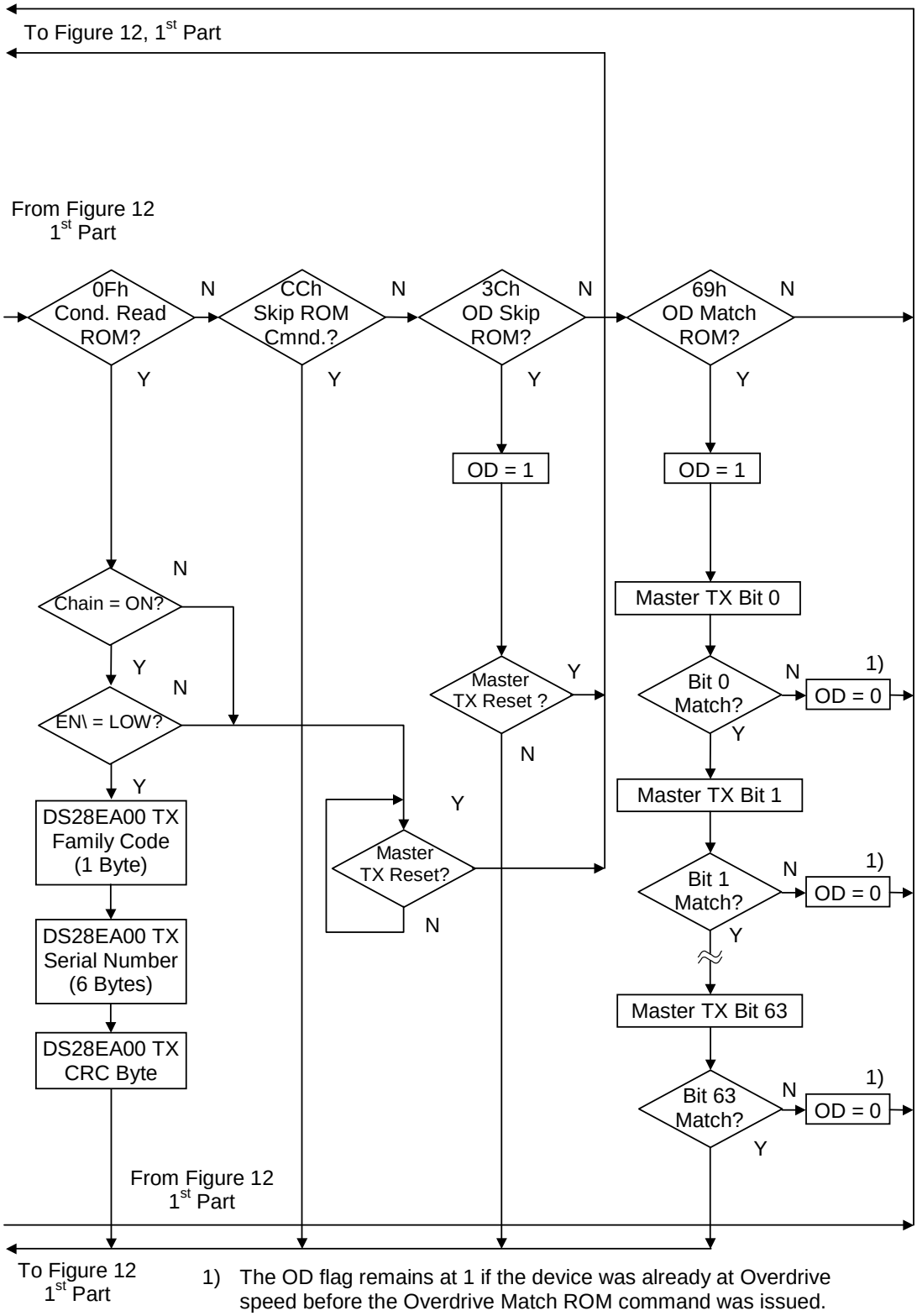


Figure 12-2. ROM Functions Flow Chart



1) The OD flag remains at 1 if the device was already at Overdrive speed before the Overdrive Match ROM command was issued.

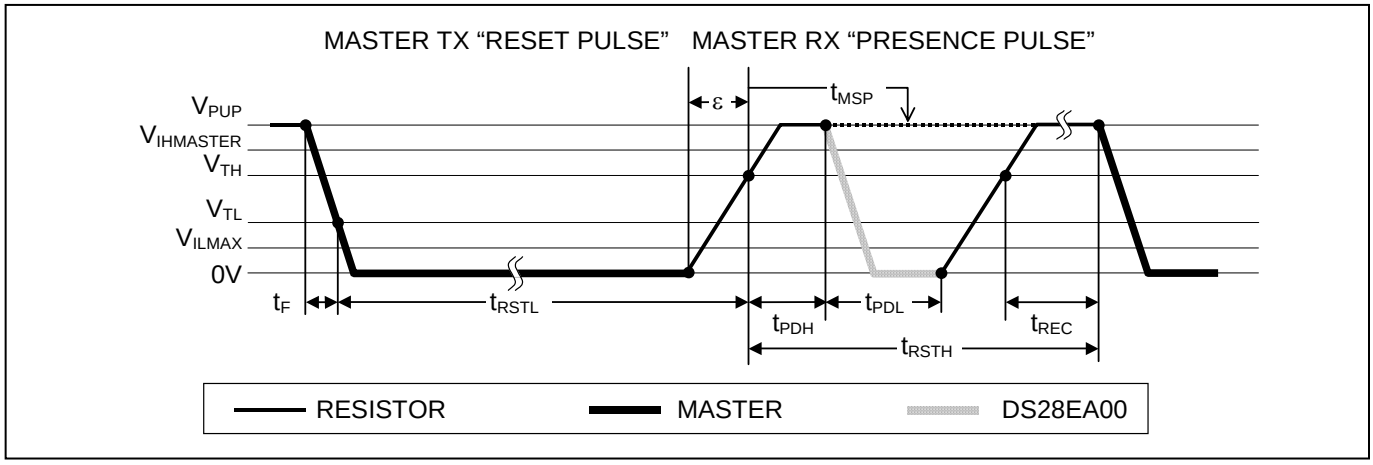
1-Wire SIGNALING

The DS28EA00 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write-Zero, Write-One, and Read-Data. Except for the Presence pulse, the bus master initiates all falling edges. The DS28EA00 can communicate at two different speeds, standard speed, and Overdrive Speed. If not explicitly set into the Overdrive mode, the DS28EA00 communicates at standard speed. While in Overdrive Mode the fast timing applies to all waveforms.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 13 as 'ε' and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS28EA00 when determining a logical level, not triggering any events.

Figure 13 shows the initialization sequence required to begin any communication with the DS28EA00. A Reset Pulse followed by a Presence Pulse indicates the DS28EA00 is ready to receive data, given the correct ROM and Control Function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge. A t_{RSTL} duration of 480µs or longer exits the Overdrive Mode, returning the device to standard speed. If the DS28EA00 is in Overdrive Mode and t_{RSTL} is no longer than 80µs, the device remains in Overdrive Mode. If the device is in Overdrive Mode and t_{RSTL} is *between* 80µs and 480µs, the device will reset, but the communication speed is undetermined.

Figure 13. Initialization Procedure "Reset and Presence Pulses"



After the bus master has released the line it goes into receive mode. Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor, or in case of a DS2482-x00 or DS2480B driver, by active circuitry. When the threshold V_{TH} is crossed, the DS28EA00 waits for t_{PDH} and then transmits a Presence Pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

The t_{RSTH} window must be at least the sum of t_{PDHMAX}, t_{PDLMAX}, and t_{RECMIN}. Immediately after t_{RSTH} is expired, the DS28EA00 is ready for data communication. In a mixed population network, t_{RSTH} should be extended to minimum 480µs at standard speed and 48µs at Overdrive speed to accommodate other 1-Wire devices.

READ/WRITE TIME SLOTS

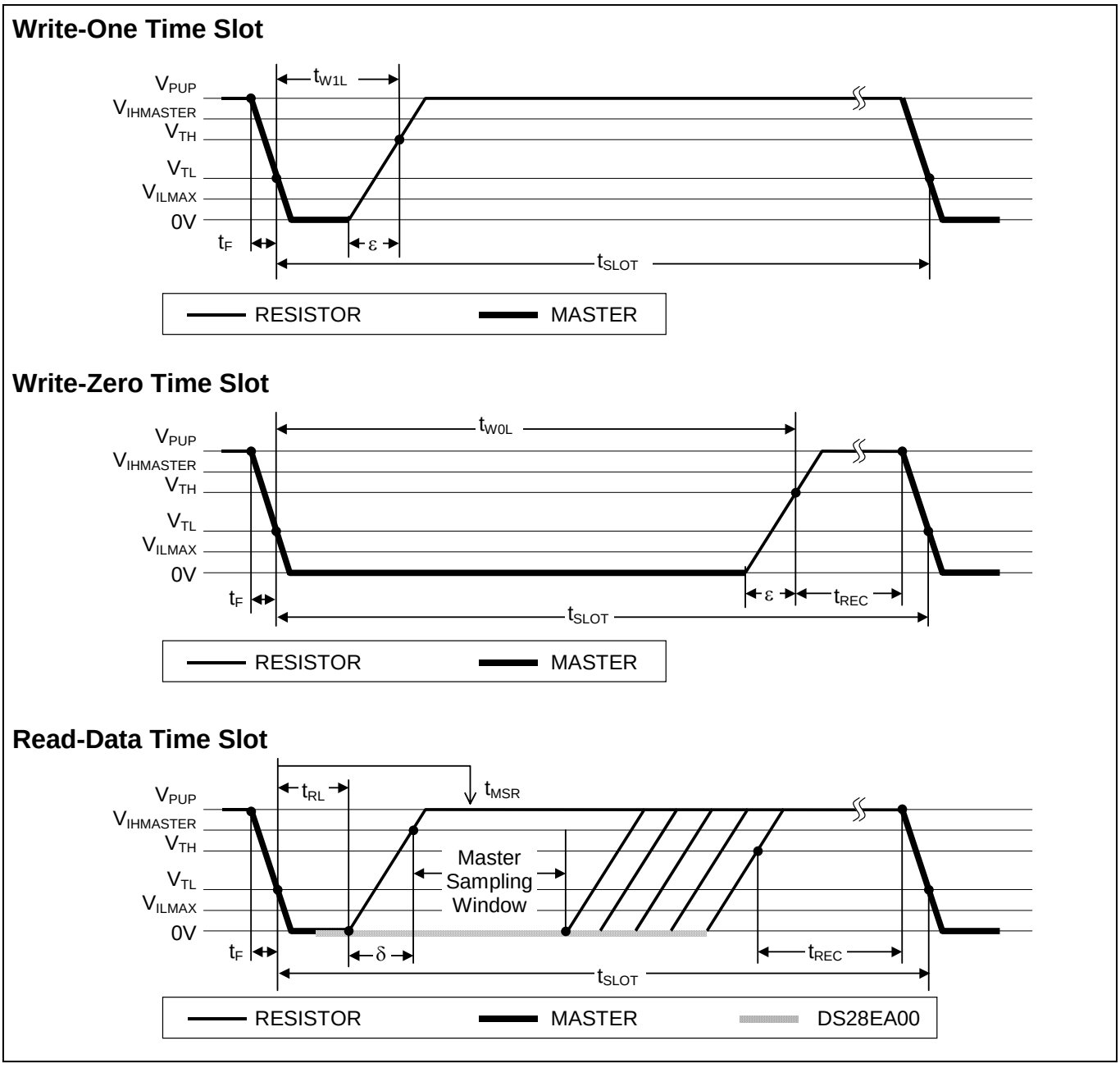
Data communication with the DS28EA00 takes place in time slots, which carry a single bit each. Write-time slots transport data from bus master to slave. Read-time slots transfer data from slave to master. Figure 14 illustrates the definitions of the write- and read-time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS28EA00 starts its internal timing generator that determines when the data line is sampled during a write-time slot and how long data is valid during a read-time slot.

Master-To-Slave

For a **write-one** time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a **write-zero** time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS28EA00 needs a recovery time t_{REC} before it is ready for the next time slot.

Figure 14. Read/Write Timing Diagram



Slave-To-Master

A **read-data** time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS28EA00 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS28EA00 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of t_{RL} + δ (rise time) on one side and the internal timing generator of the DS28EA00 on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}) in which the master must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS28EA00 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS28EA00 attached to a 1-Wire line. For multidevice configurations, t_{REC} needs to be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the DS2482-x00 or DS2480B 1-Wire line drivers can be used.

IMPROVED NETWORK BEHAVIOR (SWITCHPOINT HYSTERESIS)

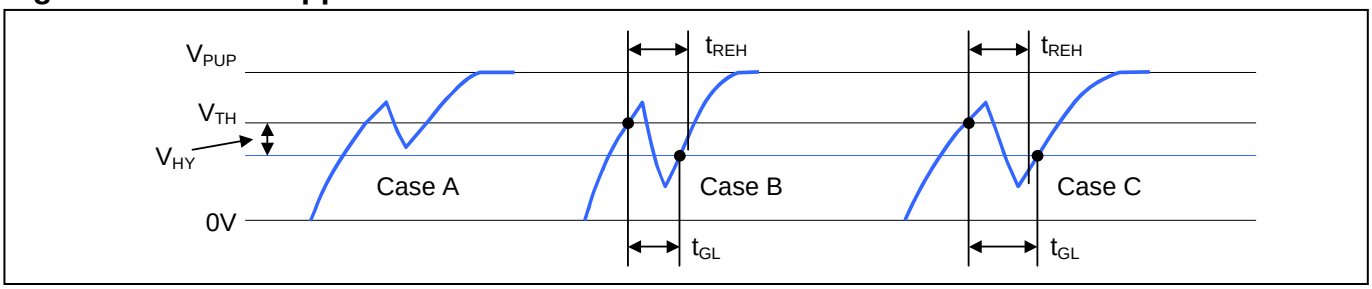
In a 1-Wire environment, line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up, or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, consequently, result in a search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS28EA00 uses a new 1-Wire front end, which makes it less sensitive to noise and also reduces the magnitude of noise injected by the slave device itself..

The 1-Wire front end of the DS28EA00 differs from traditional slave devices in four characteristics.

1) The falling edge of the presence pulse has a controlled slew rate. This provides a better match to the line impedance than a digitally switched transistor, converting the high frequency ringing known from traditional devices into a smoother low-bandwidth transition. The slew rate control is specified by the parameter t_{FPD}, which has different values for standard and Overdrive speed.
2) There is additional low-pass filtering in the circuit that detects the falling edge at the beginning of a time slot. This reduces the sensitivity to high-frequency noise. This additional filtering does not apply at Overdrive speed.
3) There is a hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH} but does not go below V_{TH} - V_{HY}, it will not be recognized (Figure 15, Case A). The hysteresis is effective at any 1-Wire speed.
4) There is a time window specified by the rising edge hold-off time t_{REH} during which glitches are ignored, even if they extend below V_{TH} - V_{HY} threshold (Figure 15, Case B, $t_{GL} < t_{REH}$). Deep voltage droops or glitches that appear late after crossing the V_{TH} threshold and extend beyond the t_{REH} window cannot be filtered out and are taken as the beginning of a new time slot (Figure 15, Case C, $t_{GL} \geq t_{REH}$).

Devices that have the parameters V_{HY}, and t_{REH} specified in their electrical characteristics use the improved 1-Wire front end.

Figure 15. Noise Suppression Scheme



SEQUENCE DISCOVERY PROCEDURE

Precondition: The PIOB pin (EN\) of the first device in the chain is at logic 0. The PIOA pin (DONE\) of the first device connects to the PIOB of the second device in the chain, etc., as shown in Figure 16. The 1-Wire master detects the physical sequence of the devices in the chain by performing the following procedure:

Starting Condition: The master issues a Skip ROM command followed by a Chain ON command, which puts all devices in the **Chain ON** state. The pullup through R_{CO} of the PIOA pin charges the PIOA/PIOB connections to logic '1' level at all devices except for the first device in the chain. If a local VDD supply is not available, the master needs to activate a low-impedance bypass to the 1-Wire pullup resistor immediately after the inverted chain control byte until the PIOA/PIOB connections have reached a voltage equivalent to the logic '1' level.

First Cycle: The master sends a **Conditional Read ROM** command, which causes the first device in the chain to respond with its 64-bit Registration Number. The master memorizes the Registration Number and the fact that this is the first device in the chain. Next the master transmits a **Chain DONE** command. Through the PIOA pin of the just discovered device, this asserts logic 0 at the PIOB pin of the second device in the chain and also prevents the just discovered device from responding again.

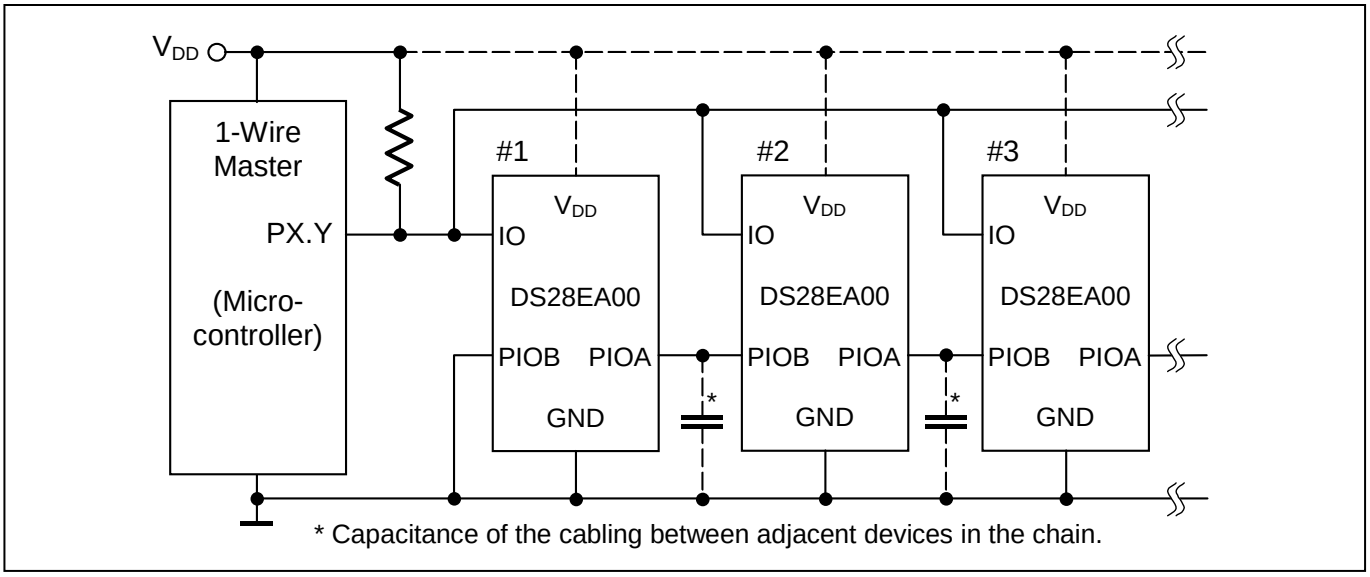
Second Cycle: The master sends a **Conditional Read ROM** command. Since DS28EA00 #2 is the only device in the chain with a LOW level at PIOB it responds with its Registration Number. The master stores the registration number with the sequence number of 2. Device #1 cannot respond since it is in Chain DONE state. Next the master transmits a **Chain DONE** command.

Additional Cycles: To identify the Registration Numbers of the remaining devices and their physical sequence, the master repeats the steps of **Conditional Read ROM**, and **Chain DONE**. If there is no response to Conditional Read ROM, all devices in the chain are identified.

Ending Condition

At the end of the discovery process all devices in the chain are in the Chain DONE state. The master should end the sequence discovery by issuing a Skip ROM command followed by a **Chain OFF** command. This puts all the devices into the Chain OFF state, and transfers control of the PIOB and PIOA pins to the PIO Access Read and Write function commands.

Figure 16. DS28EA00 Wired for Sequence Discovery ("Chain Function")



COMMAND-SPECIFIC 1-Wire COMMUNICATION PROTOCOL—LEGEND

SYMBOL	DESCRIPTION
RST	1-Wire Reset Pulse generated by master.
PD	1-Wire Presence Pulse generated by slave.
SELECT	Command and data to satisfy the ROM function protocol.
SKIPR	ROM Function Command "Skip ROM".
CDRR	ROM Function Command "Conditional Read ROM".
WSP	Command "Write Scratchpad".
RSP	Command "Read Scratchpad".
CPSP	Command "Copy Scratchpad".
CTEMP	Command "Convert Temperature".
RPM	Command "Read Power Mode".
RCLE	Command "Recall EEPROM".
PIOR	Command "PIO Access Read".
PIOW	Command "PIO Access Write".
CHAIN	Command "Chain".
<n bytes>	Transfer of n bytes.
CRC	Transfer of a CRC byte
<xxh>	Transfer of a specific byte value “xx” (hexadecimal notation)
00 loop	Indefinite loop where the master reads 00 bytes.
FF loop	Indefinite loop where the master reads FF bytes.
AA loop	Indefinite loop where the master reads AA bytes.
xx loop	Indefinite loop where the slave transmits the inverted invalid control byte.
CONVERSION	A temperature conversion takes place; activity on the 1-Wire bus is permitted only with local V_{DD} supply.
PROGRAMMING	Data transfer to Backup EEPROM; activity on the 1-Wire bus is permitted only with local V_{DD} supply.

COMMAND-SPECIFIC 1-Wire COMMUNICATION PROTOCOL—COLOR CODES

Master to slave	Slave to master	Programming	Conversion

WRITE SCRATCHPAD

RST	PD	Select	WSP	<3 bytes>	RST	PD

READ SCRATCHPAD

RST	PD	Select	RSP	<8 bytes>	CRC	FF loop

COPY SCRATCHPAD (PARASITE POWERED)

RST	PD	Select	CPS	Wait $t_{PROGMAX}$	FF loop

During the wait, the master should activate a low-impedance bypass to the 1-Wire pullup resistor.

COPY SCRATCHPAD (LOCAL V_{DD} POWERED)

RST	PD	Select	CPS	<00h>	FF loop

The master reads 00h bytes until the write cycle is completed.

CONVERT TEMPERATURE (PARASITE POWERED)

RST	PD	Select	CTEMP	Wait $t_{CONVMAX}$	FF loop

During the wait, the master should activate a low-impedance bypass to the 1-Wire pullup resistor.

CONVERT TEMPERATURE (LOCAL V_{DD} POWERED)

RST	PD	Select	CTEMP	<00h>	FF loop

The master reads 00h bytes until the conversion is completed.

READ POWER MODE (PARASITE POWERED)

RST	PD	Select	RPM	<00h>

READ POWER MODE (LOCAL V_{DD} POWERED)

RST	PD	Select	RPM	<FFh>

RECALL EEPROM

RST	PD	Select	RCLE	<00h>	FF loop

The master reads 00h bytes until the recall is completed.

PIO ACCESS READ

RST	PD	Select	PIOR	<PIO Status Byte>

See the Command description for behavior if the device is in Chain ON or Chain DONE state.

Continues until master sends Reset Pulse

PIO ACCESS WRITE (SUCCESS)

RST	PD	Select	PIOW	<PIO Output data>	<$\overline{\text{PIO Output data}}$>	<AAh>	<PIO Status Byte>

Loop until master sends Reset Pulse

PIO ACCESS WRITE (INVALID DATA BYTE)

RST	PD	Select	PIOW	<PIO Output data>	<invalid data byte>	FF loop

The PIO Access Write command is ignored by the device while in Chain ON or Chain DONE state.

CHANGE CHAIN STATE (SUCCESS)

RST	PD	Select	CHAIN	<Chain Control Byte>	<$\overline{\text{Chain Control Byte}}$>	AA loop

CHANGE CHAIN STATE (TRANSMISSION ERROR)

RST	PD	Select	CHAIN	<Any Byte>	< Byte ≠ inverted Previous byte>	00 loop

CHANGE CHAIN STATE (INVALID CONTROL BYTE)

RST	PD	Select	CHAIN	<Invalid Control Byte>	<Inverted Previous Byte >	xx loop

SEQUENCE DISCOVERY EXAMPLE

RST	PD	SKIPR	CHAIN	<5Ah>	<A5h>	Wait for chain to charge	<AAh>

Put all devices into Chain ON state.

RST	PD	CDRR	<Registration Number>	CHAIN	<96h>	<69h>	<AAh>

Identify the first device and put it into Chain DONE state.

RST	PD	CDRR	<Registration Number>	CHAIN	<96h>	<69h>	<AAh>

Identify the next device and put it into Chain DONE state. Repeat this sequence until no device responds.

RST	PD	CDRR	<8 bytes FFh>

No response, all devices have been discovered.

RST	PD	SKIPR	CHAIN	<3Ch>	<C3h>	<AAh>

Put all devices into Chain OFF state.

For the sequence discovery to function properly, the logic state at PIOB (EN\) must not change during the transmission of the Conditional Read ROM command code, and, if the device responds, must stay at logic 0 until the entire 64-bit Registration Number is transmitted.