Rev 1; 3/04

DALLAS SEMICONDUCTOR MAXIM

Ultra3 LVD/SE SCSI 14-Line Terminator

General Description

The DS2127 Ultra3 LVD/SE SCSI terminator provides low-voltage differential (LVD)/single-ended (SE) terminations for 14 SCSI lines. Through the voltage on the DIFF_CAP pin, the device detects the types of drivers on the bus. If the device is connected in an LVD-only bus, the DS2127 provides LVD termination. If any single-ended devices are connected to the bus, the DS2127 uses SE termination. If any high-voltage differential (HVD) devices are connected to the bus, the DS2127 isolates itself from the SCSI bus. The mode change has a built-in delay that is determined by an integrated SPI-3 mode change filter/delay. The terminating resistors can also be disconnected from the bus by asserting the ISO pin.

For the LVD termination, the DS2127 provides 14 precisely trimmed resistors. Each resistor is biased with two current sources to a fail-safe state. For SE termination, the DS2127 provides 14 precision 110Ω resistors and one regulator for active-negation bias.

Applications

SCSI Array Backplane

SCSI Cables

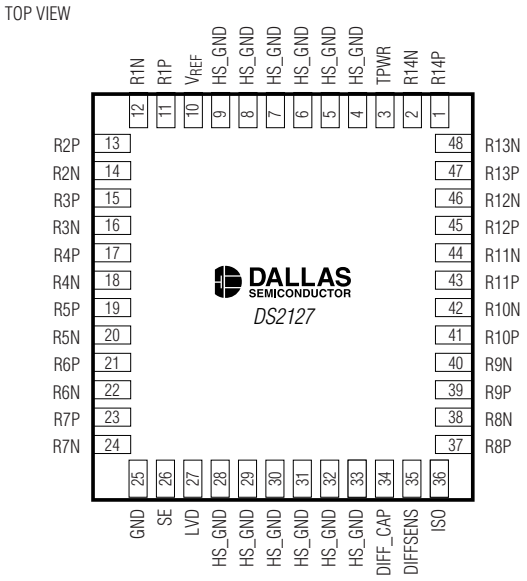
Features

- **Fully Compliant with Ultra2, Ultra3, Ultra160, and Ultra320 SCSI Standards**
- **Provides LVD/SE Termination for 14 Signal Pairs**
- **Auto-Selection of LVD or SE Termination**
- **5% Tolerance on SE and LVD Termination Resistance**
- **Low 3pF Power-Down Capacitance**
- **Built-In Mode-Change Filter/Delay**
- **On-Board Thermal-Shutdown Circuitry**
- **SCSI Bus Hot-Plug Compatible**
- **Fully Supports Actively Negated SE SCSI Signals**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
DS2127	0°C to +70°C	48 LQFP	DS2127

Pin Configuration



LQFP

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on All Pins Relative to Ground .....-0.3V to +6.0V
V_{REF} Continuous Output Current.....±200mA
Operating Temperature Range.....0°C to +70°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Soldering Temperature .....See IPC/JEDEC J-STD-020A Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(TPWR = $V_{TPWR(MIN)}$ to $V_{TPWR(MAX)}$, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TPWR Operating Supply Range (Note 1)	V_{TPWR}	LVD	2.7	3.3	5.5	V
		SE	4	5.0	5.5	
TPWR SUPPLY CURRENT						
TPWR Supply Current (All Lines Open)	I_{TPWR_LVD}	LVD SCSI mode			32	mA
	I_{TPWR_SE}	SE SCSI mode			10	
	I_{TPWR_ISO}	ISO mode (terminators disabled)			750	µA
LVD TERMINATION (Applies to each line pair, 1 to 14 in LVD mode)						
Differential-Mode Termination Resistance	R_{DM}		100		110	Ω
Common-Mode Termination Resistance	R_{CM}	R_P and R_N shorted together ($V_{CM(MAX)}$ = 2V, $V_{CM(MIN)}$ = 0.5V)	110		165	Ω
Differential-Mode Bias	V_{DM}	All lines open	100		125	mV
Common-Mode Bias	V_{CM}	R_P and R_N shorted together (Note 1)	1.15	1.25	1.35	V
SE TERMINATION (Applies to single-ended terminators, 1 to 14 in SE mode)						
Single-Ended Mode Termination Resistance	R_{SE}	R_{SE} = (V_{LX} - 0.2) / I_{LX}, where V_{LX} = voltage at terminator pin with pin unloaded and I_{LX} = current for each terminator pin with the pin forced to 0.2V	104.5	110	115.5	Ω
Termination Current	I_{SE}	Signal level at 0.2V, all lines low	-21	-24	-25.4	mA
		Signal level at 0.5V	-18		-22.4	
SE Voltage Reference	V_{REF}		2.7	2.85	3.0	V
Pin Leakage		With ISO high			400	nA
Single-Ended GND Resistance	R_{GND}	Measured at R_P pins, I = 10mA		20	60	Ω
TERMINATOR PIN CAPACITANCE						
Terminator Pin Capacitance	C_{IN}	With ISO high (Note 2)			3	pF
V_{REF} REGULATOR						
1.25V Regulator Output Voltage	V_{REF_LVD}	0.5V ≤ V_{CM} ≤ 2.0V, V_{CM} applied to all R_P and R_N lines simultaneously	1.15	1.25	1.35	V
1.25V Regulator Short-Circuit Source Current	I_{SOURCE}	V_{REF} = 0V	-375	-700	-1000	mA
1.25V Regulator Short-Circuit Sink Current	I_{SINK}	V_{REF} = 3.3V	170	300	700	mA

ELECTRICAL CHARACTERISTICS (continued)

(TPWR = $V_{TPWR(MIN)}$ to $V_{TPWR(MAX)}$, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REF} REGULATOR						
1.25V Regulator Line Regulation		V_{REF} unloaded; vary TPWR from 2.7V to 5.5V		1.0	2.5	%
2.85V Regulator			2.7	2.85	3.0	V
2.85V Regulator Short-Circuit Source Current		V_{REF} = 0V	-375	-700	-1000	mA
2.85V Regulator Short-Circuit Sink Current		V_{REF} = 3.3V	170	300	700	mA
2.85V Regulator Line Regulation		V_{REF} unloaded; vary TPWR from 2.7V to 5.5V		1.0	2.5	%
DIFFSENS OUTPUT						
DIFFSENS Driver Output Voltage	V_{DSO}	-5mA ≤ $I_{DIFFSENS}$ ≤ 50µA	1.2		1.4	V
DIFFSENS Driver Source Current	I_{DSH}	$V_{DIFFSENS}$ = 0V	-15		-5	mA
DIFFSENS Driver Sink Current	I_{DSL}	$V_{DIFFSENS}$ = 2.75V	100		200	µA
DIFFSENS Leakage (Note 3)	$I_{LEAK, LOW}$	With ISO high, $\lvert V_{DIFFSENS} \rvert$ = 0.3V	-3		+1	µA
	$I_{LEAK, HIGH}$	With ISO high, $\lvert V_{DIFFSENS} - V_{TPWR} \rvert$ = 0.3V	1		3	
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		For increasing temperature		130		°C
Thermal-Shutdown Hysteresis				10		°C
MODE CHANGE DELAY/FILTER						
Mode Change Delay	t_{DELAY}		0.66	1.25	2.00	ms
LOGICAL SIGNALS (ISO)						
Input Low Voltage	V_{IL}		-0.3		+0.8	V
Input High Voltage	V_{IH}		2.0		TPWR + 0.3	V
Input Current	I_{IL}	V_{CC} = 3.3V	-30	-10		µA
STATUS BITS (LVD, SE)						
Source Current	I_{OH}	V_{CC} = 3.3V, V_{LOAD} = 2.4V	-4	-6		mA
Sink Current	I_{OL}	V_{CC} = 3.3V, V_{LOAD} = 0.4V	2	5		mA
DIFF_CAP						
Input Current	IL	V_{IL} = -0.3V	-1		+1	µA
DIFF_CAP SE Operating Range	V_{SEOR}		-0.3		+0.5	V
DIFF_CAP LVD Operating Range	V_{LVDOR}		0.7		1.9	V
DIFF_CAP HVD Operating Range	V_{HVDOR}		2.4		V_{TPWR} + 0.3	V

Note 1: All voltages are referenced to ground.
Note 2: Guaranteed by design and not production tested.
Note 3: Room temperature only.

Ultra3 LVD/SE SCSI 14-Line Terminator

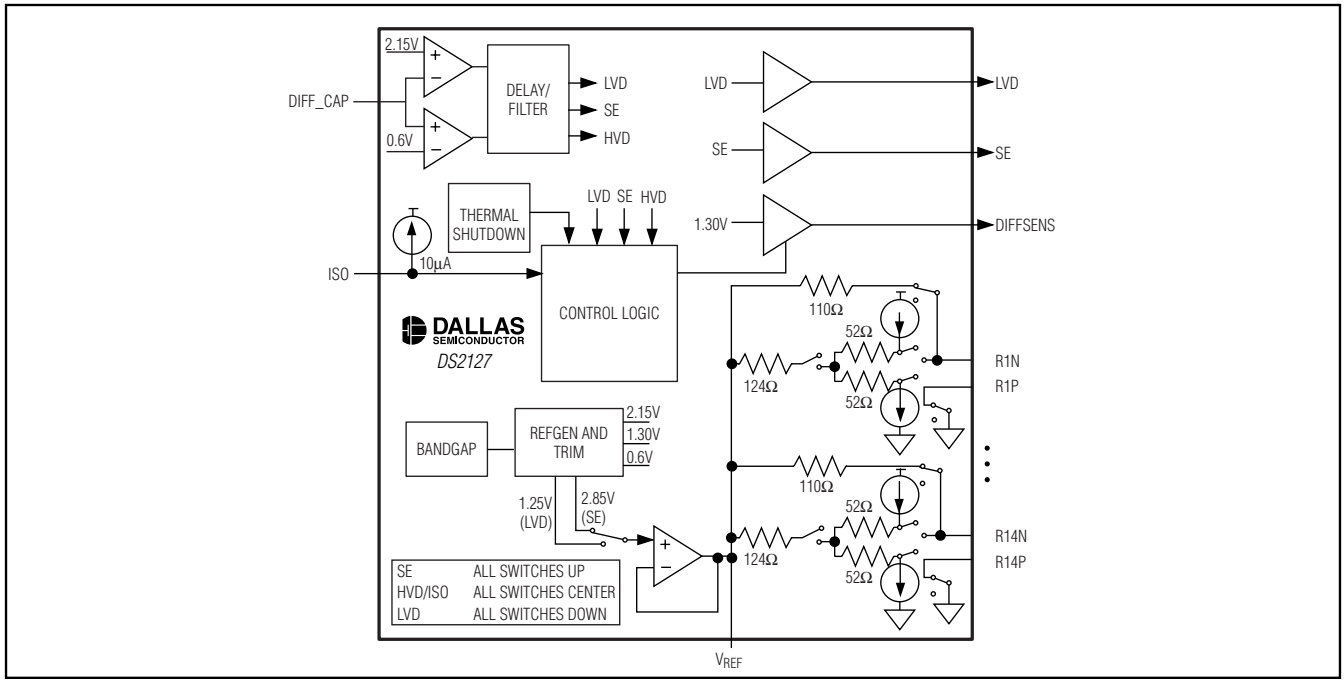

Figure 1. Block Diagram

Pin Description

PIN	NAME	FUNCTION
1, 2, 11–24, 37–48	R__P, R__N	Signal Termination. Connect to SCSI bus signal lines. Asserting ISO removes the terminators from the SCSI bus. R__P pins are the ground line for SE operation and the positive lines in differential mode. R__N pins are the signal lines in SE operation and the negative lines in differential mode.
3	TPWR	Termination Power. Connect to the SCSI TERMPWR line and decouple with a ceramic 2.2µF capacitor.
4–9, 28–33	HS_GND	Heat-Sink Ground. Internally connected to the mounting pad. These pins must be connected to ground. These pins should be connected to a ground plane with the layout optimized for heat transfer.
10	V_{REF}	Regulator Output Voltage. This must be decoupled with a 4.7µF capacitor. Asserting ISO floats this output. A high-frequency capacitor (0.1µF) should also be placed on the V_{REF} pin in applications that use fast rise/fall-time drivers.
25	GND	Signal Ground
26	SE	SE Mode Indicator. A high state indicates SE mode detected on SCSI bus.
27	LVD	LVD Mode Indicator. A high state indicates LVD mode detected on SCSI.
34	DIFF_CAP	DIFFSENSE Capacitor. Connect a 0.1µF capacitor for the DIFFSENSE filter. Input to detect the type of device (differential or single-ended) on the SCSI bus.
35	DIFFSENS	DIFFSENSE. Output to drive the SCSI bus DIFFSENS line.
36	ISO	Isolation Input. When pulled high, terminating resistors and biasing current sources are removed from the SCSI bus. When not connected to ground, the pin has a 10µA current source pulling the pin to the high state.

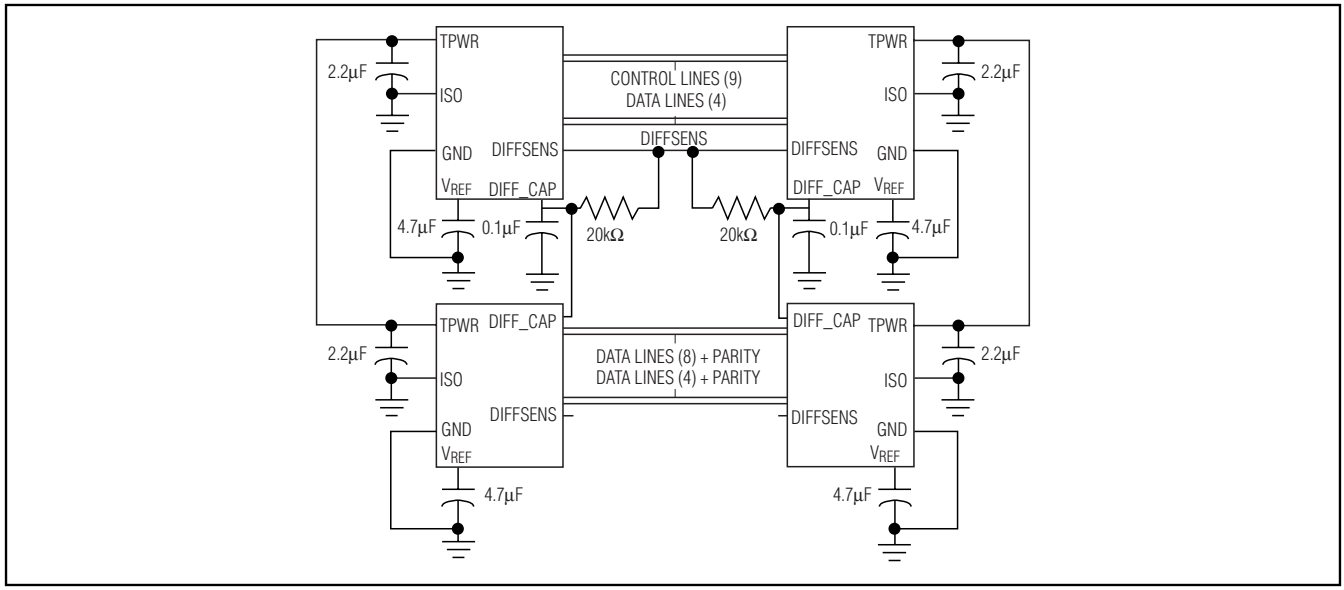

Figure 2. Typical Operating Circuit

Detailed Description

The DS2127 provides dual-mode active terminators with auto-switching SE and LVD termination for 14 SCSI lines. The DIFFSENSE signal performs mode detection and selection.

In LVD mode, the termination configuration is a y-type terminator with a 105Ω differential resistance and a 150Ω common-mode resistance. The termination resistor is biased with two current sources and the common-mode node is connected to a 1.25V voltage regulator. A fail-safe bias of 112mV is maintained when no drivers are connected to the SCSI bus.

In SE mode, each negative signal input pin is connected to 2.85V through a 110Ω resistor.

In HVD mode, the termination resistors are isolated from the SCSI bus and the resistor pins are left floating. The voltage regulator is powered down and the V_{REF} pin is in a high-impedance state.

The DIFF_CAP pin is connected to the SCSI DIFFSENSE line and monitors the voltage to determine the proper operating mode of the device. Any DIFFSENSE voltage below 0.5V indicates single ended; any DIFFSENSE voltage between 0.7V and 1.9V is LVD, and above 2.4V is an HVD SCSI. On power-up, the DS2127 assumes SE mode. If the voltage on the DIFF_CAP is between 0.7V and 1.9V, the device waits t_{DELAY} before entering the LVD mode. The delay is the same when changing modes. A new mode change can start at any time after a previous mode change has been detected.

Typically, four DS2127s are used in a SCSI bus segment. On two chips, the DIFF_CAP inputs at each end of the bus should be connected together. There should be a 50Hz noise filter implemented on DIFF_CAP at each end of the bus, as close as possible to the DIFF_CAP pins. This filter consists of a 20kΩ resistor between the DIFFSENS and DIFF_CAP pins, and a 0.1µF capacitor from DIFF_CAP to GND. See Figure 2 for the typical operating circuit.

When ISO is connected to TPWR, the termination pins are isolated from the SCSI bus and V_{REF} becomes inactive, and the device is in a low-power state. During thermal shutdown, the termination pins are isolated from the SCSI bus and V_{REF} becomes high impedance. The DIFFSENS driver is shut down during either of these two events. LVD and SE signals indicate whether the SCSI bus segment is in LVD or SE mode.

Chip Information

TRANSISTOR COUNT: 8114 CMOS and 87 Bipolar

PROCESS: BiCMOS

SUBSTRATE CONNECTED TO GROUND

Thermal Information

Thermal Resistance (junction-to-ambient):
θ_{JA} = +29°C/W

Thermal Resistance (junction-to-case):
θ_{JC} = +10°C/W

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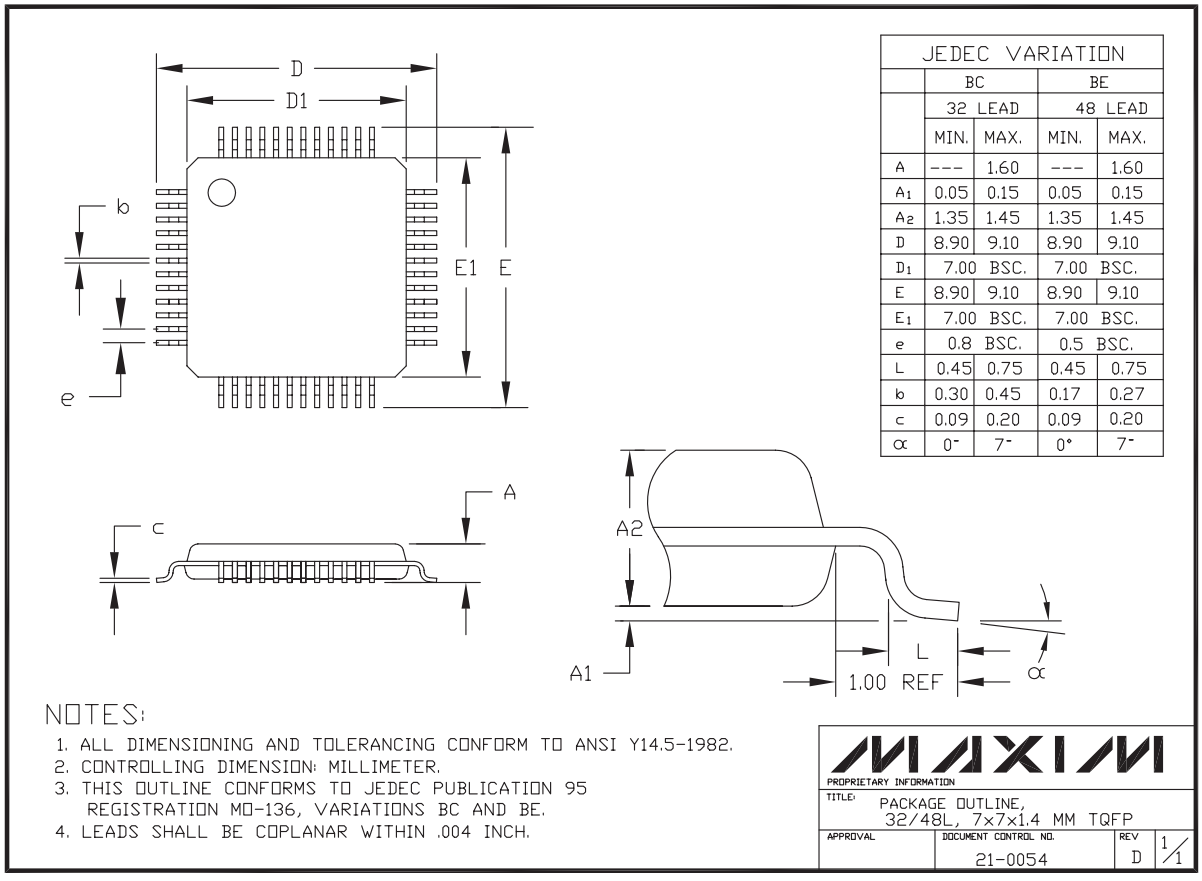
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



JEDEC VARIATION				
	BC		BE	
	32 LEAD		48 LEAD	
	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60
A_1	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D_1	7.00 BSC.		7.00 BSC.	
E	8.90	9.10	8.90	9.10
E_1	7.00 BSC.		7.00 BSC.	
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
c	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC AND BE.
4. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.4 MM TQFP			
APPROVAL	DOCUMENT CONTROL NO. 21-0054	REV. D	1/1