

PowerMOS transistor Logic level FET

BUK581-60A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

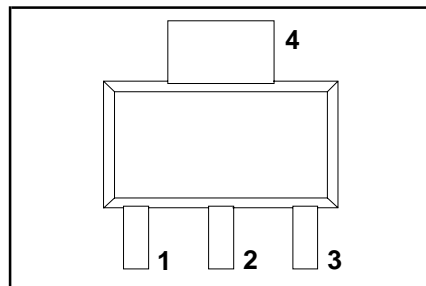
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	1.5	A
P_{tot}	Total power dissipation	1.5	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; $V_{GS} = 5\text{ V}$	0.40	Ω

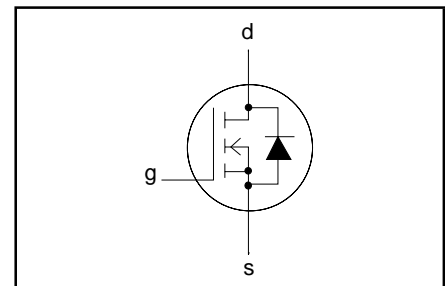
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	$T_{amb} = 25\text{ }^\circ\text{C}$	-	1.5	A
I_D	Drain current (DC)	$T_{amb} = 100\text{ }^\circ\text{C}$	-	1	A
I_{DM}	Drain current (pulse peak value)	$T_{amb} = 25\text{ }^\circ\text{C}$	-	6	A
P_{tot}	Total power dissipation	$T_{amb} = 25\text{ }^\circ\text{C}$	-	1.5	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	From junction to solder point ¹	Mounted on any PCB .	-	14	17	K/W
$R_{th\ j-amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	-	85	K/W

¹ Temperature measured at solder joint on drain tab.

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STATIC CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 0.1\text{ mA}$	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 60\text{ V}; V_{GS} = 0\text{ V};$	-	1	10	μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 60\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 15\text{ V}; V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 1.5\text{ A}$	-	0.28	0.40	Ω

DYNAMIC CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 1.5\text{ A}$	1.0	2.2	-	S
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	170	300	pF
C_{oss}	Output capacitance		-	60	100	pF
C_{rss}	Feedback capacitance		-	25	50	pF
t_{don}	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 3\text{ A};$ $V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega;$ $R_{gen} = 50\text{ }\Omega$	-	7	10	ns
t_r	Turn-on rise time		-	45	55	ns
t_{doff}	Turn-off delay time		-	15	25	ns
t_f	Turn-off fall time		-	25	35	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

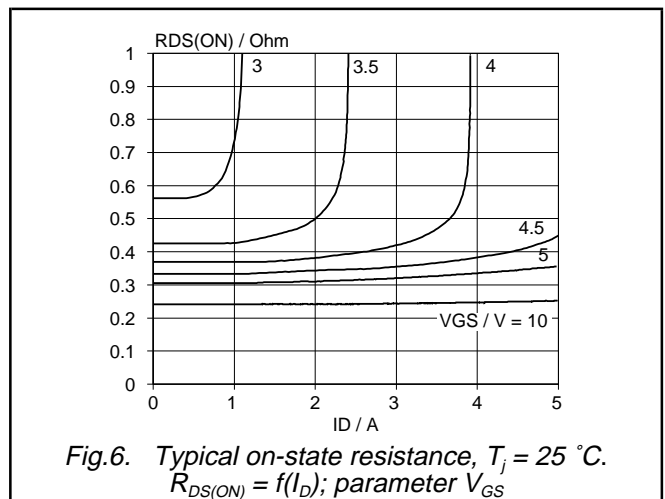
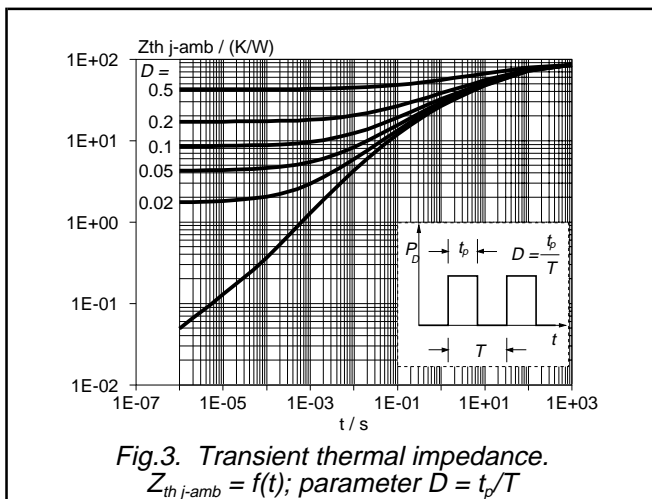
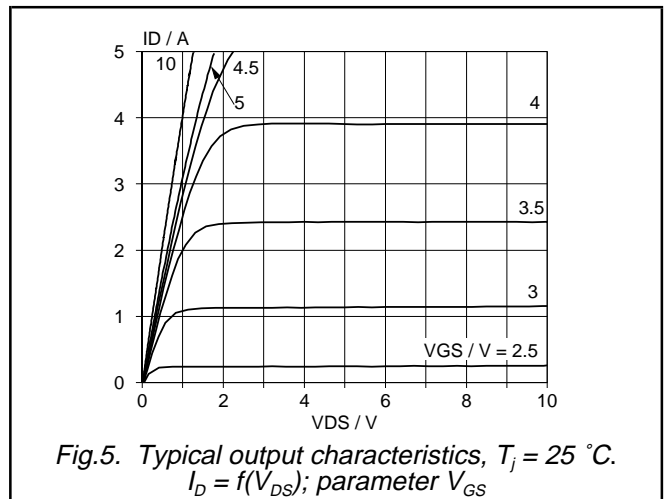
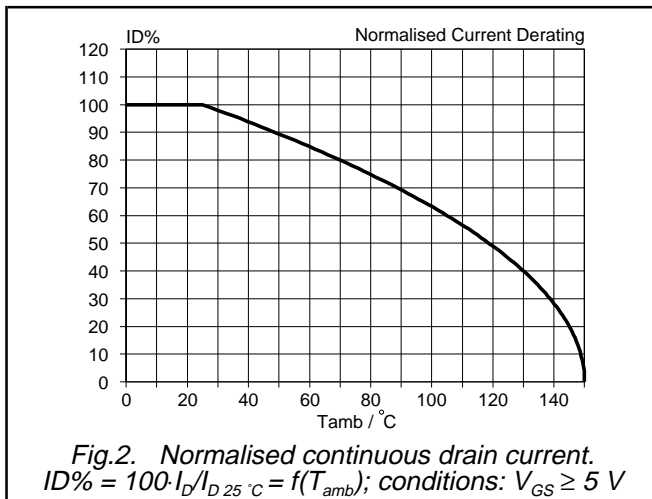
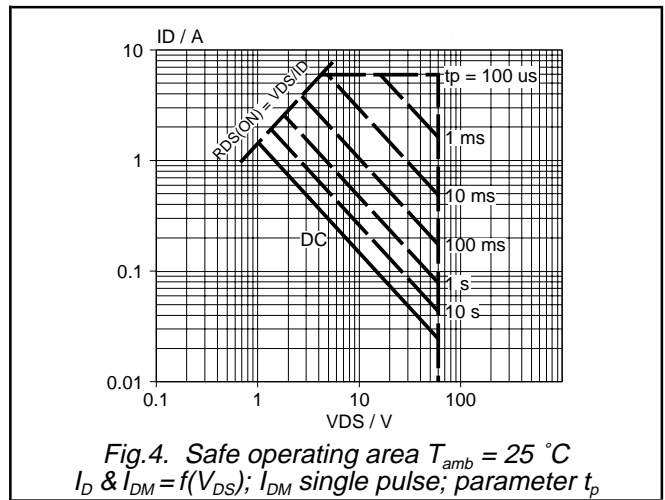
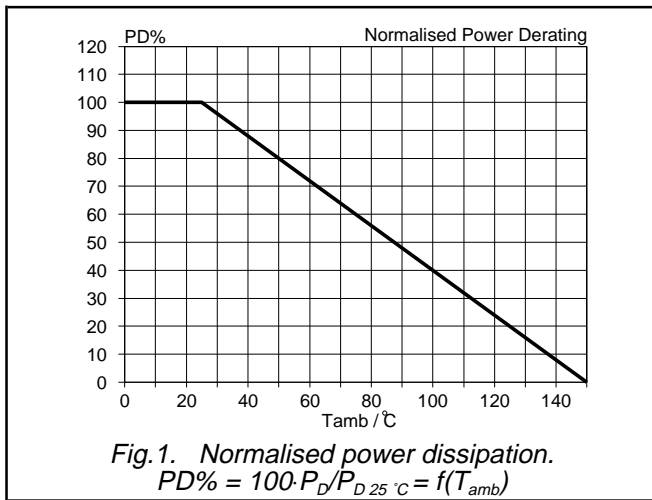
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	1.5	A
I_{DRM}	Pulsed reverse drain current	-	-	-	6	A
V_{SD}	Diode forward voltage	$I_F = 1.5\text{ A}; V_{GS} = 0\text{ V}$	-	0.85	1.1	V
t_{rr}	Reverse recovery time	$I_F = 1.5\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$ $V_{GS} = -10\text{ V}; V_R = 30\text{ V}$	-	30	-	ns
Q_{rr}	Reverse recovery charge		-	50	-	nC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non repetitive unclamped inductive turn-off energy	$I_D = 1.5\text{ A}; V_{DD} \leq 25\text{ V}$ $V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega$ $T_{amb} = 25\text{ }^\circ\text{C}$	-	-	10	mJ

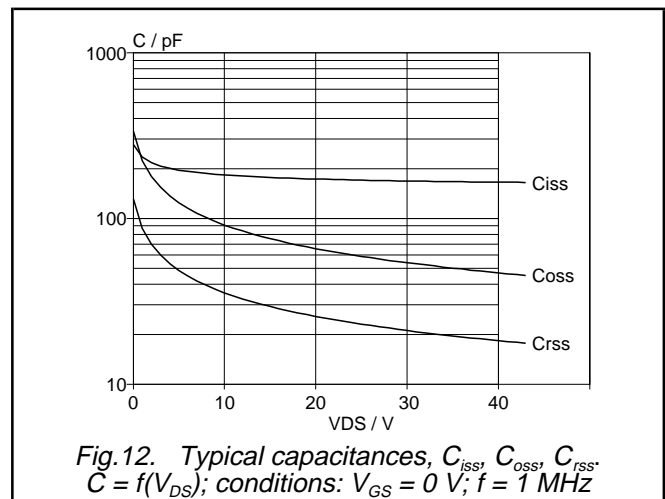
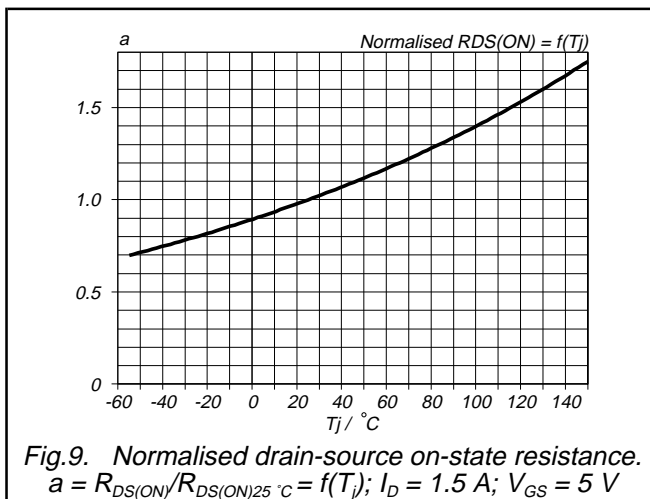
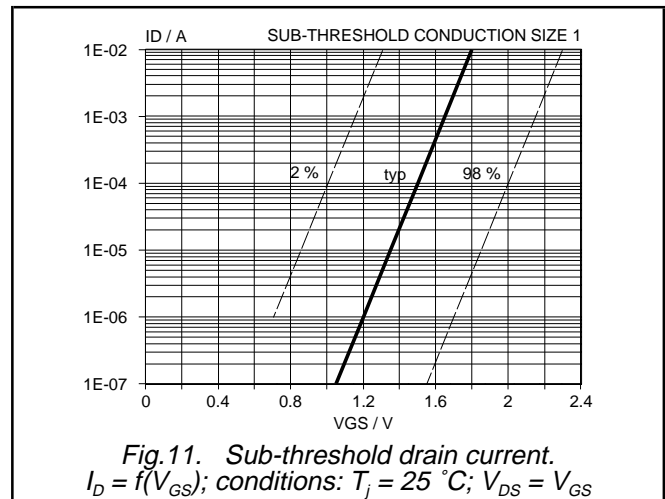
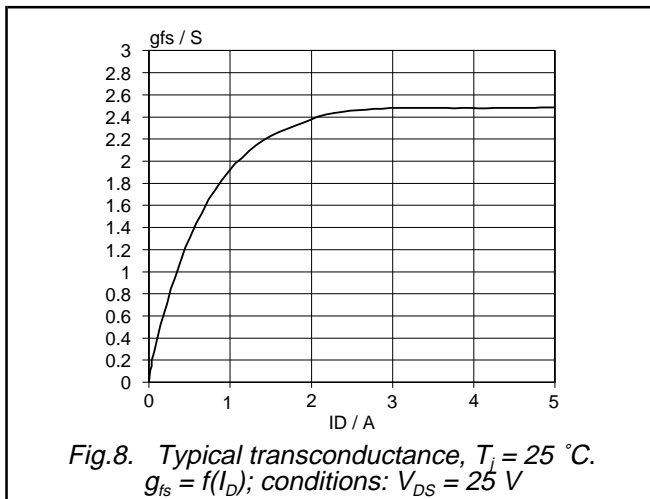
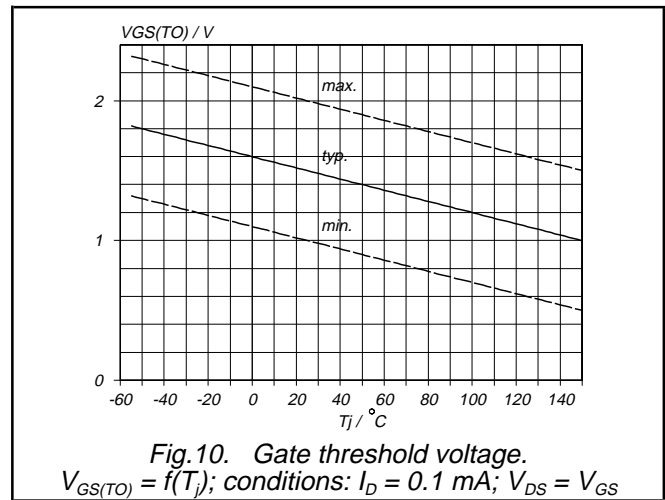
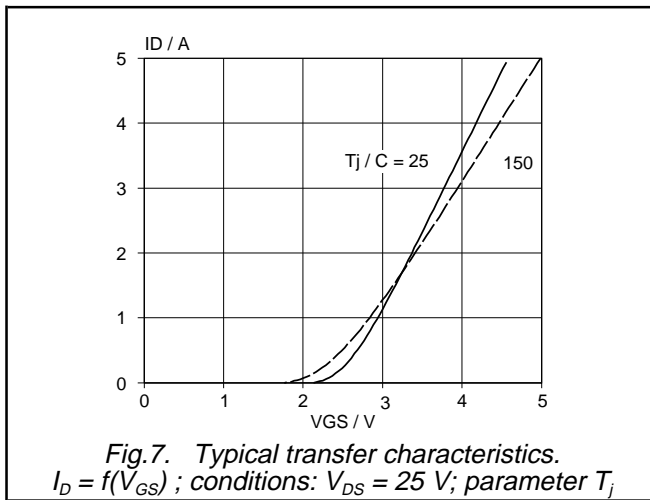
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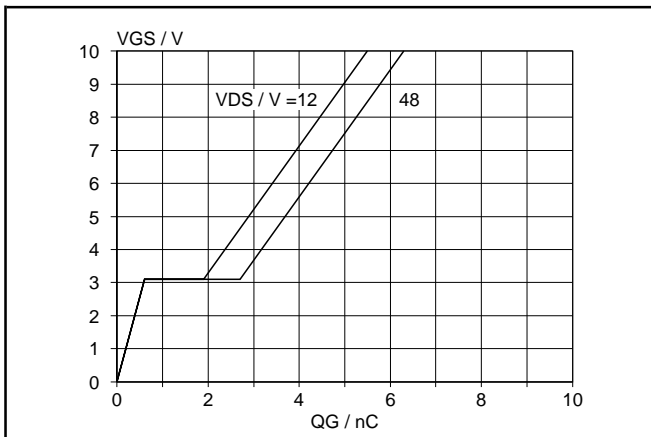


Fig. 13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 1.5$ A; parameter V_{DS}

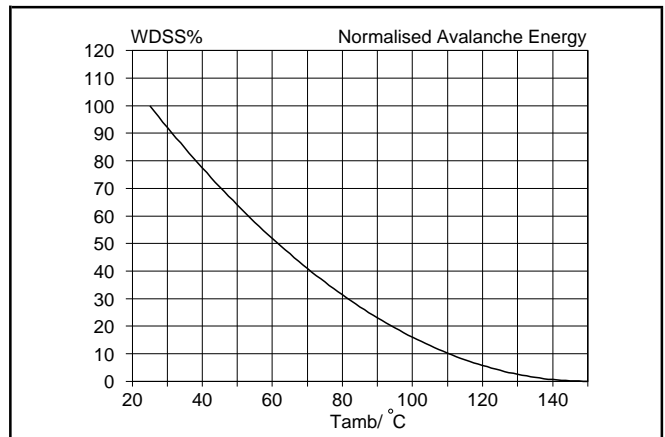


Fig. 15. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 1.5$ A

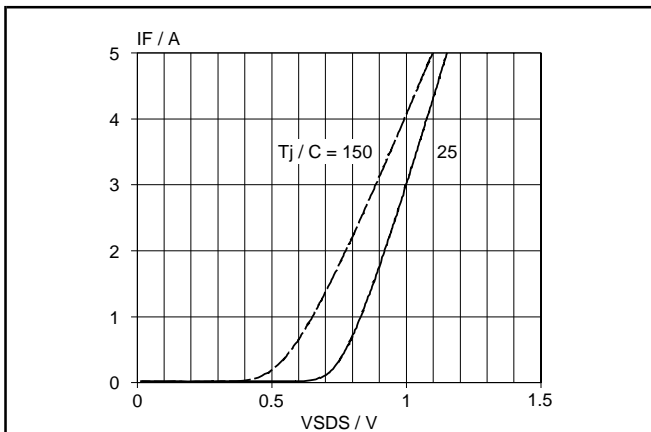


Fig. 14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

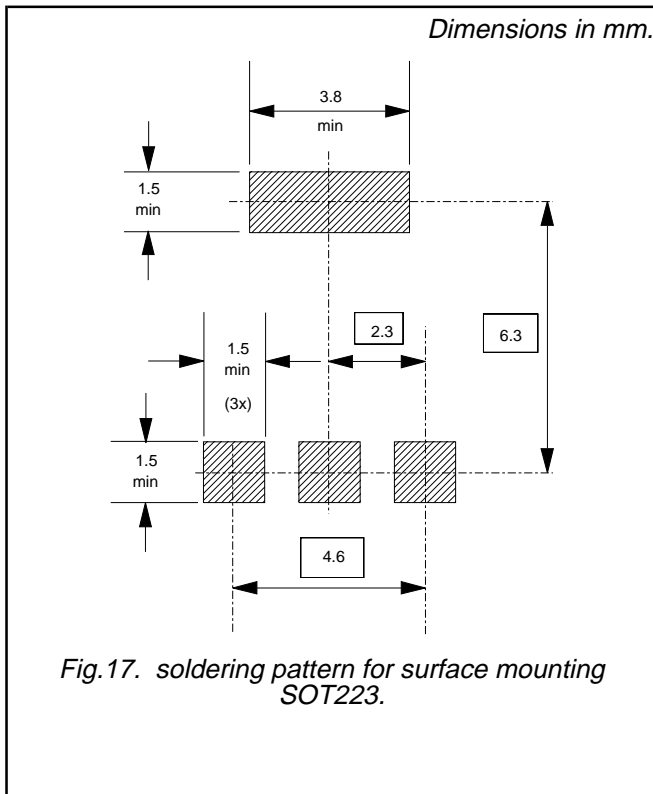


Fig. 16. Avalanche energy test circuit.
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

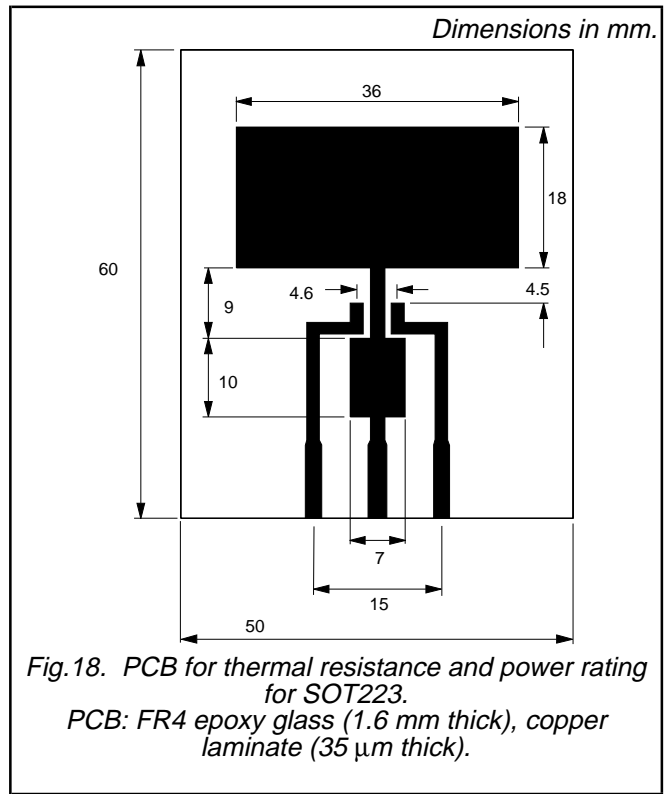
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MOUNTING INSTRUCTIONS



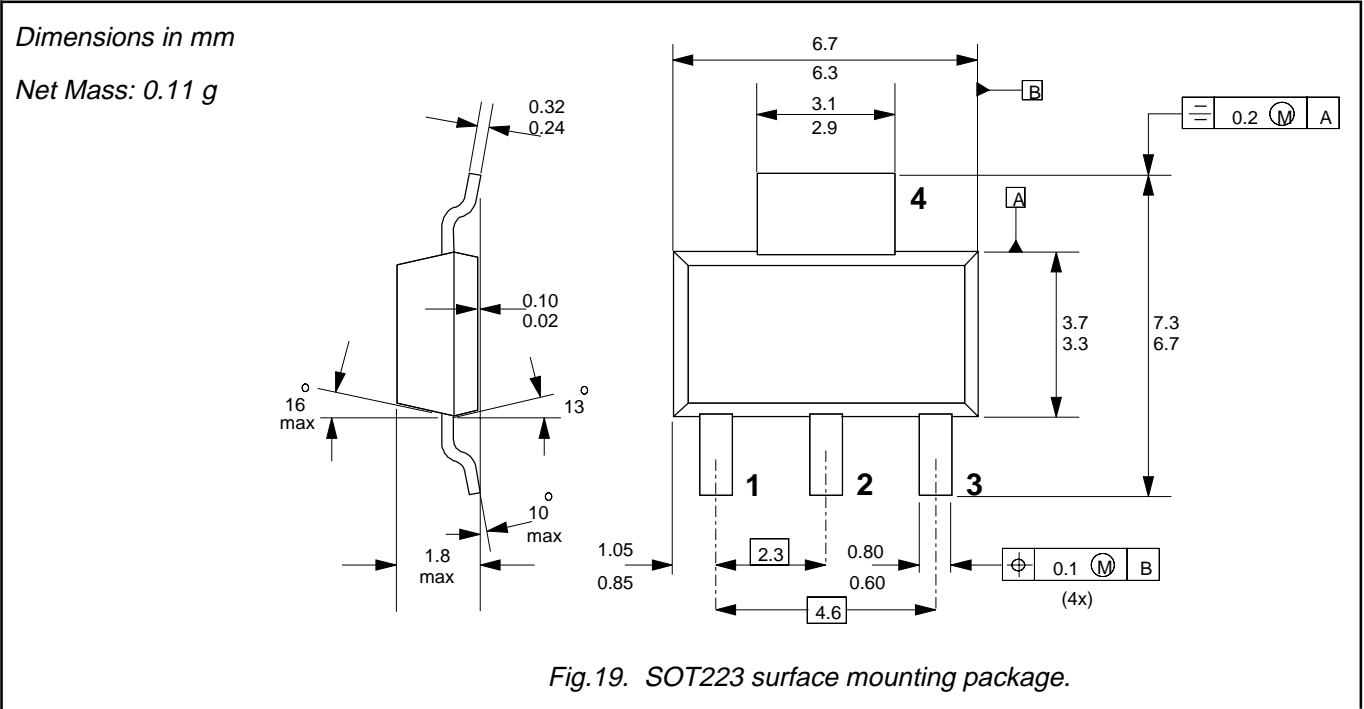
PRINTED CIRCUIT BOARD



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MECHANICAL DATA



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to surface mounting instructions for SOT223 envelope.
3. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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