PRELIMINARY DATA SHEET

BSP 3505D
Baseband
Sound Processor

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MICRONAS

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Baseband Sound Processor

Release Notes: The hardware description in this document is valid for the BSP 3505D version A2.

1. Introduction

The **BSP 3505D** is designed as a single-chip Baseband Sound Processor for applications in analog and digital TV sets, video recorders, and satellite receivers.

The IC is produced in submicron CMOS technology, and is fully pin and software compatible to the MSP 34xx family. The BSP 3505D is available in a PLCC68, PSDIP64, PSDIP52, PQFP80, and in a PQFP44 package.

Note: The BSP 3505D version has reduced control registers and less functional pins. The remaining registers are software compatible to the MSP 34xxD. The pinning is compatible to the MSP 34xxD.

1.1. BSP 3505D Integrated Functions

– Stereo baseband input via integrated A/D converters

– Two stereo D/A converters

– AVC: Automatic Volume Correction

– Bass, treble, volume, loudness processing

– Full SCART in/out matrix without restrictions

– spatial effect (pseudostereo / basewidth enlargement)

– Digital control output pins D_CTR_OUT0/1

– Reduction of necessary controlling

– Less external components

1.2. Features of the DSP-Section

– flexible selection of audio sources to be processed

– digital baseband processing: volume, bass, treble, loudness, and spatial effects

– simple controlling of volume, bass, treble, loudness, and spatial effects

1.3. Features of the Analog Section

– two selectable analog stereo audio baseband inputs (= two SCART inputs)
input level: ≤2 V RMS,
input impedance: ≥25 kΩ

– one selectable analog mono input:
input level: ≤2 V RMS,
input impedance: ≥15 kΩ

– stereo high-quality A/D converter, S/N-Ratio: ≥85 dB

– 20 Hz to 20 kHz bandwidth for SCART-to-SCART-copy facilities

– loudspeaker: stereo four-fold oversampled D/A-converter
output level per channel: max. 1.4 VRMS
output resistance: max. 5 kΩ
S/N-ratio: ≥85 dB at maximum volume
max. noise voltage in mute mode: ≤10 µV
(BW: 20 Hz ...16 kHz)

– stereo four-fold oversampled D/A converter supplying a stereo SCART-output
output level per channel: max. 2 V RMS,
output resistance: max. 0.5 kΩ,
S/N-Ratio: ≥85 dB (20 Hz...16 kHz)

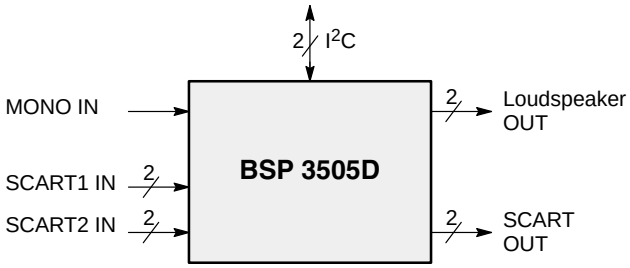


Fig. 1–2: Main I/O Signals BSP 3505D

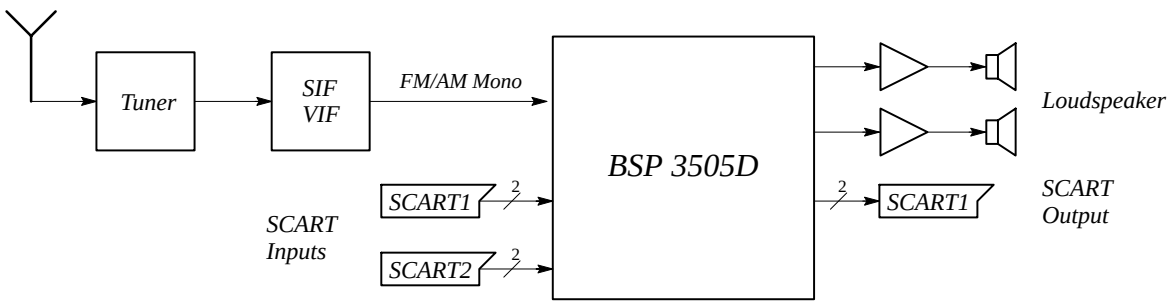


Fig. 1–1: Typical BSP 3505D application

2. Architecture of the BSP 3505D

Fig. 2–2 shows a simplified block diagram of the IC. Its architecture is split into two main functional blocks:

1. DSP (digital signal processing) section performing audio baseband processing
2. analog section containing two A/D-converters, four D/A-converters, and SCART-switching facilities.

2.1. Analog Section and SCART Switching Facilities

The analog input and output sections include full matrix switching facilities, which are shown in Fig. 2–1.

The switches are controlled by the ACB bits defined in the audio processing interface (see section 4. Programming the BSP 3505D).

2.1.1. Standby Mode

If the BSP 3505D is switched off by first pulling STANDBYQ low, and then disconnecting the 5 V, but keeping the 8 V power supply (**'Standby'-mode**), the switches S1 and S2 (see Fig. 2–1) maintain their position and function. This facilitates the copying from selected SCART-inputs to SCART-output in the TV-set's standby mode.

In case of power-on start or starting from standby, the IC switches automatically to the default configuration, shown in Fig. 2–1. This action takes place after the first I^2C transmission into the DSP part. By transmitting the ACB register first, the individual default setting mode of the TV set can be defined.

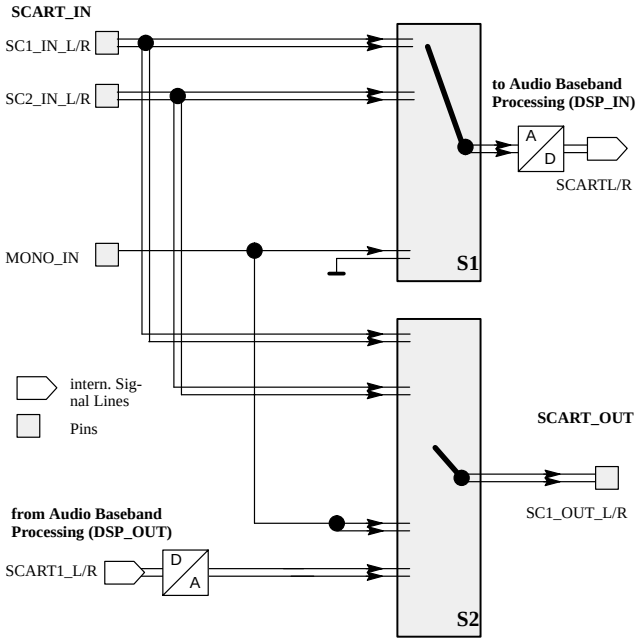


Fig. 2–1: SCART-Switching Facilities (see 4.4.12.) positions show the default configuration after Power On Reset.
Note: SCART_OUT is undefined after RESET!

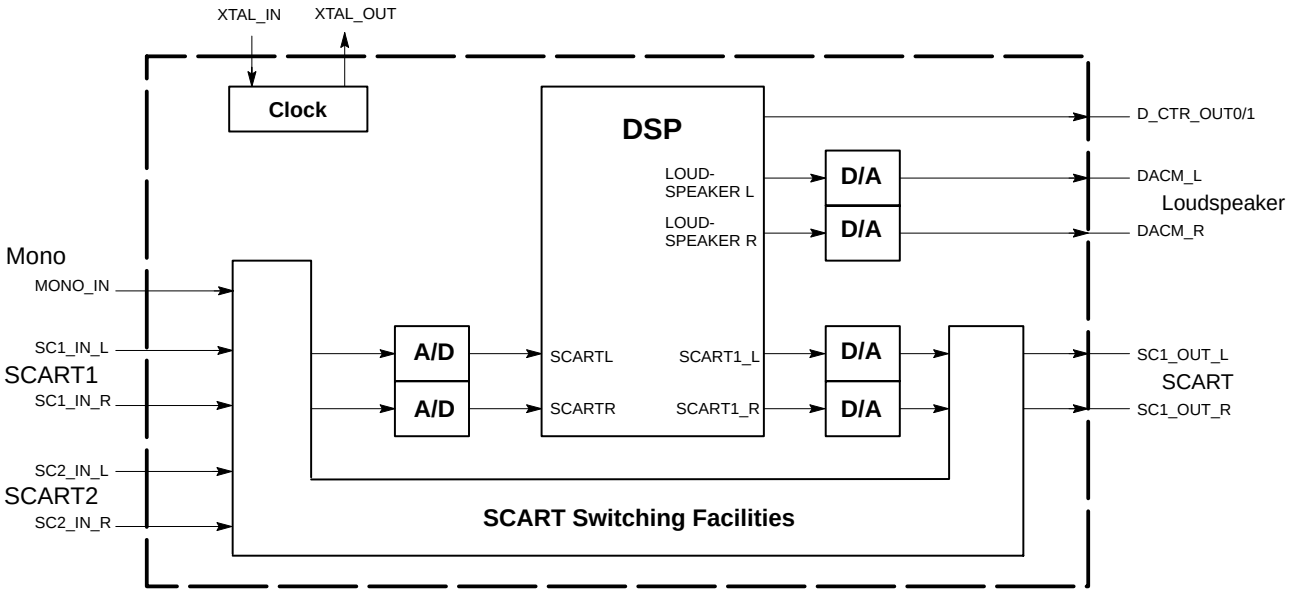


Fig. 2–2: Architecture of the BSP 3505D

2.2. BSP 3505D Audio Baseband Processing

All audio baseband functions are performed by digital signal processing (DSP). The DSP functions are grouped into three processing parts: input preprocessing, channel source selection, and channel postprocessing (see Fig. 2–3).

The input preprocessing is intended to form a standardized signal level.

All input and output signals can be processed simultaneously.

2.3. Clock and Crystal Specifications

Remark on using the crystal: External capacitors at each crystal pin to ground are required. The higher the capacitors, the lower the clock frequency results.

The nominal free running frequency should match the center of the tolerance range between 18.433 and 18.431 MHz as closely as possible.

2.4. Digital Control Output Pins

The static level of two output pins of the BSP 3505D (D_CTR_OUT0/1) is switchable between HIGH and LOW by means of the I²C-bus. This enables the controlling of external hardware controlled switches or other devices via I²C-bus (see section 4.4.11.)

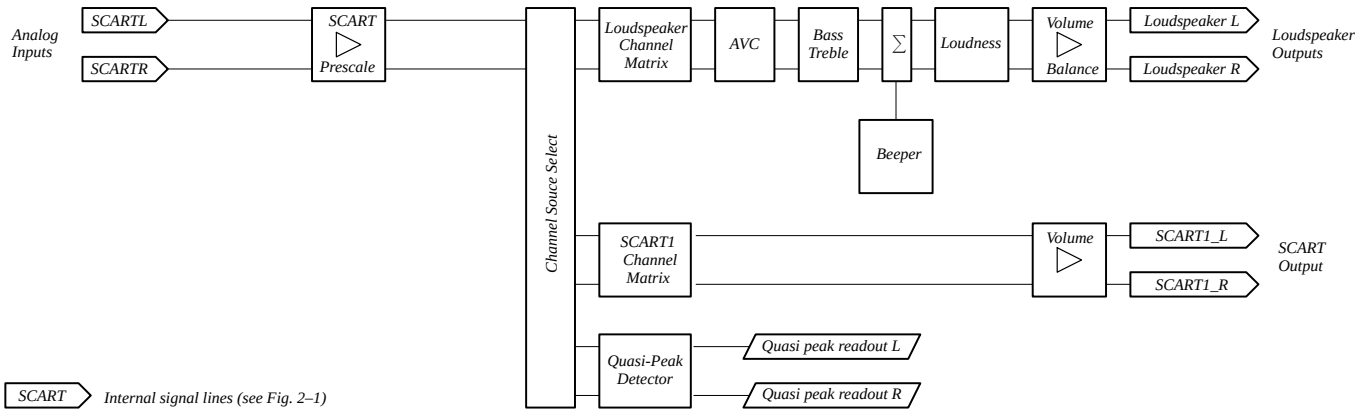


Fig. 2–3: Audio Baseband Processing (DSP-Firmware)

3. I²C Bus Interface: Device and Subaddresses

As a slave receiver, the BSP 3505D can be controlled via I²C bus. Access to internal memory locations is achieved by subaddressing. The DSP processor part has its own subaddressing register bank.

In order to allow for more BSP or MSP ICs to be connected to the control bus, an ADR_SEL pin has been implemented. With ADR_SEL pulled to high, low, or left open, the BSP 3505D responds to changed device addresses. Thus, three identical devices can be selected.

By means of the RESET bit in the CONTROL register, all devices with the same device address are reset.

The IC is selected by asserting a special device address in the address part of an I²C transmission. A device address pair is defined as a write address (80, 84, or 88_{hex}) and a read address (81, 85, or 89_{hex}). Writing is done by sending the device write address first, followed by the subaddress byte, two address bytes, and two data bytes. Reading is done by sending the device write address, followed by the subaddress byte and two address bytes. Without sending a stop condition, reading of the addressed data is completed by sending the device read address (81, 85, or 89_{hex}) and reading two bytes of data.

Refer to Fig. 3–1: I²C Bus Protocol and section 3.2. Proposal for BSP 3505D I²C Telegrams.

Due to the internal architecture of the BSP 3505D the IC cannot react immediately to an I²C request. The typical response time is about 0.3 ms for the DSP processor part. If the receiver (BSP) can't receive another complete byte of data until it has performed some other function; for example, servicing an internal interrupt, it can hold the clock line I²C_CL LOW to force the transmitter into a wait state. The positions within a transmission where this may happen are indicated by 'Wait' in section 3.1. The maximum Wait-period of the BSP during normal operation mode is less than 1 ms.

I²C-Bus conditions caused by BSP hardware problems: In case of any internal error, the BSPs wait-period is extended to 1.8 ms. Afterwards, the BSP does not acknowledge (NAK) the device address. The data line will be left HIGH by the BSP and the clock line will be released. The master can then generate a STOP condition to abort the transfer.

By means of NAK, the master is able to recognize the error state and to reset the IC via I²C-Bus. While transmitting the reset protocol (s. 5.2.4.) to 'CONTROL', the master must ignore the not acknowledge bits (NAK) of the BSP.

A general timing diagram of the I²C Bus is shown in Fig. 3–2.

Table 3–1: I²C Bus Device Addresses

ADR_SEL	Low		High		Left Open	
Mode	**Write**	**Read**	**Write**	**Read**	**Write**	**Read**
BSP device address	80_{hex}	81_{hex}	84_{hex}	85_{hex}	88_{hex}	89_{hex}

Table 3–2: I²C Bus Subaddresses

Name	Binary Value	Hex Value	Mode	Function
CONTROL	0000 0000	00	Write	software reset
TEST	0000 0001	01	Write	only for internal use
WR_DSP	0001 0010	12	Write	write address DSP
RD_DSP	0001 0011	13	Write	read address DSP

Table 3–3: Control Register (Subaddress: 00_{hex})

Name	Subaddress	MSB	14	13..1	LSB
CONTROL	00_{hex}	1 : RESET 0 : normal	0	0	0

3.1. Protocol Description

Write to DSP

S	write device address	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	data-byte high	ACK	data-byte low	ACK	P

Read from DSP

S	write device address	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	S	read device address	Wait	ACK	data-byte high	ACK	data-byte low	NAK	P

Write to Control or Test Registers

S	write device address	Wait	ACK	sub-addr	ACK	data-byte high	ACK	data-byte low	ACK	P

Note: S = I^2C-Bus Start Condition from master
P = I^2C-Bus Stop Condition from master
ACK = Acknowledge-Bit: LOW on I^2C_DA from slave (=BSP, gray) or master (=CCU, hatched)
NAK = Not Acknowledge-Bit: HIGH on I^2C_DA from master (=CCU, hatched) to indicate ‘End of Read’ or from BSP indicating internal error state
Wait = I^2C-Clock line held low by the slave (=BSP) while interrupt is serviced (<1.8 ms)

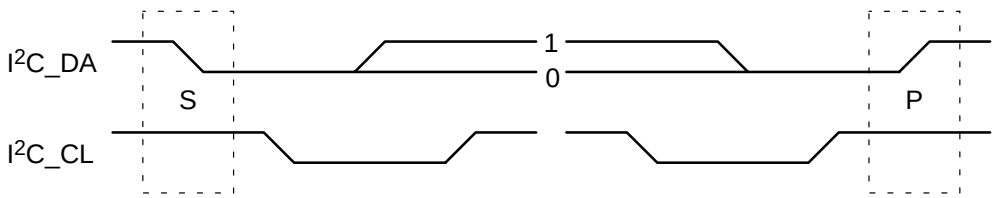


Fig. 3–1: I^2C bus protocol (MSB first; data must be stable while clock is high)

(Data: MSB first)

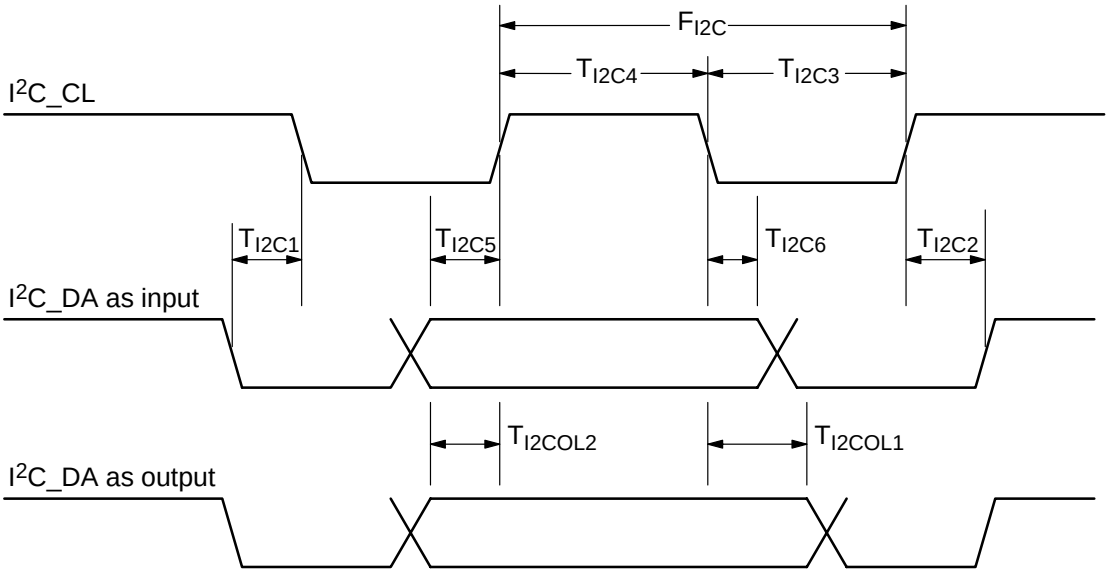


Fig. 3–2: I²C bus timing diagram

3.2. Proposal for BSP 3505D I²C Telegrams

3.2.1. Symbols

daw write device address
dar read device address
< Start Condition
> Stop Condition
aa Address Byte
dd Data Byte

3.2.2. Write Telegrams

`<daw 00 d0 00>` write to CONTROL register
`<daw 12 aa aa dd dd>` write data into DSP

3.2.3. Read Telegrams

`<daw 13 aa aa <dar dd dd>` read data from DSP

3.2.4. Examples

`<80 00 80 00>` RESET BSP statically
`<80 00 00 00>` clear RESET
`<80 12 00 08 02 20>` set loudspeaker channel source to SCART, stereo

3.3. Start Up Sequence: Power Up and I²C-Controlling

After power on or RESET (see Fig. 3–3), the IC is in an inactive state. The CCU has to transmit the required coefficient set for a given operation via the I²C bus. Initialization must start with the MODE Register.

The reset pin should not be >0.45*DVSUP (see recommended conditions) before the 5 Volt digital power supply (DVSUP) and the analog power supply (AVSUP) are >4.75 Volt **AND** the BSP clock is running. (Delay: 0.5 ms typ, 2 ms max)

This means, if the reset low–high edge starts with a delay of 2 ms after DVSUP and AVSUP >4,75 Volt, even under worst case conditions, the reset is ok.

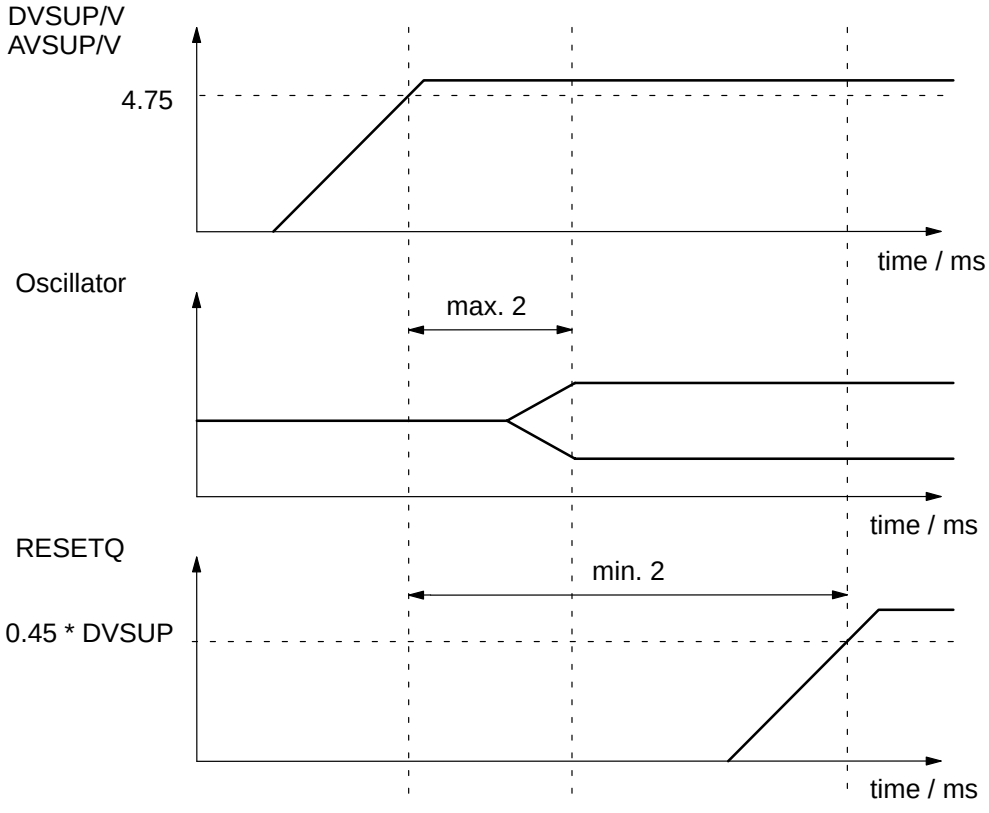


Fig. 3–3: Power-up sequence

Note: The reset should not reach high level before the oscillator has started. This requires a reset delay of >2 ms

4. Programming the BSP 3505D

4.1. Register ‘MODE_REG’

The register ‘MODE_REG’ contains the control bits determining the operation mode of the BSP 3505D;
Table 4–1 explains all bit positions.

Table 4–1: Control word ‘MODE_REG’: All bits are “0” after power-on-reset

Register	Protocol	Write Address (hex)	Function
MODE_REG	long	0083	mode register
Bit	**Function**	**Comment**	**Definition**
[0]	not used		must be 0
[1]	DCTR_TRI	Digital_Control_Output tristate	0 : active 1 : tristate
[2]	not used		must be 1
[3–4]	not used		must be 0
[5]	not used		must be 1
[6–9]	not used		must be 0
[10–15]	not used		must be 0

4.2. DSP Write Registers: Table and Addresses

Table 4–2: DSP Write Registers; Subaddress: 12_{hex}**;** if necessary these registers are readable as well.

DSP Write Register	Address	High/ Low	Adjustable Range, Operational Modes	Reset Mode
Volume loudspeaker channel	0000_{hex}	H	[+12 dB ... –114 dB, MUTE]	MUTE
Volume / Clipping Mode loudspeaker		L	1/8 dB Steps / Reduce Vol., Tone, Comprom.	00_{hex}
Balance loudspeaker channel [L/R]	0001_{hex}	H	[0..100 / 100 % and vv][–127..0 / 0 dB and vv]	100%/100%
Balance Mode loudspeaker		L	[Linear mode / logarithmic mode]	linear mode
Bass loudspeaker channel	0002_{hex}	H	[+12 dB ... –12 dB]	0 dB
Treble loudspeaker channel	0003_{hex}	H	[+12 dB ... –12 dB]	0 dB
Loudness loudspeaker channel	0004_{hex}	H	[0 dB ... +17 dB]	0 dB
Loudness Filter Characteristic		L	[NORMAL, SUPER_BASS]	NORMAL
Spatial effect strength loudspeaker ch.	0005_{hex}	H	[–100%...OFF...+100%]	OFF
Spatial effect mode/customize		L	[SBE, SBE+PSE]	SBE+PSE
Volume SCART1 channel	0007_{hex}	H	[00_{hex} ... $7F_{hex}$],[+12 dB ... –114 dB, MUTE]	00_{hex}
Volume / Mode SCART1 channel		L	[Linear mode / logarithmic mode]	linear mode
Loudspeaker channel source	0008_{hex}	H	[SCART]	FM/AM
Loudspeaker channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA
SCART1 channel source	$000A_{hex}$	H	[SCART]	FM/AM
SCART1 channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA
Quasi-peak detector source	$000C_{hex}$	H	[SCART]	FM/AM
Quasi-peak detector matrix		L	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA
Prescale SCART	$000D_{hex}$	H	[00_{hex} ... $7F_{hex}$]	00_{hex}
ACB Register (SCART Switching Facilities)	0013_{hex}	H/L	Bits [15..0]	00_{hex}
Beeper	0014_{hex}	H/L	[00_{hex} ... $7F_{hex}$]/[00_{hex} ... $7F_{hex}$]	0/0
Automatic Volume Correction	0029_{hex}	H	[off, on, decay time]	off

4.3. DSP Read Registers: Table and Addresses

Table 4–3: DSP Read Registers; Subaddress: 13_{hex}

DSP Read Register	Address	High/Low	Output Range	
Quasi peak readout left	0019_{hex}	H&L	[00_{hex} ... $7FFF_{hex}$]	16 bit two’s complement
Quasi peak readout right	$001A_{hex}$	H&L	[00_{hex} ... $7FFF_{hex}$]	16 bit two’s complement

4.4. DSP Write Registers: Functions and Values

Write registers are 16 bit wide, whereby the MSB is denoted bit [15]. Transmissions via I^2C bus have to take place in 16-bit words. Some of the defined 16-bit words are divided into low [7..0] and high [15..8] byte, or in an other manner, thus holding two different control entities. All write registers are readable. Unused parts of the 16-bit registers must be zero. Addresses not given in this table must not be written at any time!

4.4.1. Volume Loudspeaker Channel

Volume Loudspeaker	**0000_{hex}** **[15..4]**	
+12 dB	0111 1111 0000	$7F0_{hex}$
+11.875 dB	0111 1110 1110	$7EE_{hex}$
+0.125 dB	0111 0011 0010	732_{hex}
0 dB	0111 0011 0000	730_{hex}
–0.125 dB	0111 0010 1110	$72E_{hex}$
–113.875 dB	0000 0001 0010	012_{hex}
–114 dB	0000 0001 0000	010_{hex}
Mute	0000 0000 0000 RESET	000_{hex}
Fast Mute	1111 1111 1110	FFE_{hex}

The highest given positive 8-bit number ($7F_{hex}$) yields in a maximum possible gain of 12 dB. Decreasing the volume register by 1 LSB decreases the volume by 1 dB. Volume settings lower than the given minimum mute the output. With large scale input signals, positive volume settings may lead to signal clipping.

The BSP 3505D loudspeaker volume function is divided up in a digital and an analog section.

With Fast Mute, volume is reduced to mute position by digital volume only. Analog volume is not changed. This reduces any audible DC plops. Going back from Fast Mute should be done to the volume step before Fast Mute was activated.

Clipping Mode Loudspeaker	**0000_{hex}** **[3..0]**	
Reduce Volume	0000 RESET	0_{hex}
Reduce Tone Control	0001	1_{hex}
Compromise Mode	0010	2_{hex}

If the clipping mode is set to “Reduce Volume”, the following clipping procedure is used: To prevent severe clipping effects with bass or treble boosts, the internal volume is automatically limited to a level where, in combination with either bass or treble setting, the amplification does not exceed 12 dB.

If the clipping mode is “Reduce Tone Control”, the bass or treble value is reduced if amplification exceeds 12 dB.

If the clipping mode is “Compromise Mode”, the bass or treble value and volume are reduced half and half if amplification exceeds 12 dB.

Example:	**Vol.: +6 dB**	**Bass: +9 dB**	**Treble: +5 dB**
Red. Volume	3	9	5
Red. Tone Con.	6	6	5
Compromise	4.5	7.5	5

4.4.2. Balance Loudspeaker Channel

Positive balance settings reduce the left channel without affecting the right channel; negative settings reduce the right channel leaving the left channel unaffected. In linear mode, a step by 1 LSB decreases or increases the balance by about 0.8% (exact figure: 100/127). In logarithmic mode, a step by 1 LSB decreases or increases the balance by 1 dB.

Balance Mode Loudspeaker	**0001_{hex}**	**[3..0]**
linear	0000 RESET	0_{hex}
logarithmic	0001	1_{hex}

Linear Mode		
Balance Loudspeaker Channel [L/R]	**0001_{hex}**	**H**
Left muted, Right 100%	0111 1111	$7F_{hex}$
Left 0.8%, Right 100%	0111 1110	$7E_{hex}$
Left 99.2%, Right 100%	0000 0001	01_{hex}
Left 100%, Right 100%	0000 0000 RESET	00_{hex}
Left 100%, Right 99.2%	1111 1111	FF_{hex}
Left 100%, Right 0.8%	1000 0010	82_{hex}
Left 100%, Right muted	1000 0001	81_{hex}

Logarithmic Mode		
Balance Loudspeaker Channel [L/R]	**0001_{hex}**	**H**
Left –127 dB, Right 0 dB	0111 1111	$7F_{hex}$
Left –126 dB, Right 0 dB	0111 1110	$7E_{hex}$
Left –1 dB, Right 0 dB	0000 0001	01_{hex}
Left 0 dB, Right 0 dB	0000 0000 RESET	00_{hex}
Left 0 dB, Right –1 dB	1111 1111	FF_{hex}
Left 0 dB, Right –127 dB	1000 0001	81_{hex}
Left 0 dB, Right –128 dB	1000 0000	80_{hex}

4.4.3. Bass Loudspeaker Channel

Bass Loudspeaker	**0002_{hex}**	**H**
+20 dB	0111 1111	$7F_{hex}$
+18 dB	0111 1000	78_{hex}
+16 dB	0111 0000	70_{hex}
+14 dB	0110 1000	68_{hex}
+12 dB	0110 0000	60_{hex}
+11 dB	0101 1000	58_{hex}
+1 dB	0000 1000	08_{hex}
+1/8 dB	0000 0001	01_{hex}
0 dB	0000 0000 RESET	00_{hex}
–1/8 dB	1111 1111	FF_{hex}
–1 dB	1111 1000	$F8_{hex}$
–11 dB	1010 1000	$A8_{hex}$
–12 dB	1010 0000	$A0_{hex}$

With positive bass settings, internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass to a value that, in conjunction with volume, would result in an overall positive gain.

4.4.4. Treble Loudspeaker Channel

Treble Loudspeaker	0003_{hex}	H
+15 dB	0111 1000	78_{hex}
+14 dB	0111 0000	70_{hex}
+1 dB	0000 1000	08_{hex}
+1/8 dB	0000 0001	01_{hex}
0 dB	0000 0000 RESET	00_{hex}
–1/8 dB	1111 1111	FF_{hex}
–1 dB	1111 1000	$F8_{hex}$
–11 dB	1010 1000	$A8_{hex}$
–12 dB	1010 0000	$A0_{hex}$

With positive treble settings, internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set treble to a value that, in conjunction with volume, would result in an overall positive gain.

4.4.5. Loudness Loudspeaker Channel

Loudness Loudspeaker	0004_{hex}	H
+17 dB	0100 0100	44_{hex}
+16 dB	0100 0000	40_{hex}
+1 dB	0000 0100	04_{hex}
0 dB	0000 0000 RESET	00_{hex}

Mode Loudness Loudspeaker	0004_{hex}	L
Normal (constant volume at 1 kHz)	0000 0000 RESET	00_{hex}
Super Bass (constant volume at 2 kHz)	0000 0100	04_{hex}

Loudness increases the volume of low and high frequency signals, while keeping the amplitude of the 1 kHz reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness to a value that, in conjunction with volume, would result in an overall positive gain.

By means of ‘Mode Loudness’, the corner frequency for bass amplification can be set to two different values. In Super Bass mode, the corner frequency is shifted up. The point of constant volume is shifted from 1 kHz to 2 kHz.

4.4.6. Spatial Effects Loudspeaker Channel

Spatial Effect Strength Loudspeaker	**0005_{hex}**	**H**
Enlargement 100%	0111 1111	$7F_{hex}$
Enlargement 50%	0011 1111	$3F_{hex}$
Enlargement 1.5%	0000 0001	01_{hex}
Effect off	0000 0000 RESET	00_{hex}
Reduction 1.5%	1111 1111	FF_{hex}
Reduction 50%	1100 0000	$C0_{hex}$
Reduction 100%	1000 0000	80_{hex}

Spatial Effect Mode Loudspeaker	**0005_{hex}**	**[7..4]**
Stereo Basewidth Enlargement (SBE) and Pseudo Stereo Effect (PSE). (Mode A)	0000 RESET 0000	0_{hex} 0_{hex}
Stereo Basewidth Enlargement (SBE) only. (Mode B)	0010	2_{hex}

Spatial Effect Customize Coefficient Loudspeaker	**0005_{hex}**	**[3..0]**
max high pass gain	0000 RESET	0_{hex}
2/3 high pass gain	0010	2_{hex}
1/3 high pass gain	0100	4_{hex}
min high pass gain	0110	6_{hex}
automatic	1000	8_{hex}

There are several spatial effect modes available:

Mode A (low byte = 00_{hex}) is compatible to the formerly used spatial effect. Here, the kind of spatial effect depends on the source mode. If the incoming signal is in mono mode, Pseudo Stereo Effect is active; for stereo signals, Pseudo Stereo Effect and Stereo Basewidth Enlargement is effective. The strength of the effect is controllable by the upper byte. A negative value reduces the stereo image. A rather strong spatial effect is recommended for small TV sets where loudspeaker spacing is rather close. For large screen TV sets, a more moderate spatial effect is recommended. In mode A, even in case of stereo input signals, Pseudo Stereo Effect is active, which reduces the center image.

In Mode B, only Stereo Basewidth Enlargement is effective. For mono input signals, the Pseudo Stereo Effect has to be switched on.

It is worth mentioning, that all spatial effects affect amplitude and phase response. With the lower 4 bits, the frequency response can be customized. A value of 0000_{bin} yields a flat response for center signals (L = R) but a high pass function of L or R only signals. A value of 0110_{bin} has a flat response for L or R only signals but a lowpass function for center signals. By using 1000_{bin}, the frequency response is automatically adapted to the sound material by choosing an optimal high pass gain.

4.4.7. Volume SCART1

Volume Mode SCART1	0007_{hex}	[3..0]
linear	0000 RESET	0_{hex}
logarithmic	0001	1_{hex}

Linear Mode		
Volume SCART1	**0007_{hex}**	**H**
OFF	0000 0000 RESET	00_{hex}
0 dB gain (digital full scale (FS) to 2 V_{RMS} output)	0100 0000	40_{hex}
+6 dB gain (–6 dBFS to 2 V_{RMS} output)	0111 1111	$7F_{hex}$

Logarithmic Mode		
Volume SCART1	**0007_{hex}**	**[15..4]**
+12 dB	0111 1111 0000	$7F0_{hex}$
+11.875 dB	0111 1110 1110	$7EE_{hex}$
+0.125 dB	0111 0011 0010	732_{hex}
0 dB	0111 0011 0000	730_{hex}
–0.125 dB	0111 0010 1110	$72E_{hex}$
–113.875 dB	0000 0001 0010	012_{hex}
–114 dB	0000 0001 0000	010_{hex}
Mute	0000 0000 0000 RESET	000_{hex}

4.4.8. Channel Source Modes

Loudspeaker Source	0008_{hex}	H
SCART1 Source	**$000A_{hex}$**	**H**
Quasi-Peak Detector Source	**$000C_{hex}$**	**H**
NONE (MSP3410: FM)	0000 0000 RESET	00_{hex}
NONE (MSP3410: NICAM)	0000 0001	01_{hex}
SCART	0000 0010	02_{hex}

4.4.9. Channel Matrix Modes

Loudspeaker Matrix	0008_{hex}	L
SCART1 Matrix	**$000A_{hex}$**	**L**
Quasi-Peak Detector Matrix	**$000C_{hex}$**	**L**
SOUNDA / LEFT	0000 0000 RESET	00_{hex}
SOUNDB / RIGHT	0001 0000	10_{hex}
STEREO	0010 0000	20_{hex}
MONO	0011 0000	30_{hex}

4.4.10. SCART Prescale

Volume Prescale SCART	$000D_{hex}$	H
OFF	0000 0000 RESET	00_{hex}
0 dB gain (2 V_{RMS} input to digital full scale)	0001 1001	19_{hex}
+14 dB gain (400 mV_{RMS} input to digital full scale)	0111 1111	$7F_{hex}$

4.4.11. Definition of Digital Control Output Pins

ACB Register	0013_{hex} [15..14]
D_CTR_OUT0 low (RESET) high	 x0 x1
D_CTR_OUT1 low (RESET) high	 0x 1x

4.4.12. Definition of SCART-Switching Facilities

ACB Register	0013_{hex} [13..0]
DSP IN Selection of Source: * SC1_IN_L/R MONO_IN SC2_IN_L/R Mute	 xx xx00 xx00 0000 xx xx01 xx00 0000 xx xx10 xx00 0000 xx xx11 xx10 0000
SC1_OUT_L/R Selection of Source: SC2_IN_L/R MONO_IN SCART1 via D/A SC1_IN_L/R Mute	 xx 01xx x0x0 0000 xx 10xx x0x0 0000 xx 11xx x0x0 0000 xx 01xx x1x0 0000 xx 11xx x1x0 0000
* = RESET position, which becomes active at the time of the first write transmission on the control bus to the audio processing part (DSP). By writing to the ACB register first, the RESET state can be redefined. **Note:** After RESET, SC1_OUT_L/R is undefined!	

Note: If “MONO_IN” is selected at the DSP_IN selection, the channel matrix mode of the corresponding output channel(s) must be set to “sound A”.

4.4.13. Beeper

Beeper Volume	0014_{hex}	H
OFF	0000 0000 RESET	00_{hex}
Maximum Volume (full digital scale FDS)	0111 1111	$7F_{hex}$
Beeper Frequency	**0014_{hex}**	**L**
16 Hz (lowest)	0000 0001	01_{hex}
1 kHz	0100 0000	40_{hex}
4 kHz (highest)	1111 1111	FF_{hex}

A squarewave beeper can be added to the loudspeaker channel. The addition point is just before volume adjustment.

4.4.14. Automatic Volume Correction (AVC)

AVC	**on/off**	**0029_{hex}**	**[15.12]**
AVC	off and Reset of int. variables	0000 RESET	0_{hex}
AVC	on	1000	8_{hex}
AVC	**Decay Time**	**0029_{hex}**	**[11..8]**
8 sec 4 sec 2 sec 20 ms	(long) (middle) (short) (very short)	1000 0100 0010 0001	8_{hex} 4_{hex} 2_{hex} 1_{hex}

Different sound sources fairly often do not have the same volume level. Advertisement during movies, as well, usually has a different (higher) volume level than the movie itself. The Automatic Volume Correction (AVC) solves this problem and equalizes the volume levels.

The absolute value of the incoming signal is fed into a filter with 16 ms attack time and selectable decay time. The decay time must be adjusted as shown in the table above. This attack/decay filter block works similar to a peak hold function. The volume correction value with its quasi continuous step width is calculated using the attack/decay filter output.

The Automatic Volume Correction works with an internal reference level of –18 dBFS. This means, input signals with a volume level of –18 dBFS will not be affected by the AVC. If the input signals vary in a range of –24 dB to 0 dB, the AVC compensates this.

Example: A static input signal of 1 kHz on Scart has an output level as shown in the table below.

Scart Input 0 dbr = 2 Vrms	**Volume Correction**	**Main Output 0 dBr = 1.4 Vrms**
0 dBr	–18 dB	–18 dBr
–6 dBr	–12 dB	–18 dBr
–12 dBr	–6 dB	–18 dBr
–18 dBr	–0 dB	–18 dBr
–24 dBr	+ 6 dB	–18 dBr
–30 dBr	+ 6 dB	–24 dBr
Loudspeaker Volume = 73_{hex} = 0 dBFS Scart Prescale = 20_{hex} i.e. 2.0 Vrms = 0 dBFS		

To reset the internal variables, the AVC should be switched off and on during any channel or source change. For standard applications, the recommended decay time is 4 sec.

Note: AVC should not be used in any Dolby Prologic mode, except PANORAMA, where no other than the loudspeaker output is active.

4.5. DSP Read Registers: Functions and Values

All readable registers are 16-bit wide. Transmissions via I^2C bus have to take place in 16-bit words. Single data entries are 8 bit. Some of the defined 16-bit words are divided into low and high byte, thus holding two different control entities.

These registers are not writeable.

4.5.1. Quasi-Peak Detector

Quasi-Peak Readout Left	**0019_{hex}** **H+L**
Quasi-Peak Readout Right	**$001A_{hex}$** **H+L**
Quasi peak readout	[0_{hex} ... $7FFF_{hex}$] values are 16 bit two's complement

The quasi peak readout register can be used to read out the quasi peak level of any input source, in order to adjust all inputs to the same normal listening level. The refresh rate is 32 kHz. The feature is based on a filter time constant:

attack-time: 1.3 ms
decay-time: 37 ms

4.5.2. BSP Hardware Version Code

Hardware Version	**$001E_{hex}$ H**
Hardware Version	[00_{hex} ... FF_{hex}]
BSP 3505D – **A**2	01_{hex}

A change in the hardware version code defines hardware optimizations that may have influence on the chip's behavior. The readout of this register is identical to the hardware version code in the chip's imprint.

4.5.3. BSP Major Revision Code

Major Revision	**$001E_{hex}$ L**
BSP 3505**D**	04_{hex}

4.5.4. BSP Product Code

Product	**$001F_{hex}$ H**
BSP 35**05**D	05_{hex}

4.5.5. BSP ROM Version Code

ROM Version	**$001F_{hex}$ L**
Major software revision	[00_{hex} ... FF_{hex}]
BSP 3505D – A**2**	02_{hex}

A change in the ROM version code defines internal software optimizations, that may have influence on the chip's behavior, e.g. new features may have been included. While a software change is intended to create no compatibility problems, customers that want to use the new functions can identify new BSP 3505D versions according to this number.

5. Specifications

5.1. Outline Dimensions

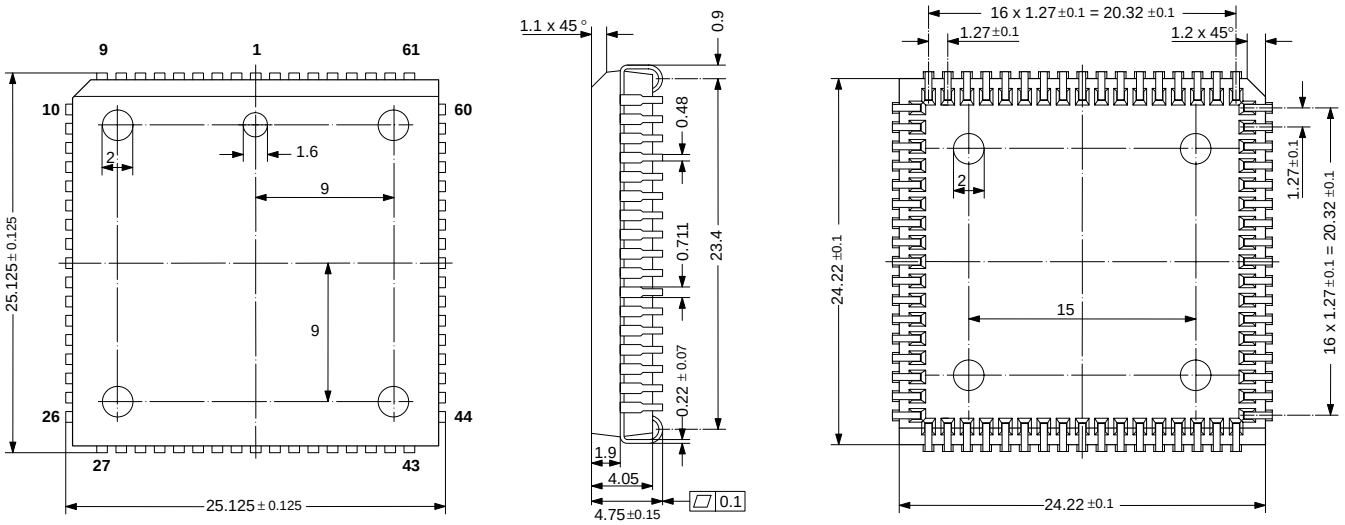


Fig. 5–1:
68-Pin Plastic Leaded Chip Carrier Package
(PLCC68)
Weight approximately 4.8 g
Dimensions in mm

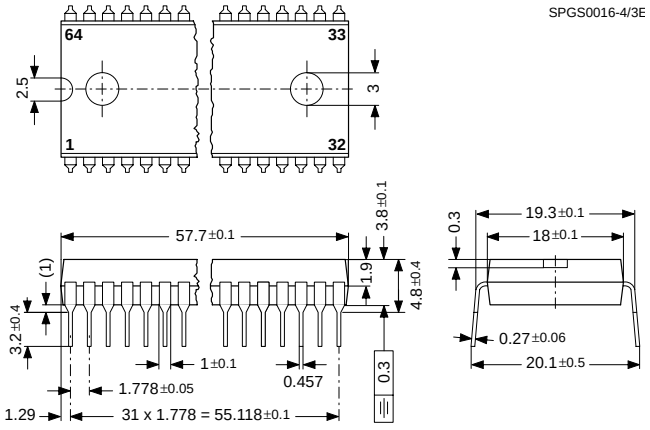


Fig. 5–2:
64-Pin Plastic Shrink Dual Inline Package
(PSDIP64)
Weight approximately 9.0 g
Dimensions in mm

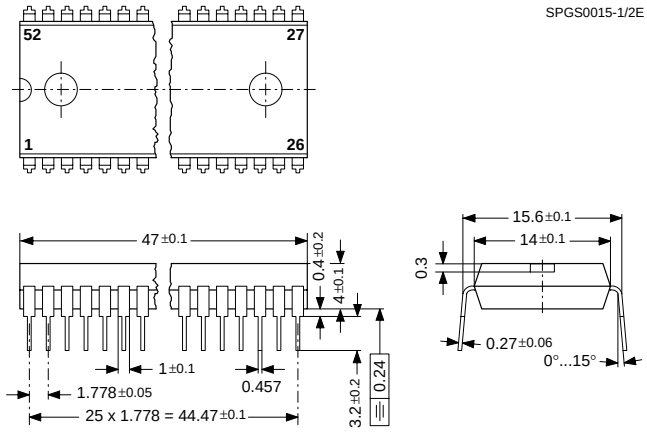


Fig. 5–3:
52-Pin Plastic Shrink Dual In Line Package
(PSDIP52)
Weight approximately 5.5 g
Dimensions in mm

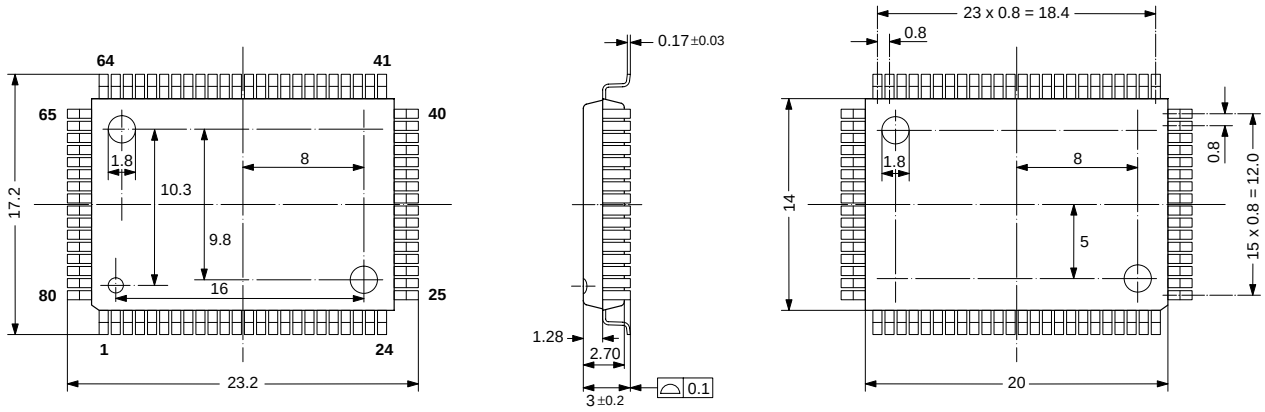


Fig. 5–4:
80-Pin Plastic Quad Flat Package
(PQFP80)
Weight approximately 1.6 g
Dimensions in mm

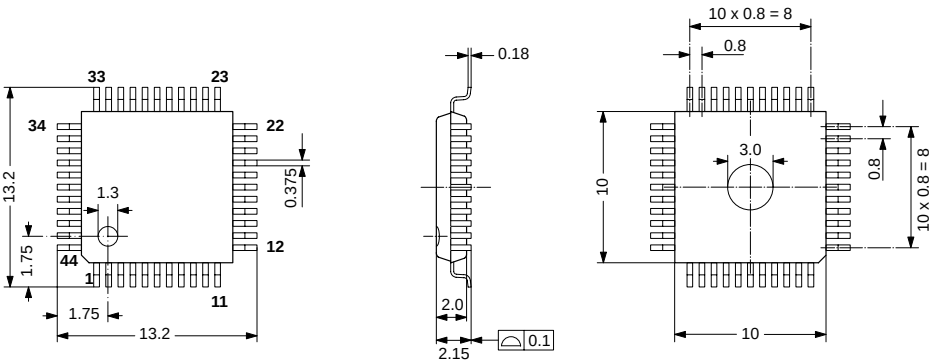


Fig. 5–5:
44-Pin Plastic Quad Flat Package
(PQFP44)
Weight approx. 0.4 g
Dimensions in mm

5.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
DVSS: if not used, connect to DVSS

X = obligatory; connect as described in circuit diagram
AHVSS: connect to AHVSS

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin	PQFP 44-pin				
1	16	14	9	–	TP	OUT	LV	Test pin
2	–	–	–	–	NC		LV	Not connected
3	15	13	8	–	TP	OUT	LV	Test pin
4	14	12	7	17	TP	IN	LV	Test pin
5	13	11	6	16	TP	OUT	LV	Test pin
6	12	10	5	15	TP	IN/OUT	LV	Test pin
7	11	9	4	14	TP	IN/OUT	LV	Test pin
8	10	8	3	13	I^2C_DA	IN/OUT	X	I^2C data
9	9	7	2	12	I^2C_CL	IN/OUT	X	I^2C clock
10	8	–	1	–	NC		LV	Not connected
11	7	6	80	11	STANDBYQ	IN	X	Standby (low-active)
12	6	5	79	10	ADR_SEL	IN	X	I^2C Bus address select
13	5	4	78	9	D_CTR_OUT0	OUT	LV	Digital control output 0
14	4	3	77	8	D_CTR_OUT1	OUT	LV	Digital control output 1
15	3	–	76	–	NC		LV	Not connected
16	2	–	75	–	NC		LV	Not connected
17	–	–	–	–	NC		LV	Not connected
18	1	2	74	–	NC		LV	Not connected
19	64	1	73	7	TP		LV	Test pin
20	63	52	72	6	XTAL_OUT	OUT	X	Crystal oscillator
21	62	51	71	5	XTAL_IN	IN	X	Crystal oscillator
22	61	50	70	4	TESTEN	IN	X	Test pin
23	60	49	69	–	NC		LV	Not connected
24	59	48	68	3	TP	IN	LV	Test pin
25	58	47	67	2	TP	IN	LV	Test pin
26	57	46	66	1	AVSUP		X	Analog power supply +5 V
–	–	–	65	–	AVSUP		X	Analog power supply +5 V
–	–	–	64	–	NC		LV	Not connected
–	–	–	63	–	NC		LV	Not connected

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin	PQFP 44-pin				
27	56	45	62	44	AVSS		X	Analog ground
–	–	–	61	–	AVSS		X	Analog ground
28	55	44	60	43	MONO_IN	IN	LV	Mono input
–	–	–	59	–	NC		LV	Not connected
29	54	43	58	42	VREFTOP		X	Reference voltage
30	53	42	57	41	SC1_IN_R	IN	LV	Scart input 1 in, right
31	52	41	56	40	SC1_IN_L	IN	LV	Scart input 1 in, left
32	51	–	55	39	ASG1		AHVSS	Analog shield ground 1
33	50	40	54	38	SC2_IN_R	IN	LV	Scart input 2 in, right
34	49	39	53	37	SC2_IN_L	IN	LV	Scart input 2 in, left
35	48	–	52	–	TP		LV	Test Pin
36	47	38	51	–	NC		LV	Not connected
37	46	37	50	–	NC		LV	Not connected
38	45	–	49	–	NC		LV	Not connected
39	44	–	48	–	NC		LV	Not connected
40	43	–	47	–	NC		LV	Not connected
41	–	–	46	–	NC		LV	Not connected
42	42	36	45	36	AGNDC		X	Analog reference voltage high voltage part
43	41	35	44	35	AHVSS		X	Analog ground
–	–	–	43	–	AHVSS		X	Analog ground
–	–	–	42	–	NC		LV	Not connected
–	–	–	41	–	NC		LV	Not connected
44	40	34	40	34	CAPL_M		X	Volume capacitor MAIN
45	39	33	39	33	AHVSUP		X	Analog power supply 8.0 V
46	38	32	38	32	NC		LV	Not connected
47	37	31	37	31	SC1_OUT_L	OUT	LV	Scart output 1, left
48	36	30	36	30	SC1_OUT_R	OUT	LV	Scart output 1, right
49	35	29	35	29	VREF1		X	Reference ground 1 high voltage part
50	34	28	34	28	NC		LV	Not connected
51	33	27	33	–	NC		LV	Not connected
52	–	–	32	–	NC		LV	Not connected

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin	PQFP 44-pin				
53	32	–	31	–	NC		LV	Not connected
54	31	26	30	–	NC		LV	Not connected
55	30	–	29	–	NC		LV	Not connected
56	29	25	28	27	DACM_L	OUT	LV	Loudspeaker out, left
57	28	24	27	26	DACM_R	OUT	LV	Loudspeaker out, right
58	27	23	26	25	VREF2		X	Reference ground 2 high voltage part
59	26	22	25	24	NC		LV	Not connected
60	25	21	24	23	NC		LV	Not connected
–	–	–	23	–	NC		LV	Not connected
–	–	–	22	–	NC		LV	Not connected
61	24	20	21	22	RESETQ	IN	X	Power-on-reset
62	23	–	20	–	NC		LV	Not connected
63	22	–	19	–	NC		LV	Not connected
64	21	19	18	21	NC		LV	Not connected
65	20	18	17	–	TP	IN	LV	Test pin
66	19	17	16	–	DVSS		X	Digital ground
–	–	–	15	–	DVSS		X	Digital ground
–	–	–	14	20	DVSS		X	Digital ground
67	18	16	13	19	DVSUP		X	Digital power supply +5 V
–	–	–	12	–	DVSUP		X	Digital power supply +5 V
–	–	–	11	–	DVSUP		X	Digital power supply +5 V
68	17	15	10	18	TP	OUT	LV	Test pin

5.3. Pin Configurations

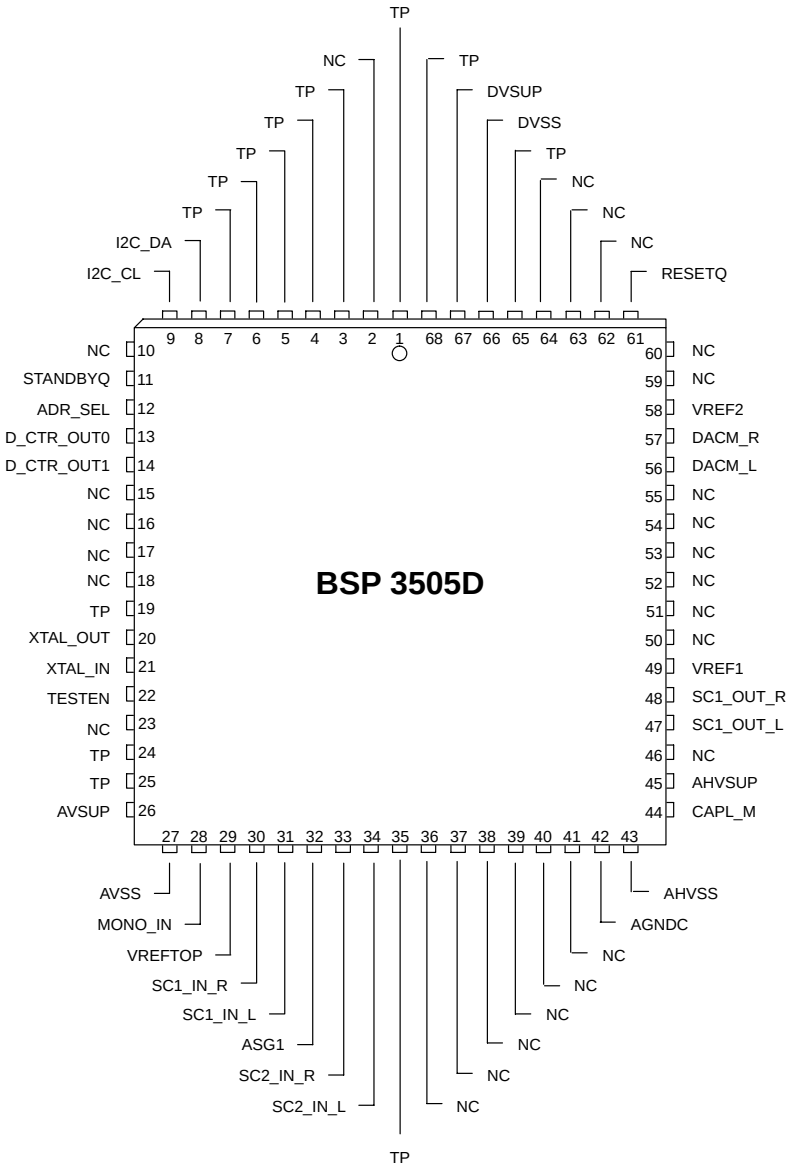


Fig. 5–6: 68-pin PLCC package

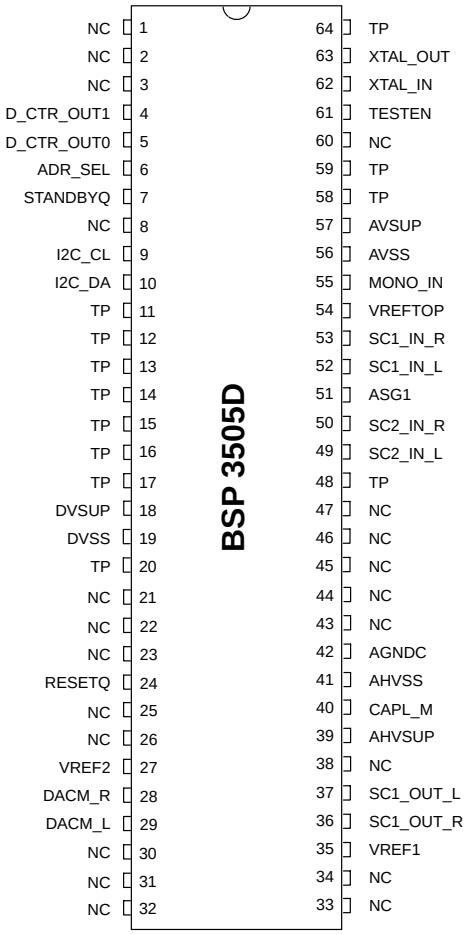


Fig. 5–7: 64-pin PSDIP package

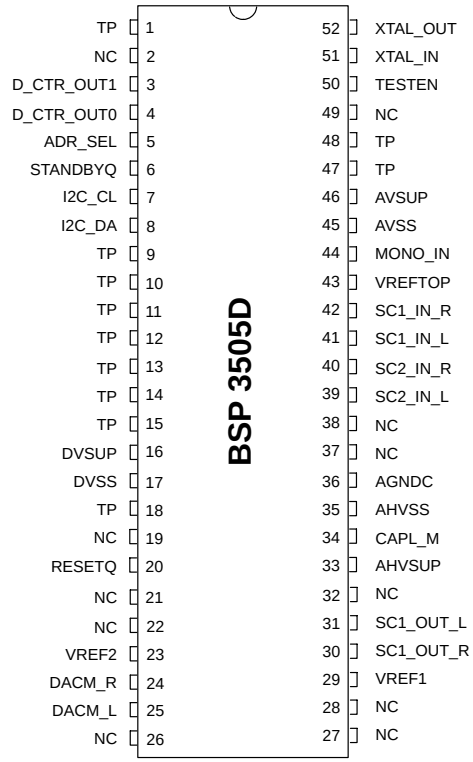


Fig. 5–8: 52-pin PSDIP package

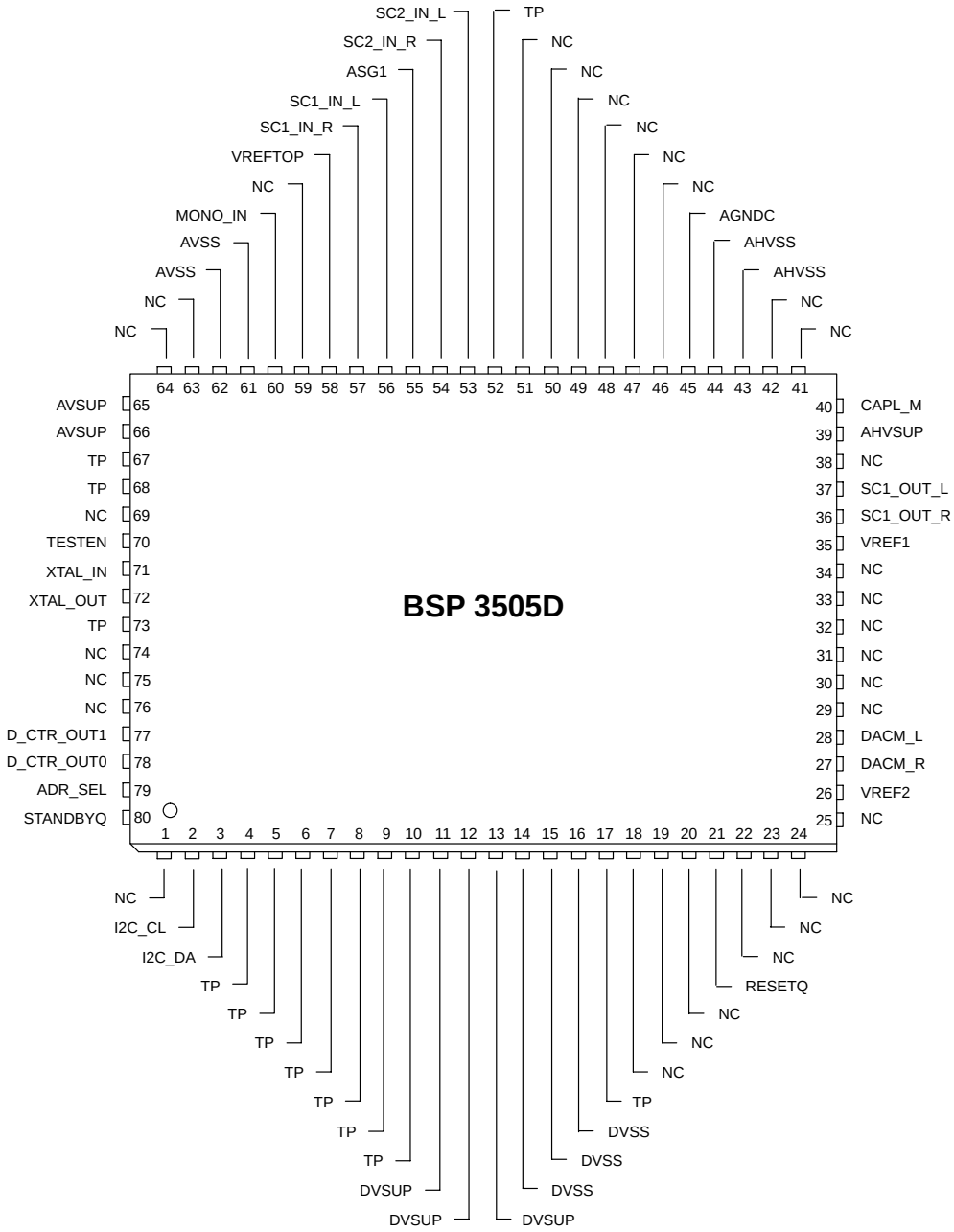


Fig. 5–9: 80-pin PQFP package

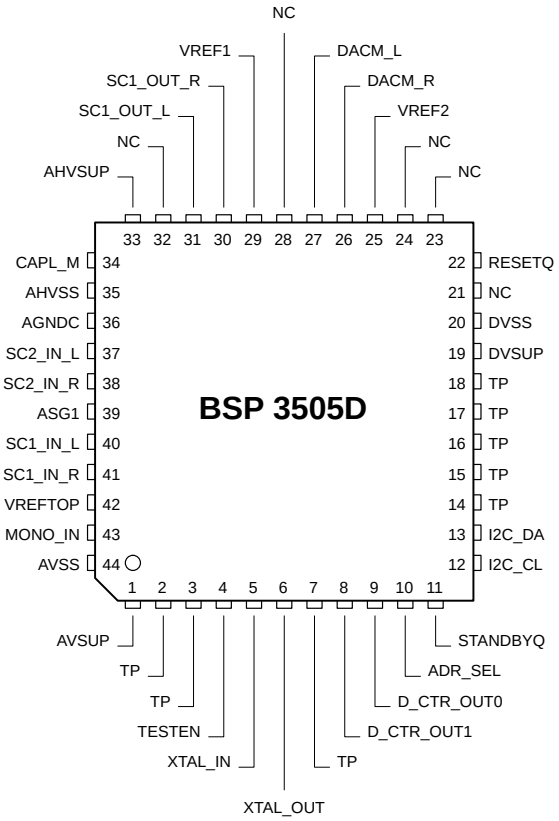


Fig. 5–10: 44-pin PQFP package

5.4. Pin Circuits (pin numbers refer to PLCC68 package)

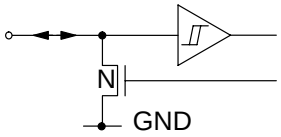


Fig. 5–11: Input/Output Pins 8 and 9 (I^2C_DA, I^2C_CL)

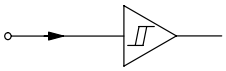


Fig. 5–12: Input Pins 11, 12, and 61 (STANDBYQ, ADR_SEL, RESETQ)

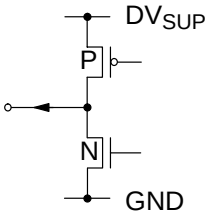


Fig. 5–13: Output Pins 13, and 14 (D_CTR_OUT0/1)

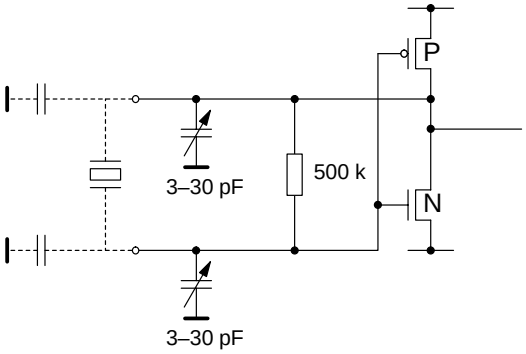


Fig. 5–14: Input/Output Pins 20 and 21 (XTALIN/OUT)

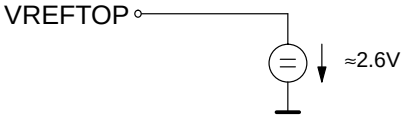


Fig. 5–15: Pin 29 (VREFTOP)

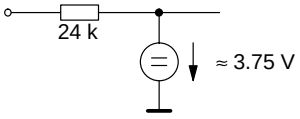


Fig. 5–16: Input Pin 28 (MONO_IN)

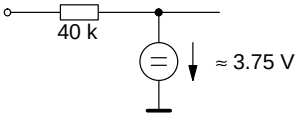


Fig. 5–17: Input Pins 30, 31, 33, and 34 (SC1–2_IN_L/R)

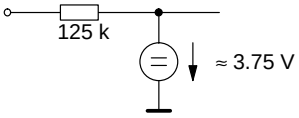


Fig. 5–18: Pin 42 (AGNDC)

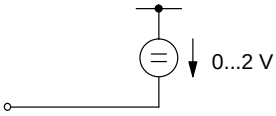


Fig. 5–19: Capacitor Pin 44 (CAPL_M)

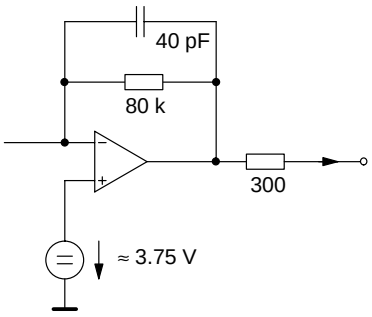


Fig. 5–20: Output Pins 47, 48 (SC1_OUT_L/R)

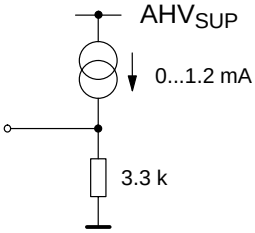


Fig. 5–21: Output Pins 56, 57 (DACM_L/R)

5.5. Electrical Characteristics

5.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	70[1)]	°C
T_S	Storage Temperature	–	–40	125	°C
V_{SUP1}	First Supply Voltage	AHVSUP	–0.3	9.0	V
V_{SUP2}	Second Supply Voltage	DVSUP	–0.3	6.0	V
V_{SUP3}	Third Supply Voltage	AVSUP	–0.3	6.0	V
dV_{SUP23}	Voltage between AVSUP and DVSUP	AVSUP, DVSUP	–0.5	0.5	V
P_{TOT}	Chip Power Dissipation PLCC68 without Heat Spreader PSDIP64 without Heat Spreader PSDIP52 without Heat Spreader PQFP44 without Heat Spreader	AHVSUP, DVSUP, AVSUP		 1200 1300 1200 960[1)]	mW
V_{Idig}	Input Voltage, all Digital Inputs		–0.3	V_{SUP2}+0.3	V
I_{Idig}	Input Current, all Digital Pins	–	–20	+20	mA[2)]
V_{Iana}	Input Voltage, all Analog Inputs	SCn_IN_s,[3)] MONO_IN	–0.3	V_{SUP1}+0.3	V
I_{Iana}	Input Current, all Analog Inputs	SCn_IN_s,[3)] MONO_IN	–5	+5	mA[2)]
I_{Oana}	Output Current, all SCART Outputs	SC1_OUT_s	[4)], [5)]	[4)], [5)]	
I_{Oana}	Output Current, all Analog Outputs except SCART Outputs	DACM_s[3)]	[4)]	[4)]	
I_{Cana}	Output Current, other pins connected to capacitors	CAPL_M AGNDC	[4)]	[4)]	

1) For PQFP44 package, max. ambient operating temperature is 65 °C.
2) positive value means current flowing into the circuit
3) “n” means “1” or “2”, “s” means “L” or “R”
4) The Analog Outputs are short circuit proof with respect to First Supply Voltage and Ground.
5) Total chip power dissipation must not exceed absolute maximum rating.

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

5.5.2. Recommended Operating Conditions

at T_A = 0 to 70 °C (65 °C for PQFP44)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{SUP1}	First Supply Voltage	AHVSUP	7.6	8.0	8.4	V
V_{SUP2}	Second Supply Voltage	DVSUP	4.75	5.0	5.25	V
V_{SUP3}	Third Supply Voltage	AVSUP	4.75	5.0	5.25	V
V_{REIL}	RESET Input High-Low and Low-High Transition Voltage	RESETQ	0.45		0.8	V_{SUP2}
t_{REIL}	RESET Low Time after DVSUP Stable and Oscillator Startup		5			µs
V_{DIGIL}	Digital Input Low Voltage	STANDBYQ, ADR_SEL, TESTEN			0.2	V_{SUP2}
V_{DIGIH}	Digital Input High Voltage		0.8			V_{SUP2}
t_{STBYQ1}	STANDBYQ Setup Time before Turn-off of Second Supply Voltage	STANDBYQ, DVSUP	1			µs
I^2C-Bus Recommendations						
V_{I2CIL}	I^2C-BUS Input Low Voltage	I^2C_CL, I^2C_DA			0.3	V_{SUP2}
V_{I2CIH}	I^2C-BUS Input High Voltage		0.6			V_{SUP2}
f_{I2C}	I^2C-BUS Frequency	I^2C_CL			1.0	MHz
t_{I2C1}	I^2C START Condition Setup Time	I^2C_CL, I^2C_DA	120			ns
t_{I2C2}	I^2C STOP Condition Setup Time		120			ns
t_{I2C3}	I^2C-Clock Low Pulse Time	I^2C_CL	500			ns
t_{I2C4}	I^2C-Clock High Pulse Time		500			ns
t_{I2C5}	I^2C-Data Setup Time Before Rising Edge of Clock	I^2C_CL, I^2C_DA	55			ns
t_{I2C6}	I^2C-Data Hold Time after Falling Edge of Clock		55			ns
Crystal Recommendations						
f_P	Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
f_{TOL}	Accuracy of Adjustment		–100		+100	ppm
D_{TEM}	Frequency Variation versus Temperature		–50		+50	ppm
R_R	Series Resistance			8	25	Ω
C_0	Shunt (Parallel) Capacitance			6.2	7.0	pF

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Load Capacitance Recommendations						
C_L	External Load Capacitance[1)]	XTAL_IN, XTAL_OUT	PSDIP PLCC	1.5 3.3		pF pF
Amplitude Recommendation for Operation with External Clock Input (C_{load} after reset = 22 pF)						
V_{XCA}	External Clock Amplitude	XTAL_IN	0.7			V_{pp}
Analog Input and Output Recommendations						
C_{AGNDC}	AGNDC-Filter-Capacitor	AGNDC	–20%	3.3		µF
	Ceramic Capacitor in Parallel		–20%	100		nF
C_{inSC}	DC-Decoupling Capacitor in front of SCART Inputs	SCn_IN_s[2)]	–20%	330	+20%	nF
V_{inSC}	SCART Input Level				2.0	V_{RMS}
V_{inMONO}	Input Level, Mono Input	MONO_IN			2.0	V_{RMS}
R_{LSC}	SCART Load Resistance	SC1_OUT_s[2)]	10			kΩ
C_{LSC}	SCART Load Capacitance				6.0	nF
C_{VMA}	Main Volume Capacitor	CAPL_M		10		µF
C_{FMA}	Main Filter Capacitor	DACM_s[2)]	–10%	1	+10%	nF
Recommendations for Reference Voltage Pin						
$C_{VREFTOP}$	VREFTOP-Filter-Capacitor	VREFTOP	–20%	10		µF
	Ceramic Capacitor in Parallel		–20%	100		nF

1) External capacitors at each crystal pin to ground are required. The higher the capacitors, the lower the clock frequency results. The nominal free running frequency should match 18.432 MHz as closely as possible. Due to different layouts of customer PCBs, the matching capacitor size should be defined in the application. The suggested values (1.5 pF/3.3 pF) are figures based on experience with various PCB layouts.

2) “n” means “1” or “2”, “s” means “L” or “R”

5.5.3. Characteristics

at T_A = 0 to 70 °C (65 °C for PQFP44), f_{CLOCK} = 18.432 MHz,
V_{SUP1} = 7.6 to 8.4 V, V_{SUP2} = 4.75 to 5.25 V for min./max. values
at T_A = 60 °C, f_{CLOCK} = 18.432 MHz, V_{SUP1} = 8 V, V_{SUP2} = 5 V for typical values, T_J = Junction Temperature
MAIN (M) = Loudspeaker Channel, AUX (A) = Headphone Channel

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
f_{CLOCK}	Clock Input Frequency	XTAL_IN		18.432		MHz	
D_{CLOCK}	Clock High to Low Ratio		45		55	%	
t_{JITTER}	Clock Jitter (Verification not provided in Production test)				50	ps	
V_{xtalDC}	DC-Voltage Oscillator			2.5		V	
$t_{Startup}$	Oscillator Startup Time at VDD Slew-rate of 1 V/1 µs	XTAL_IN, XTAL_OUT		0.4	2	ms	
I_{SUP1A}	First Supply Current (active) Analog Volume for Main and Aux at 0dB Analog Volume for Main and Aux at –30dB	AHVSUP	 9.6 6.3	 17.1 11.2	 24.6 16.1	 mA mA	
I_{SUP2A}	Second Supply Current (active)	DVSUP	86	95	102	mA	
I_{SUP3A}	Third Supply Current (active)	AVSUP	15	25	35	mA	
I_{SUP1S}	First Supply Current (standby mode) at T_j = 27 °C	AHVSUP	3.5	5.6	7.7	mA	STANDBYQ = low
V_{I2COL}	I^2C-Data Output Low Voltage	I^2C_DA			0.4	V	I_{I2COL} = 3 mA
I_{I2COH}	I^2C-Data Output High Current				1.0	µA	V_{I2COH} = 5 V
t_{I2COL1}	I^2C-Data Output Hold Time after Falling Edge of Clock	I^2C_DA, I^2C_CL	15			ns	
t_{I2COL2}	I^2C-Data Output Setup Time before Rising Edge of Clock		100			ns	f_{I2C} = 1 MHz
Analog Ground							
V_{AGNDC0}	AGNDC Open Circuit Voltage	AGNDC	3.63	3.73	3.83	V	$R_{load} \geq 10$ MΩ
R_{outAGN}	AGNDC Output Resistance		70	125	180	kΩ	3 V ≤ V_{AGNDC} ≤ 4 V
Analog Input Resistance							
R_{inSC}	SCART Input Resistance from T_A = 0 to 70 °C	SCn_IN_s[1)]	25	40	58	kΩ	f_{signal} = 1 kHz, I = 0.05 mA
R_{inMONO}	MONO Input Resistance from T_A = 0 to 70 °C	MONO_IN	15	24	35	kΩ	f_{signal} = 1 kHz, I = 0.1 mA
Audio Analog-to-Digital-Converter							
V_{AICL}	Effective Analog Input Clipping Level for Analog-to-Digital-Conversion	SCn_IN_s,[1)] MONO_IN	2.00		2.25	V_{RMS}	f_{signal} = 1 kHz

1) “n” means “1”, or “2”; “s” means “L” or “R”

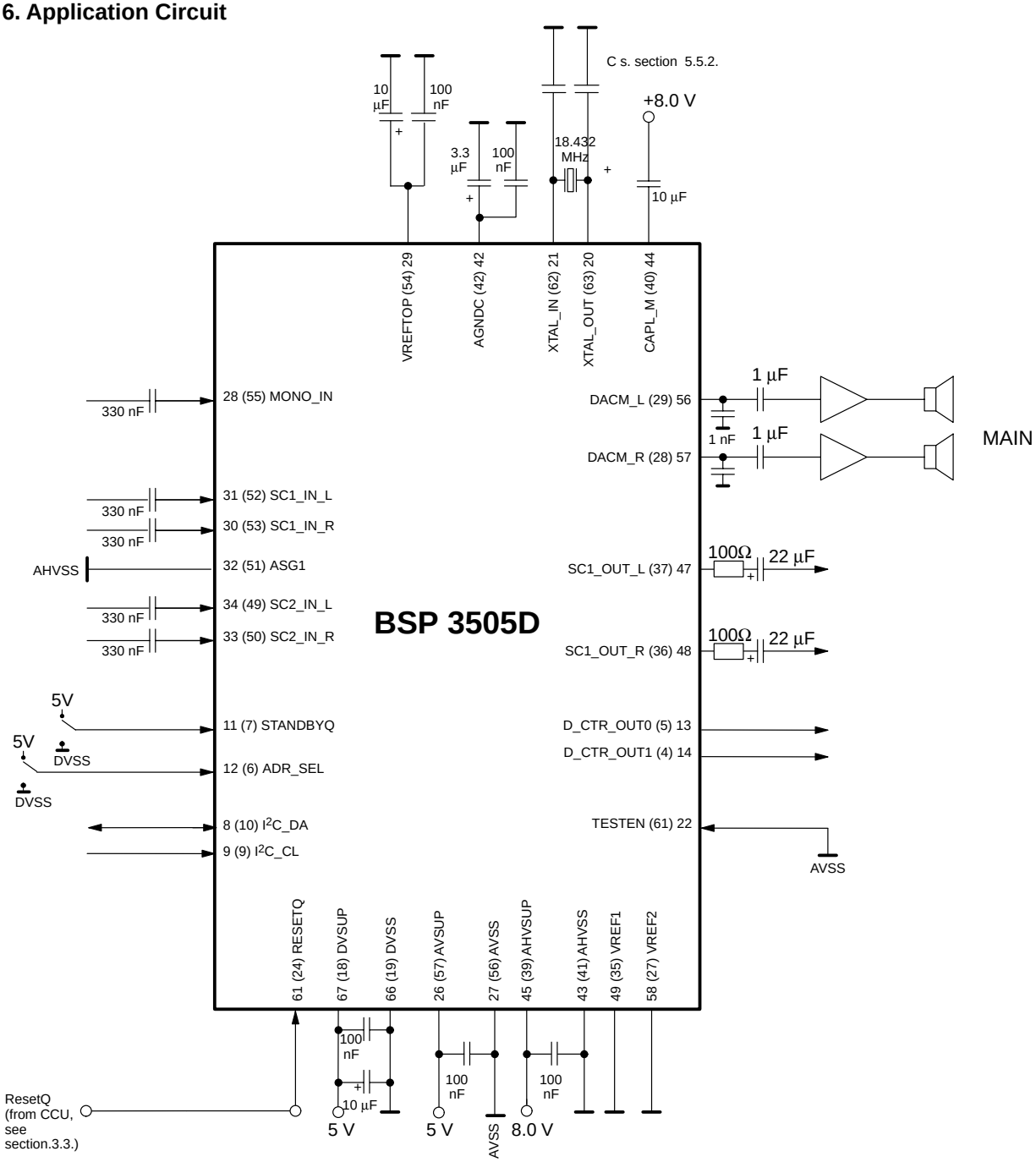
Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
SCART Outputs							
R_{outSC}	SCART Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C	SC1_OUT_s[1)]	200 200	330	460 500	Ω Ω	f_{signal} = 1 kHz, I = 0.1 mA
dV_{OUTSC}	Deviation of DC-Level at SCART Output from AGNDC Voltage		–70		+70	mV	
A_{SCtoSC}	Gain from Analog Input to SCART Output	SCn_IN_s[1)] MONO_IN → SC1_OUT_s[1)]	–1.0		+0.5	dB	f_{signal} = 1 kHz
$f_{rSCtoSC}$	Frequency Response from Analog Input to SCART Output bandwidth: 0 to 20000 Hz		–0.5		+0.5	dB	with resp. to 1 kHz
V_{outSC}	Effective Signal Level at SCART-Output during full-scale digital input signal from DSP	SC1_OUT_s[1)]	1.8	1.9	2.0	V_{RMS}	f_{signal} = 1 kHz
Main Outputs							
R_{outMA}	Main Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C	DACM_s[1)]	2.1 2.1	3.3	4.6 5.0	kΩ kΩ	f_{signal} = 1 kHz, I = 0.1 mA
$V_{outDCMA}$	DC-Level at Main-Output for Analog Volume at 0 dB for Analog Volume at –30 dB		1.8	2.04 61	2.28	V mV	
V_{outMA}	Effective Signal Level at Main-Output during full-scale digital input signal from DSP for Analog Volume at 0 dB		1.23	1.37	1.51	V_{RMS}	f_{signal} = 1 kHz
Analog Performance							
SNR	Signal-to-Noise Ratio						
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s[1)] → SC1_OUT_s[1)]	93	96		dB	Input Level = –20 dB, f_{sig} = 1 kHz, equally weighted 20 Hz ... 20 kHz
THD	Total Harmonic Distortion						
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s[1)] → SC1_OUT_s[1)]		0.01	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, equally weighted 20 Hz ... 20 kHz

1) “n” means “1” or “2”; “s” means “L” or “R”

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
XTALK	Crosstalk attenuation – PLCC68 – PSDIP64						Input Level = –3 dB, f_{sig} = 1 kHz, unused analog inputs connected to ground by Z < 1 kΩ
	between left and right channel within SCART Input/Output pair (L→R, R→L) SCn_IN[1] → SC1_OUT	 PLCC68 PSDIP64	 80 80			 dB dB	equally weighted 20 Hz ... 20 kHz
PSRR: rejection of noise on AHVSUP at 1 kHz							
	AGNDC	AGNDC		80		dB	
	From Analog Input to SCART Output	MONO_IN, SCn_IN_s[1] SC1_OUT_s[1]		70		dB	
$DC_{VREFTOP}$	DC voltage at VREFTOP	VREFTOP	2.4	2.6	2.7	V	

1) “n” means “1” or “2”; “s” means “L” or “R”

6. Application Circuit



Note: Pin numbers refer to the PLCC68 package, numbers in brackets refer to the PSDIP64 package.

Application Note:

All ground pins should be connected to one low-resistive ground plane.

All supply pins should be connected separately with short and low-resistive lines to the power supply.

Decoupling capacitors from DVSUP to DVSS, AVSUP to AVSS, and AHVSUP to AHVSS are recommended as close as possible to these pins. Decoupling of DVSUP and DVSS is most important. We recommend using more than one capacitor. By choosing different values, the frequency range of active decoupling can be extended. In our application boards we use: 220 pF, 470 pF, 1.5 nF, and 10 µF. The capacitor with lowest value should be placed nearest to the DVSUP and DVSS pins.

The ASG1 pin should be connected as closely as possible to the MSP to ground. If it is lead with the SC1 input-lines as shielding line, it should NOT be conneted to ground at the SCART connector.

7. Appendix A: BSP 3505D Version History

A2

First hardware release BSP 3505D

8. Data Sheet History

1. Preliminary Data Sheet: “BSP 3505D Baseband Sound Processor”, Oct. 21, 1998, 6251-481-1PD.
First release of the preliminary data sheet.

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