ARIZONA MICROTEK, INC.

AZ12000, AZ12001

Phase-Locked Loop Clock Generator

FEATURES

- PECL (AZ12000) or LVDS (AZ12001) Outputs
- Operating Range 3.0V to 5.5V
- Internal Crystal Oscillator Driver
- Internal Edge-Matching Phase/Frequency Detector
- Internal Charge-Pump and Integrator Amplifier
- Internal or External VCO
- Divide by 4, 8, 16, 32
- RF Bipolar Design for Low Phase Noise
- Available in a 4x4mm MLP Package

PACKAGE AVAILABILITY

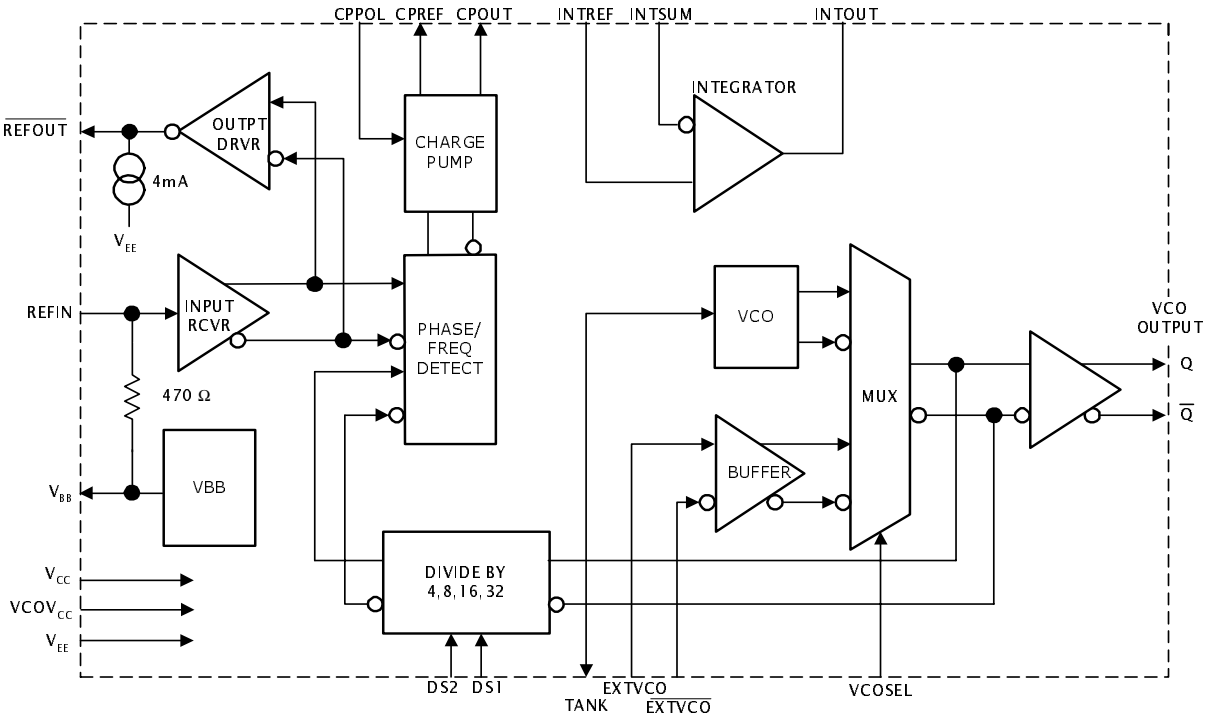
PACKAGE	PART NO.	MARKING	NOTES
MLP 24 (4x4)	AZ12000K	AZ12000 <Date Code>	1,2
MLP 24 (4x4)	AZ12001K	AZ12001 <Date Code>	1,2
DIE	AZ12000XP	N/A	3
DIE	AZ12001XP	N/A	3

1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
2 Date code format: "YY" for year followed by "WW" for week.
3 Waffle Pack

DESCRIPTION

The AZ12000/AZ12001 contains all of the functional elements necessary to implement a Phase-Locked Loop for clock multiplication at frequencies up to 800 MHz. A reference crystal oscillator driver operates at frequencies up to 200 MHz providing support for 4 times multiplication. The dynamic properties of the PLL are under the control of the user through selection of the desired external components.

BLOCK DIAGRAM



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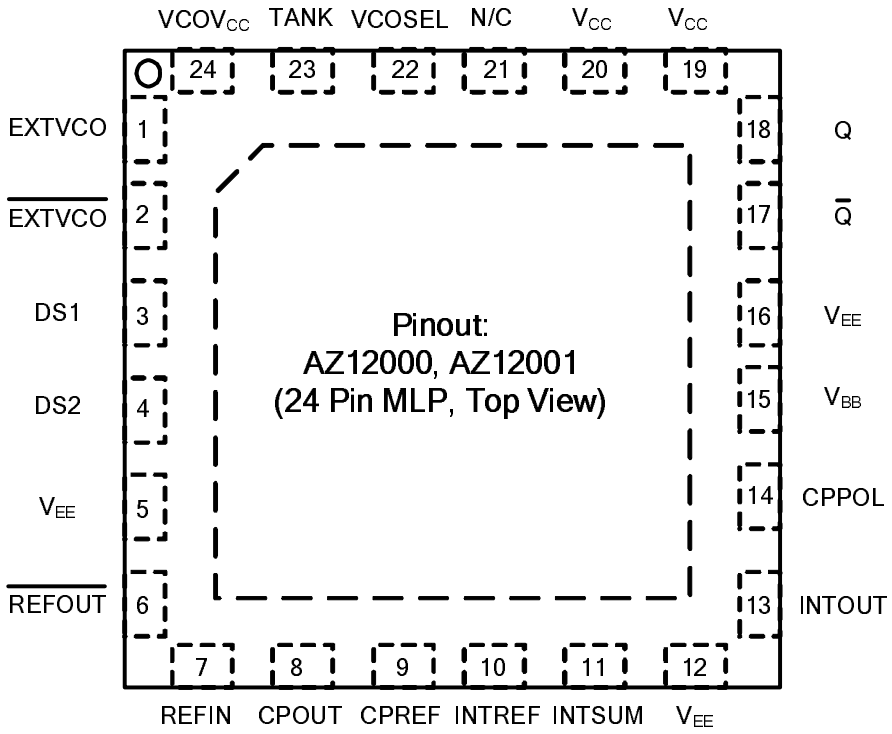
www.azmicrotek.com



Bottom Center pad may be left open or tied to V_{EE}.

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V_{CC}	Power Supply (V_{EE} = GND)	0 to +6.0	Vdc
V_I	Input Voltage (V_{EE} = GND)	0 to +6.0	Vdc
I_{OUT}	ECL/PECL Output Current — Continuous — Surge	40 80	mA
T_A	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

AZ12000 FUNCTIONAL PIN DESCRIPTIONS

Pin No	Pin Name	Functional Description	Logic Level
	REFIN	**Reference Crystal Resonator Input** This pin includes an on-chip 470 Ω pull down resistor to V_{BB}. The input from the resonator circuit should be AC coupled.	
	$\overline{\text{REFOUT}}$	**Crystal Resonator Output Drive** This pin is an inverted and amplified version of the signal on the REFIN pin. The gain from REFIN to $\overline{\text{REFOUT}}$ is approximately 20. The IC includes a 4 ma on-chip current source. If more current is needed, the $\overline{\text{REFOUT}}$ pin may be connected to V_{EE} through a resistor to provide up to 8 ma additional current.	ECL/PECL
	CPREF	**Charge Pump Reference Output** The pin voltage is nominally 1.2 volts below V_{CC}. If an external integrator is used, CPREF should be connected to the integrator reference input through a bias current cancellation network.	
	CPOUT	**Charge Pump Output** The charge pump output voltage is V(CPREF) ±0.3V during a phase correction pulse. When there is no correction pulse the output goes high impedance. If an external integrator is used, CPOUT should be connected to the input integrator resistor.	
	CPPOL	**Charge Pump Polarity** Logic LOW on this pin causes CPOUT to go low when the VCO frequency is too low, and go high when the VCO frequency is too high. Logic HIGH on this pin causes CPOUT to go low when the VCO frequency is too high, and go high when the VCO frequency is too low. This pin should be LOW when the internal VCO is used. If this pin is left open it is pulled to the HIGH condition.	CMOS/TTL compatible
	INTREF	**Integrator Reference Input** This pin should be connected to CPREF through a bias current cancellation network	
	INTSUM	**Integrator Summing Junction** This pin is the summing junction for the integrator amplifier	
	INTOUT	**Integrator Output**	
	VCOSEL	**Internal/External VCO Select** Logic HIGH on this pin enables the internal VCO. Logic LOW on this pin disables the internal VCO and allows use of the EXTVCO inputs. If this pin is left open it is pulled to the HIGH condition.	CMOS/TTL compatible
	TANK	**VCO Tank** The tank components connect between this pin and V_{CC}.	
	EXTVCO $\overline{\text{EXTVCO}}$	**External VCO Input** The external VCO input pins should be driven differentially for best performance.	ECL/PECL
	DS2 DS1	**Divide Select** VCO divide ratios are selected as shown: DS2 DS1 Ratio LOW LOW ÷4 LOW HIGH ÷8 HIGH LOW ÷16 HIGH HIGH ÷32 If the pins are left open they are pulled to the HIGH condition.	CMOS/TTL compatible
	Q $\overline{\text{Q}}$	**Clock Output** These pins are the main (multiplied) clock output.	ECL/PECL
	N/C	**No Connect** This pin is used during factory test. It mist be left open.	
	V_{BB}	**Reference Voltage Output** This pin is used to bias the REFIN signal. It must be bypassed externally to the VEE pins with a 0.01 µF capacitor.	
	V_{CC}	**Positive Supply** +3.0 to +5.5 V for PECL mode, Ground for ECL mode.	
	$VCOV_{CC}$	**VCO Positive Supply** +3.0 to +5.5 V for PECL mode, Ground for ECL mode.	
	V_{EE}	**Negative Supply** Ground for PECL mode, –3.0 to –5.5 V for ECL mode.	

AZ12001 FUNCTIONAL PIN DESCRIPTIONS

Pin No	Pin Name	Functional Description	Logic Level
	REFIN	**Reference Crystal Resonator Input** This pin includes an on-chip 470 Ω pull down resistor to V_{BB}. The input from the resonator circuit should be AC coupled.	
	$\overline{\text{REFOUT}}$	**Crystal Resonator Output Drive** This pin is an inverted and amplified version of the signal on the REFIN pin. The gain from REFIN to $\overline{\text{REFOUT}}$ is approximately 20. The IC includes a 4 ma on-chip current source. If more current is needed, the $\overline{\text{REFOUT}}$ pin may be connected to V_{EE} through a resistor to provide up to 8 ma additional current.	PECL
	CPREF	**Charge Pump Reference Output** The pin voltage is nominally 1.2 volts below V_{CC}. If an external integrator is used, CPREF should be connected to the integrator reference input through a bias current cancellation network.	
	CPOUT	**Charge Pump Output** The charge pump output voltage is V(CPREF) ±0.3V during a phase correction pulse. When there is no correction pulse the output goes high impedance. If an external integrator is used, CPOUT should be connected to the input integrator resistor.	
	CPPOL	**Charge Pump Polarity** Logic LOW on this pin causes CPOUT to go low when the VCO frequency is too low, and go high when the VCO frequency is too high. Logic HIGH on this pin causes CPOUT to go low when the VCO frequency is too high, and go high when the VCO frequency is too low. This pin should be LOW when the internal VCO is used. If this pin is left open it is pulled to the HIGH condition.	CMOS/TTL compatible
	INTREF	**Integrator Reference Input** This pin should be connected to CPREF through a bias current cancellation network	
	INTSUM	**Integrator Summing Junction** This pin is the summing junction for the integrator amplifier	
	INTOUT	**Integrator Output**	
	VCOSEL	**Internal/External VCO Select** Logic HIGH on this pin enables the internal VCO. Logic LOW on this pin disables the internal VCO and allows use of the EXTVCO inputs. If this pin is left open it is pulled to the HIGH condition.	CMOS/TTL compatible
	TANK	**VCO Tank** The tank components connect between this pin and V_{CC}.	
	EXTVCO $\overline{\text{EXTVCO}}$	**External VCO Input** The external VCO input pins should be driven differentially for best performance.	PECL
	DS2 DS1	**Divide Select** VCO divide ratios are selected as shown: DS2 DS1 Ratio LOW LOW ÷4 LOW HIGH ÷8 HIGH LOW ÷16 HIGH HIGH ÷32 If the pins are left open they are pulled to the HIGH condition.	CMOS/TTL Compatible
	Q $\overline{\text{Q}}$	**Clock Output** These pins are the main (multiplied) clock output.	LVDS
	N/C	**No Connect** This pin is used during factory test. It must be left open.	
	V_{BB}	**Reference Voltage Output** This pin is used to bias the REFIN signal. It must be bypassed externally to the VEE pins with a 0.01 µF capacitor.	
	V_{CC}	**Positive Supply** +3.0 to +5.5 V	
	$VCOV_{CC}$	**VCO Positive Supply** +3.0 to +5.5 V	
	V_{EE}	**Negative Supply** Ground	

AZ12000 (PECL OUTPUT) DC CHARACTERISTICS (V_{CC} = +3.0 to +5.5 V, V_{EE} = GND)

Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit
		Min	Max	Min	Max	Min	Typ	Max	Min	Max	
V_{BB}	Reference Voltage	V_{CC} -1.38	V_{CC} -1.26	V_{CC} -1.38	V_{CC} -1.26	V_{CC} -1.38	V_{CC} -1.31	V_{CC} -1.26	V_{CC} -1.38	V_{CC} -1.26	V
R_{PD}	REFIN Pull-Down resistor to V_{BB}						470				Ω
I_{CS}	$\overline{\text{REFOUT}}$ Current Source						4.0				ma
V_{HCTL}	High level integrator output					V_{CC} -1.0					V
V_{LCTL}	Low level integrator output							V_{EE} +0.5			V
V_{OH}	Output HIGH Voltage[1] Q $\overline{Q}$	V_{CC} -1085	V_{CC} -880	V_{CC} -1025	V_{CC} -880	V_{CC} -1025	V_{CC} -955	V_{CC} -880	V_{CC} -1025	V_{CC} -880	mV
V_{OL}	Output LOW Voltage[1] Q $\overline{Q}$	V_{CC} -1830	V_{CC} -1555	V_{CC} -1810	V_{CC} -1620	V_{CC} -1810	V_{CC} -1705	V_{CC} -1620	V_{CC} -1810	V_{CC} -1620	mV
V_{IH}	Input HIGH Voltage, PECL/ECL EXTVCO $\overline{\text{EXTVCO}}$	V_{CC} -1165	V_{CC} -880	V_{CC} -1165	V_{CC} -880	V_{CC} -1165		V_{CC} -880	V_{CC} -1165	V_{CC} -880	mV
V_{IL}	Input LOW Voltage, PECL/ECL EXTVCO $\overline{\text{EXTVCO}}$	V_{CC} -1810	V_{CC} -1475	V_{CC} -1810	V_{CC} -1475	V_{CC} -1810		V_{CC} -1475	V_{CC} -1810	V_{CC} -1475	mV
V_{IH}	Input HIGH Voltage, TTL/CMOS CPPOL VCOSEL DS2 DS1	V_{EE} +2.0		V_{EE} +2.0		V_{EE} +2.0			V_{EE} +2.0		V
V_{IL}	Input HIGH Voltage, TTL/CMOS CPPOL VCOSEL DS2 DS1		V_{EE} +0.8		V_{EE} +0.8			V_{EE} +0.8		V_{EE} +0.8	V
I_{CC} (I_{EE})	Power Supply Current		55		58		45	58		60	mA

1. Load is 50Ω to V_{CC}-2V

AZ12001 (LVDS OUTPUT) DC CHARACTERISTICS (V_{CC} = +3.0 to +5.5 V, V_{EE} = GND)

Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit
		Min	Max	Min	Max	Min	Typ	Max	Min	Max	
V_{BB}	Reference Voltage	V_{CC} -1.38	V_{CC} -1.26	V_{CC} -1.38	V_{CC} -1.26	V_{CC} -1.38	V_{CC} -1.31	V_{CC} -1.26	V_{CC} -1.38	V_{CC} -1.26	V
R_{PD}	REFIN Pull-Down resistor to V_{BB}						470				Ω
I_{CS}	$\overline{\text{REFOUT}}$ Current Source						4.0				ma
V_{HCTL}	High level integrator output					V_{CC} -1.0					V
V_{LCTL}	Low level integrator output							V_{EE} +0.5			V
V_{OH}	Output HIGH Voltage[1] Q $\overline{Q}$										mV
V_{OL}	Output LOW Voltage[1] Q $\overline{Q}$										mV
V_{IH}	Input HIGH Voltage, PECL/ECL EXTVCO $\overline{\text{EXTVCO}}$	V_{CC} -1165	V_{CC} -880	V_{CC} -1165	V_{CC} -880	V_{CC} -1165		V_{CC} -880	V_{CC} -1165	V_{CC} -880	mV
V_{IL}	Input LOW Voltage, PECL/ECL EXTVCO $\overline{\text{EXTVCO}}$	V_{CC} -1810	V_{CC} -1475	V_{CC} -1810	V_{CC} -1475	V_{CC} -1810		V_{CC} -1475	V_{CC} -1810	V_{CC} -1475	mV
V_{IH}	Input HIGH Voltage, TTL/CMOS CPPOL VCOSEL DS2 DS1	V_{EE} +2.0		V_{EE} +2.0		V_{EE} +2.0			V_{EE} +2.0		V
V_{IL}	Input HIGH Voltage, TTL/CMOS CPPOL VCOSEL DS2 DS1		V_{EE} +0.8		V_{EE} +0.8			V_{EE} +0.8		V_{EE} +0.8	V
I_{CC} (I_{EE})	Power Supply Current				60			60		60	mA

1. 100 Ω between outputs

AZ 12000 (PECL OUTPUT) AC CHARACTERISTICS (V_{CC} = +3.0 to +5.5 V, V_{EE} = GND)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
A_{V1}	Gain, REFIN to REFOUT					20					V/V
Z_O	Output Impedance, REFOUT					TBD					Ω
A_{PD}	Phase Detector Gain					20.3					radians/V
f_{VCO}	VCO frequency (Internal or External)						800				MHz
t_r / t_f	Output Rise & Fall Times (20% - 80%) Q $\overline{Q}$					120 120					ps

AZ12001 (LVDS OUTPUT) AC CHARACTERISTICS (V_{CC} = +3.0 to +5.5 V, V_{EE} = GND)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
A_{V1}	Gain, REFIN to REFOUT					20					V/V
Z_O	Output Impedance, REFOUT					TBD					Ω
A_{PD}	Phase Detector Gain					20.3					Radians/V
f_{VCO}	VCO frequency (Internal or External)						800				MHz
t_r / t_f	Output Rise & Fall Times (20% - 80%) Q $\overline{Q}$										ps

Internal Reference Oscillator

The PLL reference can be generated either with an internal oscillator or with an external source. In either case, the input is the REFIN pin. This should be AC coupled since the input is internally biased to V_{BB}. The REFOUT pin should be left open when an external reference is used.

The exact topology of the crystal circuit will vary based on the resonant mode of the crystal. The circuit shown is for a series resonant crystal. The AC gain between the REFIN and REFOUT pins is approximately 20. This value is sufficient to overcome crystal matching network losses without phase noise degradation caused by an excessive drive level. An internal current source on REFOUT eliminates the need for an external load resistor.

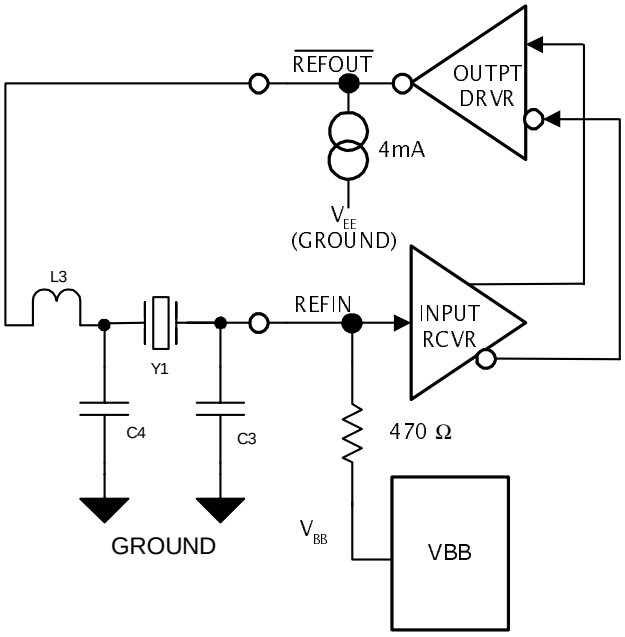


Figure 1 Reference Oscillator

Loop Filter Design

The combination of the phase detector, amplifier, VCO and divider form a second-order phase-locked loop. Proper selection of the loop components is important to obtain stable, low jitter operation.

The loop bandwidth (or natural frequency, ω_n) and damping factor (ζ) are the two major driving forces that define the loop's response to a disturbance. The value of ζ is typically 0.7 to ensure the fastest step response consistent with no ringing. However in many oscillator application ζ may be 3 or higher to provide further phase noise reduction. ω_n is chosen as a compromise between settling time, VCO jitter and reference feedthrough. These values can be computed by the following equations:

$$\omega_n = \frac{1}{N}\sqrt{\frac{K_\phi K_{VCO}}{\tau_1}}$$

$$\zeta = \frac{\tau_2 \omega_n}{2}$$

$$\tau_1 = R_1 C_1$$

$$\tau_2 = R_2 C_1$$

$K_\phi =$ Phase Detector Gain (20.3 radians/V)

$K_{VCO} =$ VCO Gain (radians/sec/volt)

$N =$ Frequency Divisor value (4,8, 16 or 32)

The component definitions are shown in the figure below. R3 should be equal to R1 to minimize integrator offsets.

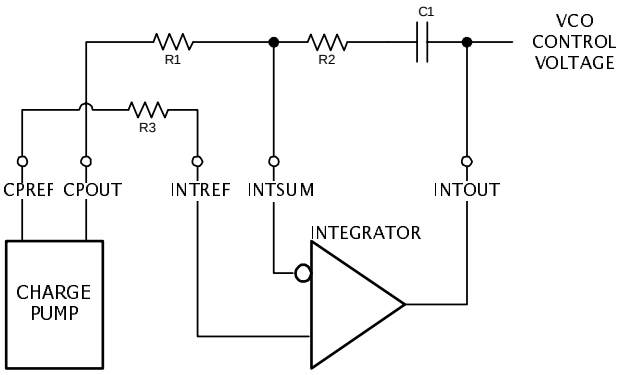


Figure 2 Charge Pump and Integrator

Internal VCO

The internal VCO is designed for reliable, low jitter operation up to 800 MHz. It operates as a single terminal negative impedance type circuit.

The tank circuit should have a minimum Q of 12 for reliable operation. The series combination of CV and C1 resonate with L1 to set the operating frequency. The VCO control voltage is isolated through an inductor or resistor and changes the varactor capacitance based on that control voltage. Note that the CPPOL pin should be tied high for internal VCO operation since the tank frequency decreases with increasing control voltage.

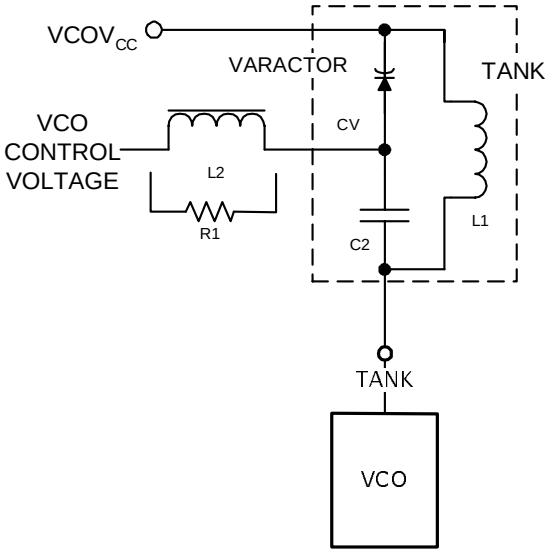


Figure 3 Internal VCO with Tank

External VCO

When VCOSEL is high, the internal VCO is disabled and the EXTVCO, $\overline{\text{EXTVCO}}$ pair is enabled. That input pair is sine wave and PECL compatible.

The CPPOL pin sets the frequency slope polarity based on the operation of the external VCO. When CPPOL is low, the charge pump generates pulses for an integrator and loop filter assuming the VCO frequency goes lower as the integrator output voltage increases. When CPPOL is high, pulses are generated for a VCO in which the frequency goes higher as the integrator output voltage increases.

Application Circuit

A typical application circuit is shown in Figure 4. This drawing shows use of the internal reference oscillator and internal VCO.

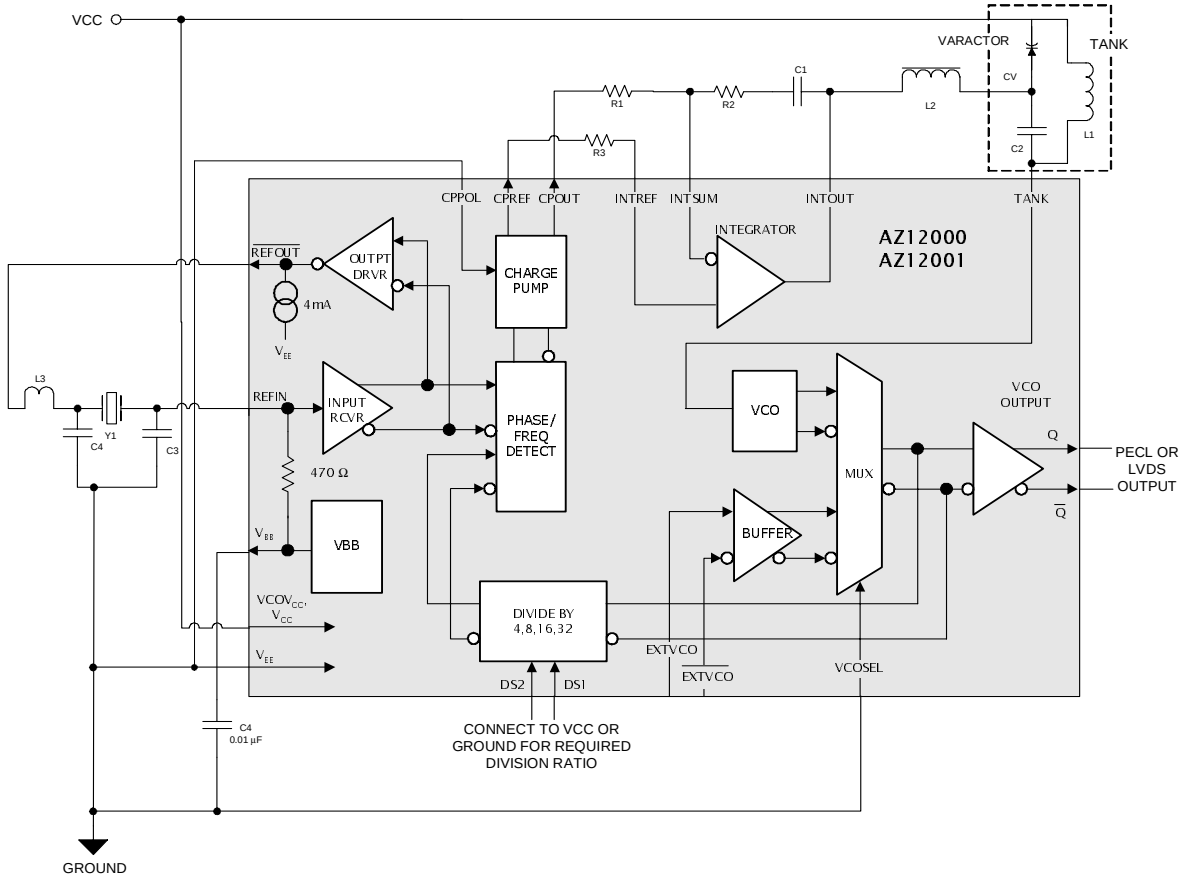
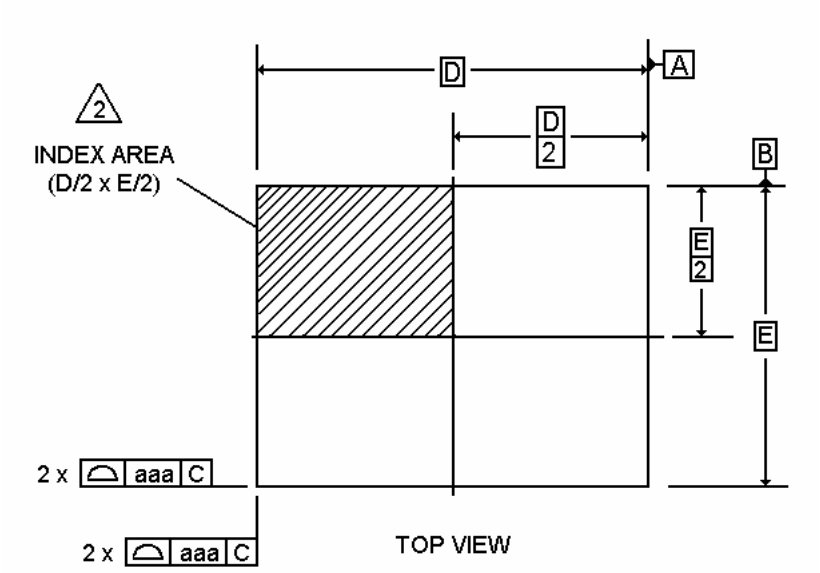
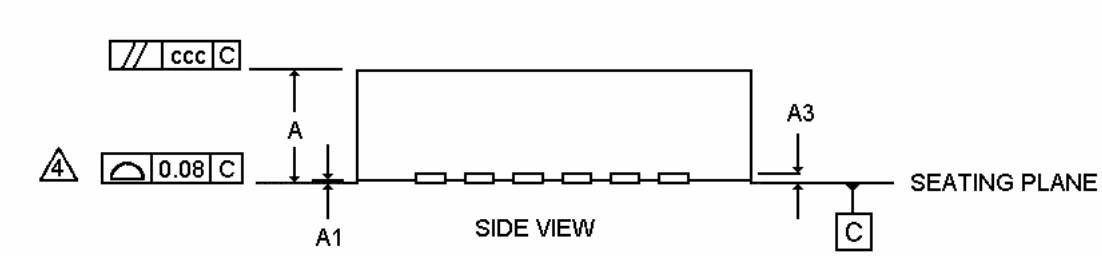


Figure 4. Typical Application with Crystal Reference and Internal VCO

PACKAGE DIAGRAM
MLP 24





NOTES

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
2. THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
3. DIMENSION b APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM PAD TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.18	0.30
D	3.90	4.10
D2	2.65	2.95
E	3.90	4.10
E2	2.65	2.95
e	0.50 BSC	
L	0.35	0.45
aaa	0.25	
bbb	0.10	
ccc	0.10