Features

- **PWM and Direction-controlled Driving of Four Externally Powered NMOS Transistors**
- **Internal Charge Pump Provides Gate Voltages for High-side Drivers in Permanent ON Mode and Supplies the Gate of the External Battery Reverse Protection NMOS**
- **5V Regulator With External Power Device (NPN) and Current Limitation Function**
- **Reset Derived From 5V Regulator Output Voltage**
- **Sleep Mode With Supply Current of Typical 35 µA, Wake-up by Signal on Pin EN or on SCI Interface (Pin /DATA)**
- **Window Watchdog; the Watchdog Time is Programmable by Choosing a Certain Value of the External Watchdog Capacitor C_{CWD} and the External Watchdog Resistor R_{CWD}**
- **Battery Overvoltage Protection and Battery Undervoltage Management**
- **Overtemperature Protection**
- **SCI Transceiver (Operating in Differential or Single-ended Mode) for Use at Battery Voltage Level**
- **Digital Control Block With the Control Pins EN, DIR, PWM**
- **Internal Low-power Regulator With Low-power Band Gap (Trimmed With Four Bits) to Guarantee Power Dissipation in Sleep Mode and to Guarantee Parameters for Wake-up**

H-bridge Motor Driver

ATA6026

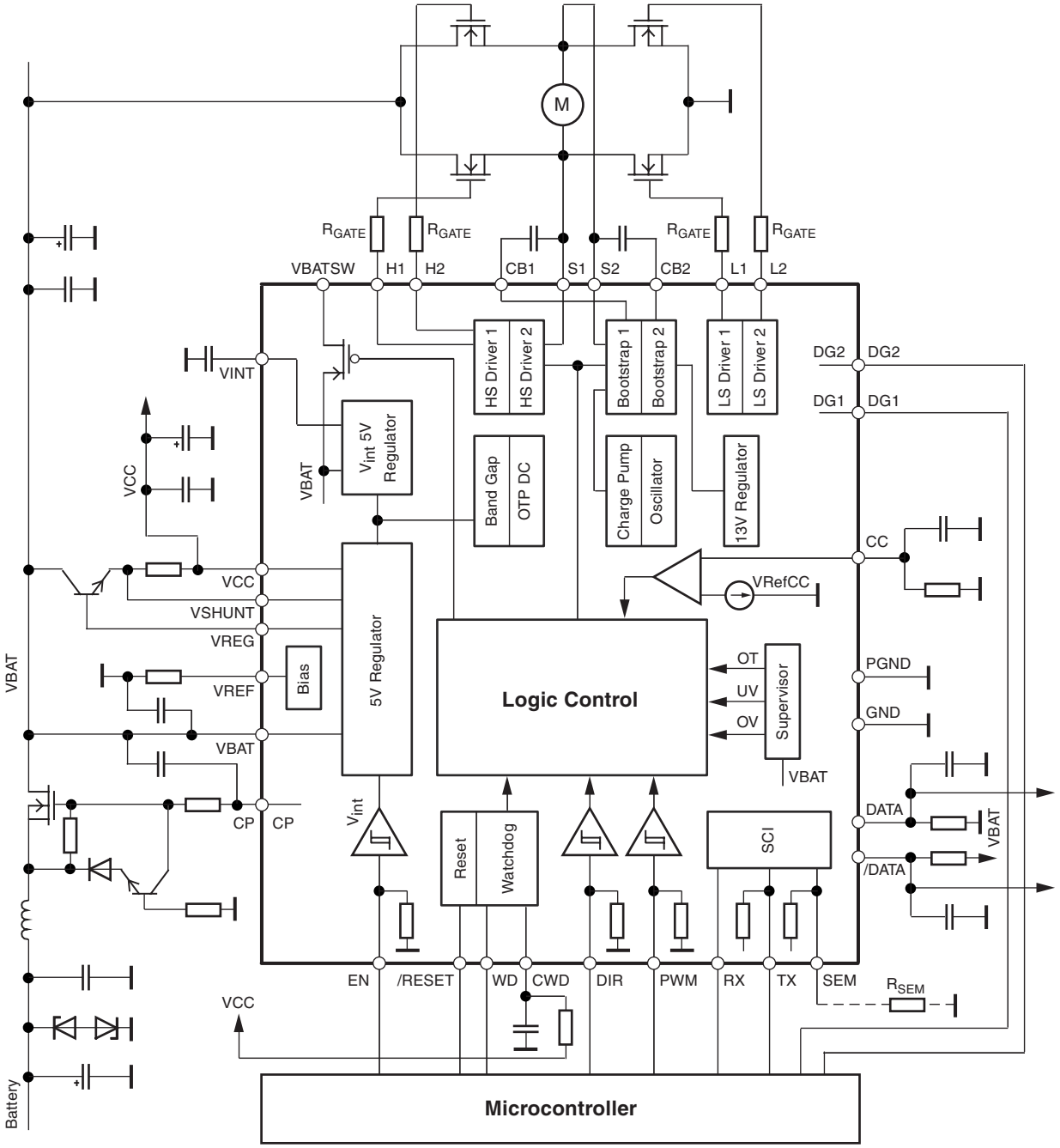
1. Description

The ATA6026 is used to drive a continuous-current motor in a full H-bridge configuration. An external microcontroller controls the driving function of the ATA6026 by providing a PWM signal and a direction signal, and allows the usage of the ATA6026 in a windshield wiper application, for example.

The ATA6026 supports PWM and direction-controlled driving of four external power MOSFETs with two external bootstrap capacitors. The PWM control is performed by the high-side switch. The opposite low-side switch is permanently ON in the driving phase. Motor braking is performed using the low-side switches. A programmable dead time is included to prevent peak currents within the H-bridge. The maximum PWM frequency is 30 kHz.

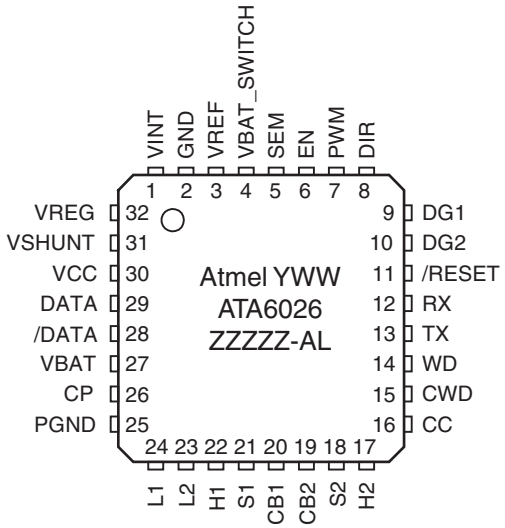
Rev. 4865C–AUTO–01/06

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN32



Note: YWW Date code (Y = Year above 2000, WW = week number)
ATA6026 Product name
ZZZZZ Wafer lot number
AL Assembly sub-lot number

Table 2-1. Pin Description

Pin	Symbol	Function	Description	ESD Protection
1	VINT	Supply	Output of internal voltage regulator (external blocking capacitor)	Open drain 14V + diode to GND + diode from VCC
2	GND	Pin	Ground, substrate of ATA6026	Diode to PGND
3	VREF	Analog in	Reference resistor for reference current	Open drain 14V + diode to GND
4	VBAT_SWITCH	Analog out (HV)	Connected with VBAT via an ATA6026-internal switch	Diodes to VBAT/GND
5	SEM	Digital input-PU	Control of SCI mode (Single-ended Mode)	Diodes to GND/VCC
6	EN	Digital input (HV) PD	Enable control input	Open drain HV + diode to GND
7	PWM	Digital input (HV) PD	PWM control input	Open drain HV + diode to GND
8	DIR	Digital input (HV) PD	Direction control input	Open drain HV + diode to GND
9	DG1	Digital output	Status output 1	Diodes to GND/VCC
10	DG2	Digital output	Status output 2	Diodes to GND/VCC
11	/RESET	Open drain-PU	Reset output, active low	Diodes to GND/VCC
12	RX	Digital output-PU	Data output pin of SCI interface	Diodes to GND/VCC
13	TX	Digital input-PU	Transmit control input for SCI interface	Diodes to GND/VCC
14	WD	Digital input	Watchdog trigger input	Diodes to GND/VCC
15	CWD	Analog in/out	Capacitor for definition of watchdog timer	Diodes to GND/VCC

Table 2-1. Pin Description (Continued)

Pin	Symbol	Function	Description	ESD Protection
16	CC	Analog in	Cross conduction time definition	Diodes to GND/VCC
17	H2	Analog out (HV)	Gate of external high-side NMOS 2	Floating open drain HV + diode to CB2
18	S2	Analog in/out (HV)	Source of external high-side NMOS 2	Floating open drain HV + diode to H2
19	CB2	Analog in/out (HV)	Boost capacitor 2 voltage input	Open drain HV + diode to GND
20	CB1	Analog in/out (HV)	Boost capacitor 1 voltage input	Open drain HV + diode to GND
21	S1	Analog in/out (HV)	Source of external high-side NMOS 1	Floating open drain HV + diode to H2
22	H1	Analog out (HV)	Gate of external high-side NMOS 1	Floating open drain HV + diode to CB1
23	L2	Analog out (HV)	Gate of external low-side NMOS 2	Open drain HV + diode to GND
24	L1	Analog out (HV)	Gate of external low-side NMOS 1	Open drain HV + diode to GND
25	PGND	Pin	Power ground (used for drivers and power devices of charge pump)	Diode to GND
26	CP	Analog out (HV)	Charge pump output	Open drain HV + diode from VBAT + diode to GND
27	VBAT	Supply (HV)	Battery voltage behind the reverse protection element	Open drain HV + diode to CP + diode to GND
28	/DATA	Analog in/out (HV)	Inverse data signal of SCI	Floating open drain HV
29	DATA	Analog in/out (HV)	Data signal SCI (high voltage + modulation)	Floating open drain HV
30	VCC	Supply	Feedback of regulated VCC and main supply of low voltage part of ATA6026	Open drain 14V + diode to GND
31	VSHUNT	Analog in	Sense input for current limitation in VCC regulator	Diodes to GND and VCC
32	VREG	Analog out	Base of external regulator pass device (NPN)	Open drain 14V + diode to GND

3. Functional Description

3.1 Power Supply Unit

3.1.1 Power Supply

The ATA6026 is supplied by a reverse-protected battery voltage. To prevent damage to the IC, proper external protection circuitry must to be added. Use of a capacitor combination of storage and HF capacitors behind the reverse protection circuitry and closed to the VBAT pin of the ATA6026 (Figure 1-1 on page 2) is recommended.

A fully-internal low-power and low-drop regulator with a voltage of 5V and cleaned by an external blocking capacitor provides the necessary low-voltage supply needed for the wake-up process. The low-power band gap is trimmed by OTPDC and is also used for the big regulator. The following blocks are supplied by the internal regulator:

- Enable input comparator
- Band gap
- Wake-up part of the SCI interface
- Digital control of the complete ATA6026
- OTPDC
- VCC regulator (5V external)

The internal supply voltage VINT must not be used for any other supply reasons!

All the remaining blocks are supplied by the VCC regulator (5V).

For detection reasons by microcontroller, there is a high-voltage switch which brings out the battery voltage to the pin VBAT_SWITCH. This switch is ON for VCC > V_{thRES}.

3.2 Sleep Mode

Sleep mode exists to guarantee the low quiescent current of the inactive ATA6026. In Sleep mode it is possible to wake up the IC by using the pins EN or /DATA. The following blocks are active in Sleep mode:

- Band gap
- Internal 5V regulator with external blocking capacitor of 100 nF
- Input structure for detecting the EN pin threshold
- Wake-up block of SCI receive part

3.3 Wake-up and Sleep Mode Strategy

The ATA6026 has 2 modes: Sleep and Active. To change between the two modes, 3 procedures are implemented and described here.

The default state after power-on is Active mode.

1. Go to Sleep

   A HIGH to LOW transition at pin EN, followed by a LOW for the time $t_{gotosleep}$ (typically 50 ms), switches the ATA6026 to Sleep mode.

   The internal 5V supply V_{INT}, the EN pin input structure, and a certain part of the SCI receiver are permanently active to ensure proper startup of the system.

2. Go to Active by activating pin EN

   The input structure on pin EN consists of a comparator with built-in hysteresis. The input of the comparator is protected against voltages up to $VBAT_{max}$.

   Pulling the EN pin up to HIGH for a time longer than t_{wakeEN} (typically 50 ms) will switch the ATA6026 to Active mode.

3. Go to Active via the SCI interface

   The second possibility for waking up the part is to use the SCI transceiver. In Sleep mode the SCI receiver is partially active and works in single-ended mode, independent of the status of the pin SEM.

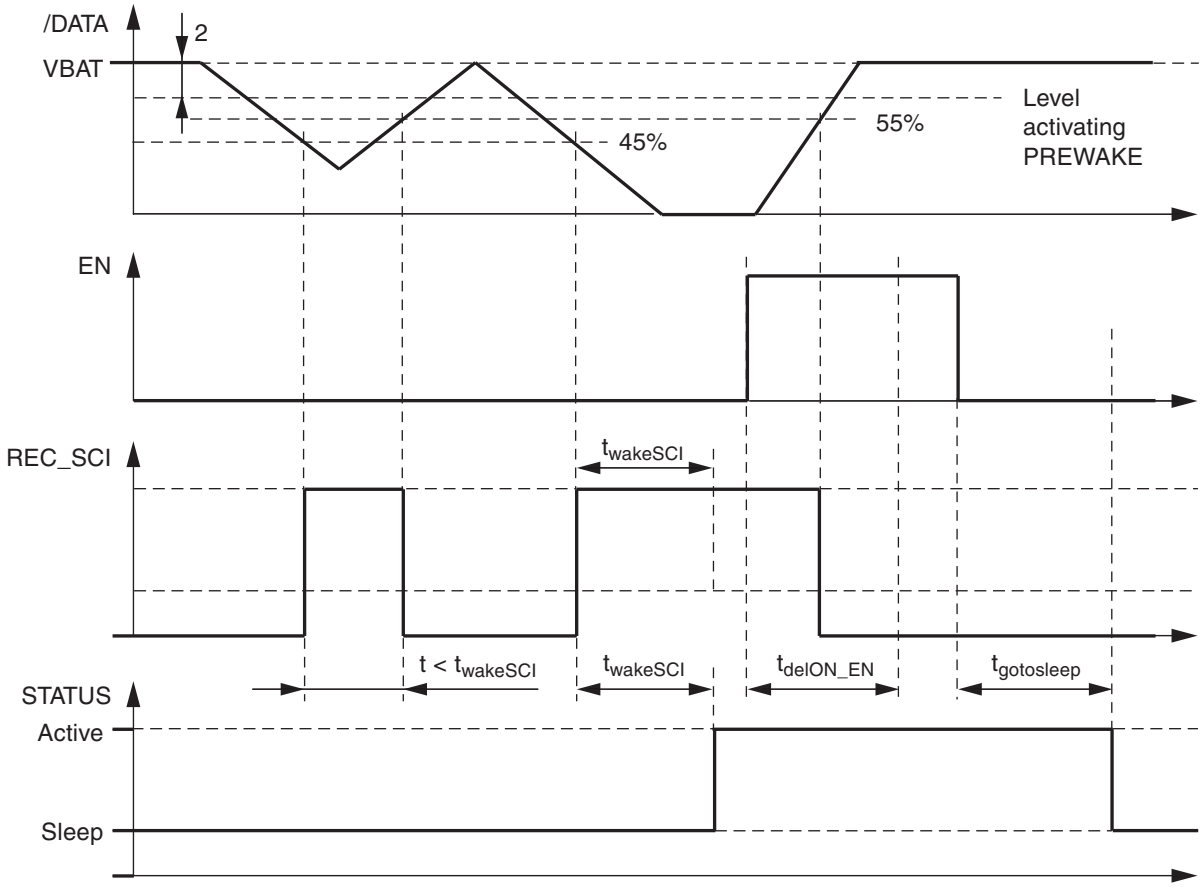
   The wake-up by SCI requires 2 steps:

   a. If the voltage on pin /DATA is below a value of $V_{/DATwake}$ (about V_{VBAT} – 2V), the receive part of the SCI interface is active (not to be confused with Active mode of the whole IC). The active receive part is able to detect a valid LOW on the /DATA pin.
   b. If /DATA is LOW for a filter time $t_{wakeSCI}$ (typically 50 ms), the IC will change to Active mode. A short change back to HIGH during the filter time will reset the filter. After entering the Active mode, this information is stored in a latch.

   When the SCI interface is used to switch to Active mode, the EN pin can remain LOW without disturbing the Active mode status.

Figure 3-1 on page 7 illustrates the wake-up by SCI.

Figure 3-1. Wake-up by SCI, Pin /DATA



The status PREWAKE is characterized by the activated receive block of SCI and activated comparator of EN input. After going to Active, the V_{CC} regulator starts working. “Go to Sleep” is possible via a valid HIGH to LOW transition at pin EN (remaining LOW for longer than $t_{gotosleep}$), if EN was previously in a valid HIGH state (HIGH for longer than t_{delON_EN}).

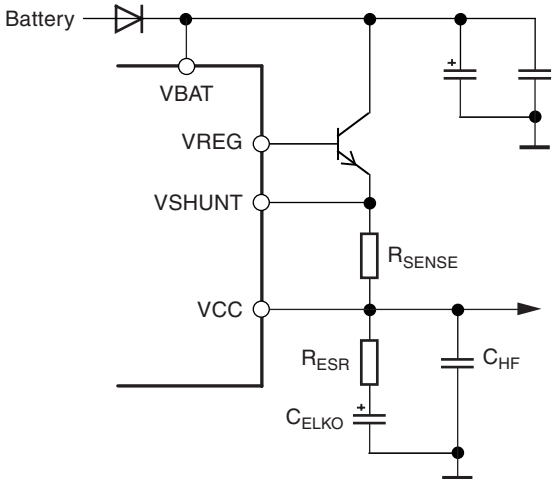
3.4 5V Regulator

The 5V regulator is on-chip, using an external NPN as the power element. The reason behind using an external pass device is to prevent large power dissipation within the ATA6026. For a battery voltage level between 6V and 9V, the regulated output voltage is 5V ±10%; above $V_{VBAT} \geq 9V$, the regulated output voltage is 5V ±3%.

To prevent the destruction of the external NPN and the ATA6026, a sense resistor is used to detect the current delivered by the regulator. In case of overcurrent, the regulator limits the current to the specified level. This means that if the characteristic of the voltage regulator changes to the characteristic of a current regulator, the delivered voltage will break down.

To function correctly, the regulator requires an external NPN transistor with a minimum BN of 25.

Figure 3-2. Principal Function of the 5V Regulator with External Pass Device



3.5 Reset and Watchdog Management

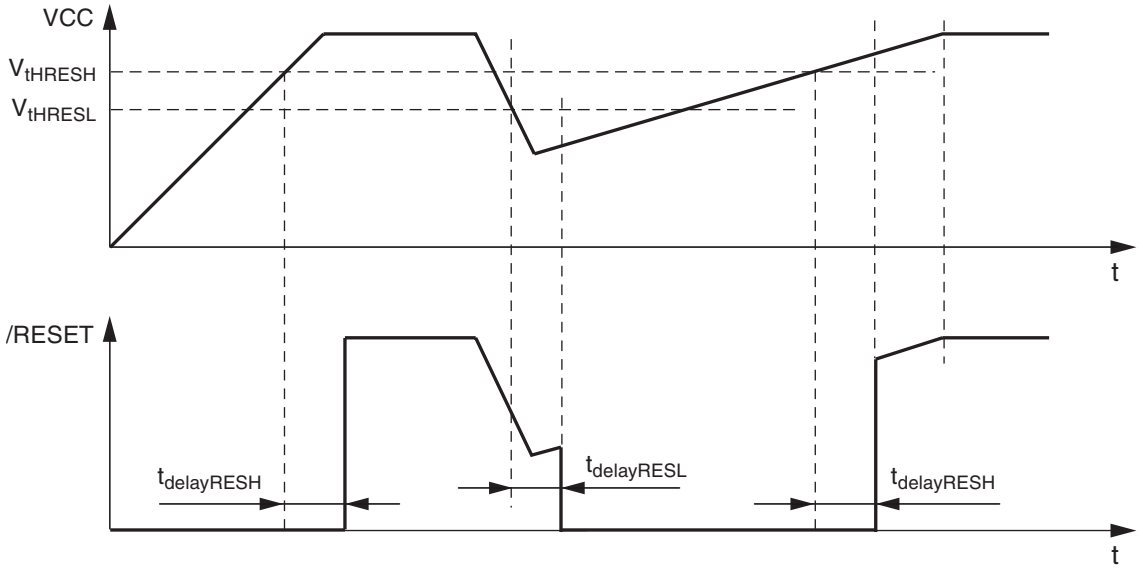
The reset and watchdog management block controls the pin /RESET and influences the behavior of the internal circuitry.

The /RESET pin is active low with an internal pull-up resistor to VCC.

- Static reset dependent on VCC level

  The reset will be active for $V_{CC} < V_{tHRESx}$. The level V_{tHRESx} is realized with a hysteresis (HYS_{RESth}).

Figure 3-3. Static Reset Behavior



- Dynamic reset dependent on watchdog behavior

Figure 3-4 shows the principal behavior of the watchdog.

An RC oscillator composed of the external elements R_{CWD} and C_{CWD} defines the timing base of the watchdog (referred to here as t).

$t(\mu s) = t_{dis}(\mu s) + 1.1 \times R_{CWD}(k\Omega) \times [C_{CWD}(nF) + C_{parasitic}(nF)]$

$t_{dis} = 1.83\ \mu s$

($C_{parasitic}$ is assumed to be 10 pF (pad capacitance + wiring capacitance on PCB))

The watchdog is realized as a window watchdog and will be triggered by the microcontroller via a LOW to HIGH transition at pin WD during the open window. If the watchdog detects a window error (no trigger in open window or wrong trigger in closed window), a reset pulse of length t_{res} will be generated. To relieve the watchdog trigger after power-on, the first open window is longer by a factor of about 4.5 compared to the following windows.

$t_{OW} = t \times 185$ (open window)

$t_{CW} = t \times 185$ (closed window)

$t_{OW1} = t \times 832$ (first open window after power-on)

$t_{res} = t \times 43$ (reset pulse length)

Figure 3-4. Principal Behavior of the Watchdog

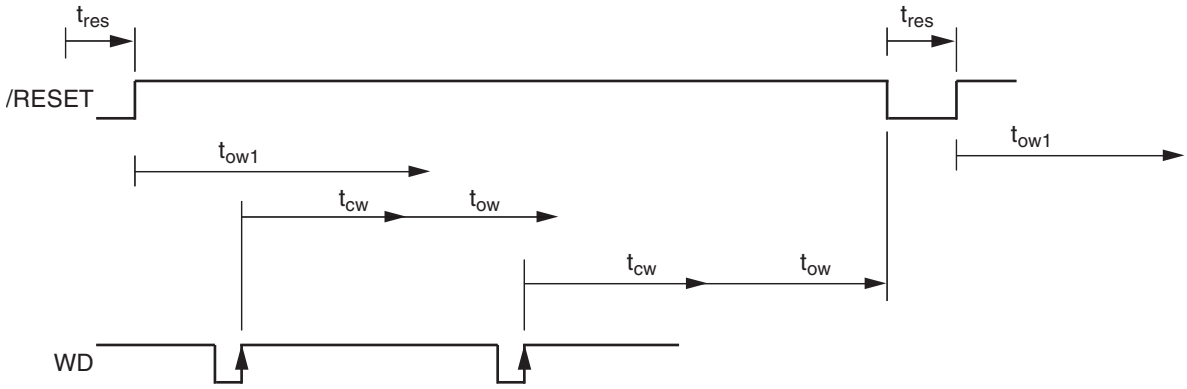


Figure 3-5. External Elements of the Watchdog

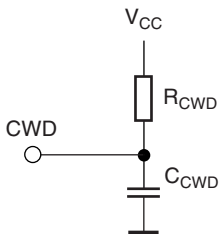


Table 3-1. Examples of Watchdog Oscillator Period t (µs) as a Function of C_{CWD} and R_{CWD}

R_{CWD} (kΩ) \ C_{CWD} (pF)	3300	2200	1000	810	680	560	100
100	366.0	245.1	113.3	92.4	78.2	65.0	14.4
81	296.9	199.0	92.2	75.3	63.8	53.1	12.1
75	275.1	184.4	85.6	69.9	59.2	49.3	11.4
68	249.6	167.4	77.8	63.6	53.9	44.9	10.6
62	227.8	152.9	71.1	58.2	49.3	41.2	9.8
56	206.0	138.3	**64.5**	52.8	44.8	37.4	9.1
51	187.8	126.2	58.9	48.3	41.0	34.3	8.5
47	173.3	116.5	54.5	44.7	38.0	31.8	8.0
43	158.7	106.8	50.1	41.1	34.9	29.3	7.5
39	144.2	97.0	45.6	37.5	31.9	26.8	7.1
36	133.3	89.8	42.3	34.8	29.6	24.9	6.7
33	122.4	82.5	39.0	32.1	27.4	23.0	6.3
30	111.4	75.2	35.6	29.4	25.1	21.1	6.0
27	100.5	67.9	32.3	26.7	22.8	19.3	5.6
24	89.6	60.6	29.0	24.0	20.5	17.4	5.3
22	82.4	55.8	26.8	22.2	19.0	16.1	5.0
20	75.1	50.9	24.5	20.4	17.5	14.9	4.8
18	67.8	46.1	22.3	18.6	16.0	13.6	4.5
16	60.5	41.2	20.1	16.8	14.5	12.4	4.3
15	56.9	38.8	19.0	15.9	13.7	11.7	4.2
13	49.6	33.9	16.8	14.1	12.2	10.5	3.9
12	46.0	31.5	15.7	13.2	11.4	9.9	3.8
10	38.7	26.6	13.4	11.4	9.9	8.6	3.6

Do not use capacitors greater than 3.3 nF or less than 470 pF
Do not use resistors less than 10 kΩ or greater than 100 kΩ
Do not apply periods shorter than 11.5 µs (f < 85 kHz is to be used)

For a typical application with C = 1 nF and R = 56 kΩ, we will get the following values:

t_{res} = 2.77 ms

$t_{ow} = t_{cw}$ = 11.9 ms

t_{ow1} = 53.66 ms

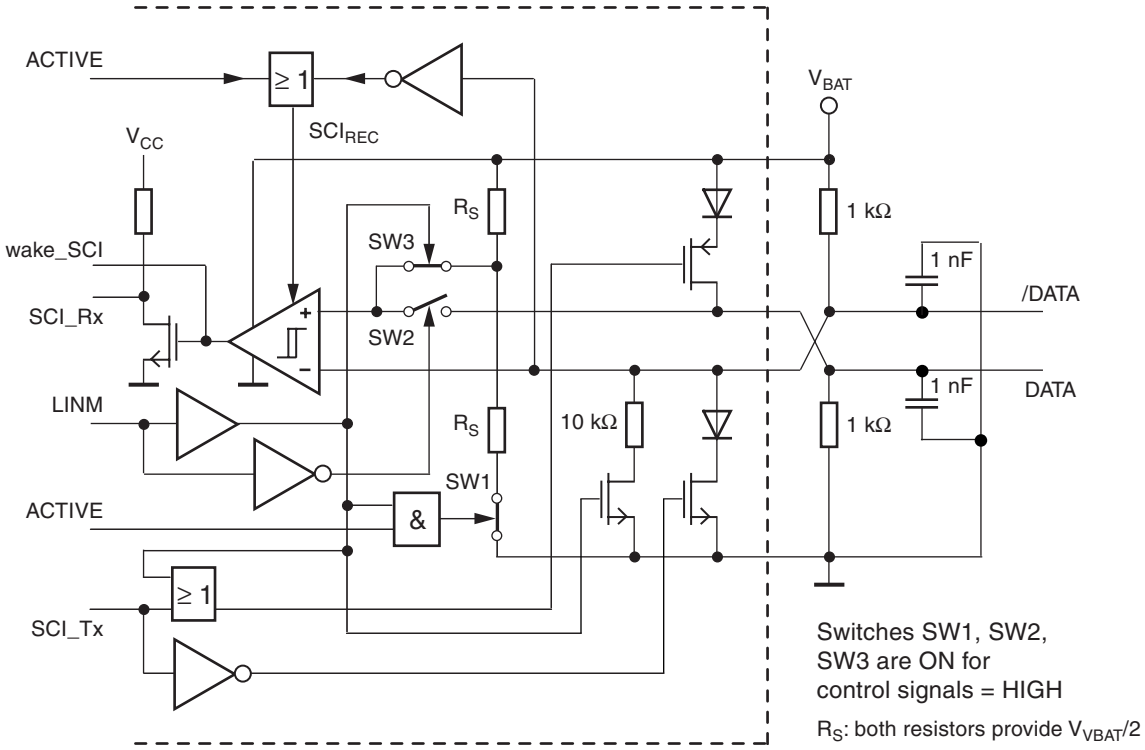
The internal tolerance is < 6.5%; tolerances of external elements have to be included into the period calculation.

3.6 SCI Transceiver

The SCI transceiver is a differential device which can also work in single-ended mode. In single-ended mode the levels and the currents are compatible with the LIN interface, but use a faster timing. It is necessary to define the SCI differential mode by externally pulling down the pin SEM. Single-ended mode is the default if the pin SEM is left open. In this case, the /DATA pin is active. The typical external elements on pin DATA are also recommended for single-ended mode (SEM mode). The driver on pin DATA is passive in single-ended mode.

SEM is a digital input pin with an internal pull-up resistor to VCC. So, in Sleep mode no current will flow through the pull-up resistor and affect the Sleep mode supply current, as the V_{CC} regulator is down while in Sleep mode.

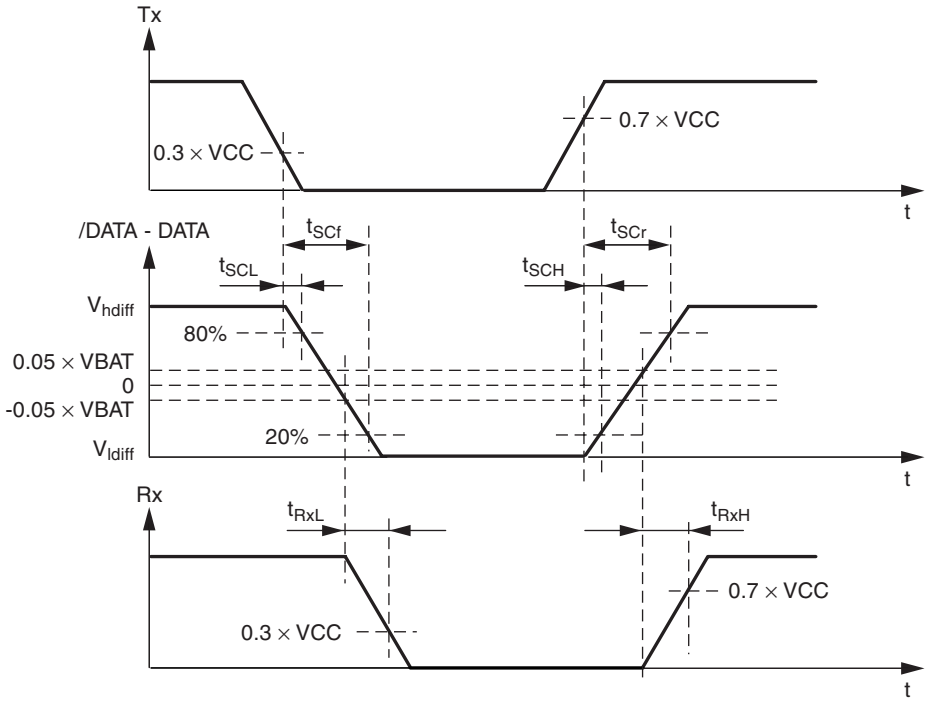
Figure 3-6. Principal Function of SCI



Definition of symbols in Figure 3-6:

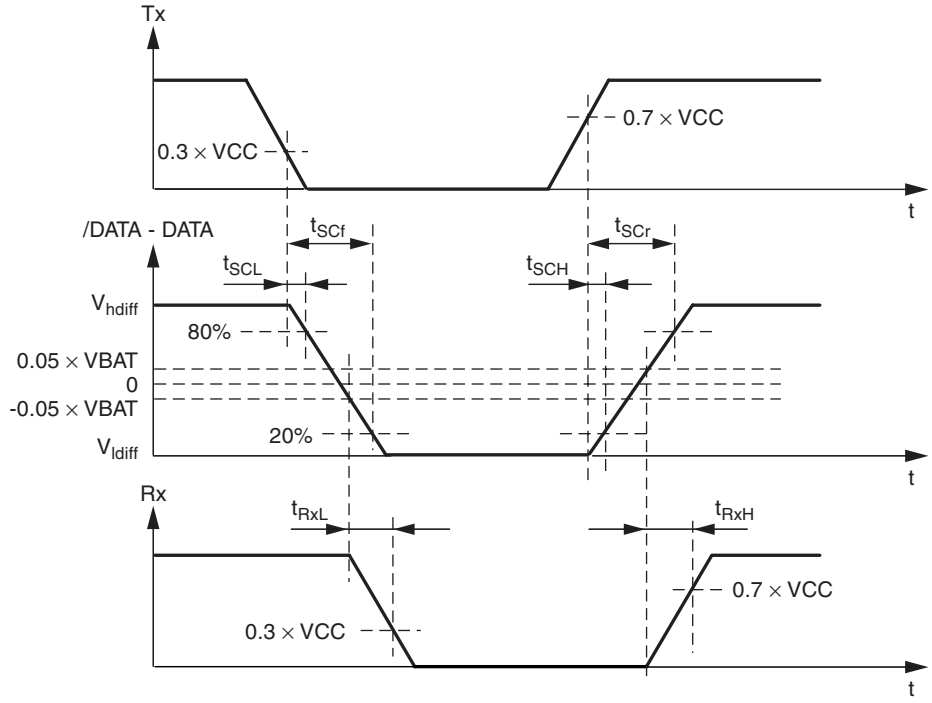
ACTIVE:	ATA6026 is in Active mode
SCI_{REC}:	Receive part of SCI is working
VCC:	V_{CC} voltage (pin VCC)
wake_SCI:	Wake-up by SCI performed (for more information on the filter time $t_{wakeSCI}$, see"Wake-up and Sleep Mode Strategy" on page 6)
SCI_Rx:	Rx output of SCI
SEM:	Single-ended mode of SCI when SEM = HIGH (SEM = "Single-ended Mode")
V_{VBAT}:	Voltage at pin VBAT (not car battery!)

Figure 3-7. Timing of SCI (Differential Mode)



$V_{hdiff} = V_{VBAT}$ (SCI driver is passive, recessive mode)
$V_{ldiff} = V_{T/DATAL} - V_{TDATAH}$ ($V_{T/DATAL}$ is the output low voltage of pin /DATA)

Figure 3-8. Timing of SCI (Single-ended Mode)



$V_{T/DATAL}$ is the output low voltage of pin /DATA

When SEM is HIGH (single-ended mode), the reference for the receive comparator will be switched from signal DATA to V_{VBAT} / 2. It is not necessary to do this external of the ATA6026; the signal SEM = HIGH signals this request to the ATA6026.

It is recommended, but not necessary, to use the external connections of DATA and /DATA for both differential mode and single-ended mode as specified in Figure 3-6 on page 11. The pin DATA may also be kept open if single-ended mode is programmed.

3.7 Control Inputs EN, DIR, PWM

Pin EN: The enable pin is used to activate the ATA6026 with a HIGH. This input uses low voltage levels but has to withstand a voltage up to 40V. An internal pull-down resistor is included.

Pin DIR: Logical input to control the direction of the external motor. An internal pull-down resistor is included. The test mode is entered when this pin is pulled to a voltage above 10V.

Pin PWM: Logical input for PWM information delivered by external microcontroller. Duty cycle and frequency of switching can be choosen by this pin. An internal pull-down resistor is included. The test mode is entered when this pin is pulled to a voltage above 10V.

Table 3-2. Status of the ATA6026 Depending on Control Inputs and Detected Failures (x Means Don't Care)

Control Inputs			Device Status				Driver Stage for External Power MOS				Diagnostic Outputs		Comments
EN	DIR	PWM	TS	OV	UV	SC	H1	L1	H2	L2	DG1	DG2	
0	x	x	x	x	x	x	Off	Off	Off	Off	0	0	Standby mode
1	x	x	1	0	0	0	Off	Off	Off	Off	1	1	Thermal shutdown(1)
1	x	x	0	1	0	0	Off	Off	Off	Off	0	1	Overvoltage(1)
1	x	x	0	0	1	0	Off	Off	Off	Off	1	0	Undervoltage(1)
1	x	x	0	0	0	1	Off	Off	Off	Off	1	1	Short circuit(1)
1	0	PWM	0	0	0	0	PWM	/PWM	Off	On	0	0	Motor PWM forward
1	1	PWM	0	0	0	0	Off	On	PWM	/PWM	0	0	Motor PWM backward
1	x	0	0	0	0	0	Off	On	Off	On	0	0	Motor brake
1	1	1	0	0	0	0	Off	On	On	Off	0	0	Motor full forward
1	0	1	0	0	0	0	On	Off	Off	On	0	0	Motor full backward

Note: 1. See section "Diagnosis" on page 14 for explanation

TS: Thermal shutdown
OV: Overvoltage of VBAT
UV: Undervoltage of VBAT
SC: Short circuit

3.8 Diagnosis

Table 3-3. Table of Events Detected by the ATA6026

Event	Description	DG1	DG2	Additional reaction of ATA6026	Timing
UV	Undervoltage ($V_{BAT} < V_{THUV}$)	1	0	Switch OFF L1, L2, H1, H2	16 µs to 35 µs after detection
Release UV	V_{BAT} increasing above V_{THUV}	0	0	Switch ON L1, L2, H1, H2 according to PWM/DIR status	After LOW to HIGH transition at PWM
OV	Overvoltage ($V_{BAT} > V_{THOV}$)	0	1	Switch OFF L1, L2, H1, H2	16 µs to 35 µs after detection
Release OV	V_{BAT} increasing above V_{THOV}	0	0	Switch ON L1, L2, H1, H2 according to PWM/DIR status	After LOW to HIGH transition at PWM
SC	Short circuit (if source-drain voltage of switched external NMOS is > 4V, short circuit is detected)	1	1	Switch OFF L1, L2, H1, H2	5 µs to 15 µs after detection
Release SC	Short circuit condition disappears	0	0	Switch ON L1, L2, H1, H2 according to PWM/DIR status	After LOW to HIGH transition at PWM
TS	Thermal shutdown (junction temperature > 165°C ±hysteresis)	1	1	Switch OFF L1, L2, H1, H2, DATA, /DATA	Directly after detection
Release TS	Thermal shutdown (junction temperature < 165°C ±hysteresis)	0	0	Switch ON L1, L2, H1, H2, according to PWM/DIR status	After LOW to HIGH transition at PWM
				Switch ON DATA, /DATA according to Tx status	Directly after detection

Note: After power-on, the undervoltage status may be latched. To switch the drivers ON, a LOW to HIGH transition at PWM is required.

3.8.1 Overvoltage

This block protects the IC and the external power MOS transistors against overvoltage on the battery.

Function: In the case of overvoltage alarm (V_{THOV}), the external NMOS transistors will be switched off, and the event will be signalled by switching the pin DG2 ON (see Table 3-3). If the overvoltage condition disappears, after the next LOW to HIGH transition at pin PWM, the drivers for the external power MOS transistors will switch back to the status defined by the control pin DIR and the pin DG2 will be cleared to LOW if there is no other event to be signalled. The SCI drivers are not influenced by the voltage supervisor. The comparator includes a hysteresis.

3.8.2 Undervoltage

This block switches off the external power MOS transistors in case of undervoltage on the battery.

Function: In case of undervoltage alarm (V_{THuV}), the external NMOS transistors will be switched off and the event will be signalled by switching ON the pin DG1 (see Table 3-3 on page 14). If the undervoltage condition disappears, after the next LOW to HIGH transition at pin PWM the drivers for the external power MOS transistors will switch back to the status defined by the control pin DIR, and the pin DG1 will be cleared to LOW if there is no other event be signalled. The SCI drivers are not influenced by the voltage supervisor. The comparator includes a hysteresis.

3.8.3 Temperature Supervisor

There is a temperature sensor integrated on-chip to prevent overheating of the ATA6026 and to protect external NMOSFETS from a failure in external circuitry. In case of detected overtemperature (150°C to 180°C), all drivers including SCI drivers will be switched OFF immediately and both of the diagnostic pins DG1 and DG2 will be switched to HIGH to signal this event to the processor.

The status thermal shutdown (TS) will be stored in a latch: After the next LOW to HIGH transition at pin PWM, the drivers for the external power MOS transistors will switch back to the status defined by the control pin DIR, the pins DG1 and DG2 will be cleared to LOW if there is no other event to be signalled, and the SCI drivers immediately will switch to the status defined by the control pin TX.

A hysteresis is built in to prevent fast oscillations.

Attention: With DG1 = DG2 = HIGH, short circuit is signalled as well as overtemperature.

3.8.4 Short Circuit Detection

To detect a short in H-bridge circuitry, internal comparators detect the voltage difference between source and drain of the external power NMOS. If transistors are switched ON and the source drain voltage difference is higher than the value VSC (4V with tolerances) for a time greater than t_{SC}, the signal SC (short circuit) will be set, the external power MOS transistors will be switched off immediately, and the pins DG1 and DG2 will be switched to HIGH to signal this event to the processor.

With the next programmed LOW to HIGH transition on pin PWM, the bits will be cleared and the corresponding drivers will switch back to the status defined by the control pin DIR; the pins DG1 and DG2 will switch back to LOW if the short circuit condition has cleared.

3.9 Behavior of the Bridge Drivers in Case of RESET

In case of RESET (/RESET = LOW), the high-side drivers will be switched OFF and the low-side drivers will remain in the status defined by PWM and DIR.

In case of overvoltage (OV), undervoltage (UV), thermal shutdown (TS), or short circuit (SC), all the drivers will be switched off, independent of the status of the /RESET pin.

3.10 Charge Pump

The fully-integrated charge pump is needed to supply the gates of the external power MOSFETs of the HS drivers in case of permanent ON (100% PWM, no bootstrap function is available). In addition, the gate of the external power NMOS used for reverse battery protection is supplied by the charge pump output.

The charge pump is fully integrated, including the oscillator with a typical frequency of 2.2 MHz, and works by pumping the regulated 5V three times above the battery. In addition, the charge pump output is supplied by the action of the bootstrap capacitors.

If EN is switched to “0” (Sleep mode), the charge pump function is disabled, and the charge pump output voltage will be set to one diode threshold below V_{BAT}.

3.11 H-bridge Driver

The IC includes two push-pull drivers to control two external power NMOS used as high-side drivers, and two push-pull drivers to control two external power NMOS used as low-side drivers. The drivers can be used with either standard or logic-level power NMOS.

The drivers for the high-side control use external bootstrap capacitors to supply the gates with a voltage of 8V to 14V above the battery voltage level.

The bootstrap capacitor has to be greater than or equal to $10 \times C_{GATE}$, where C_{GATE} is the capacitance of the external switching NMOS. Smaller values of bootstrap capacitor will reduce the dynamic gate voltage of the external switching NMOS.

It is also possible to control the external load (motor) in the reverse direction (see Table 3-3 on page 14).

A duty cycle of 100% in both directions is possible, using the charge pump to supply the gates of the high-side drivers.

The output voltage of the drivers for the low-side control is limited to a level of less than 16V, but is not clamped active.

3.11.1 Cross Conduction Time

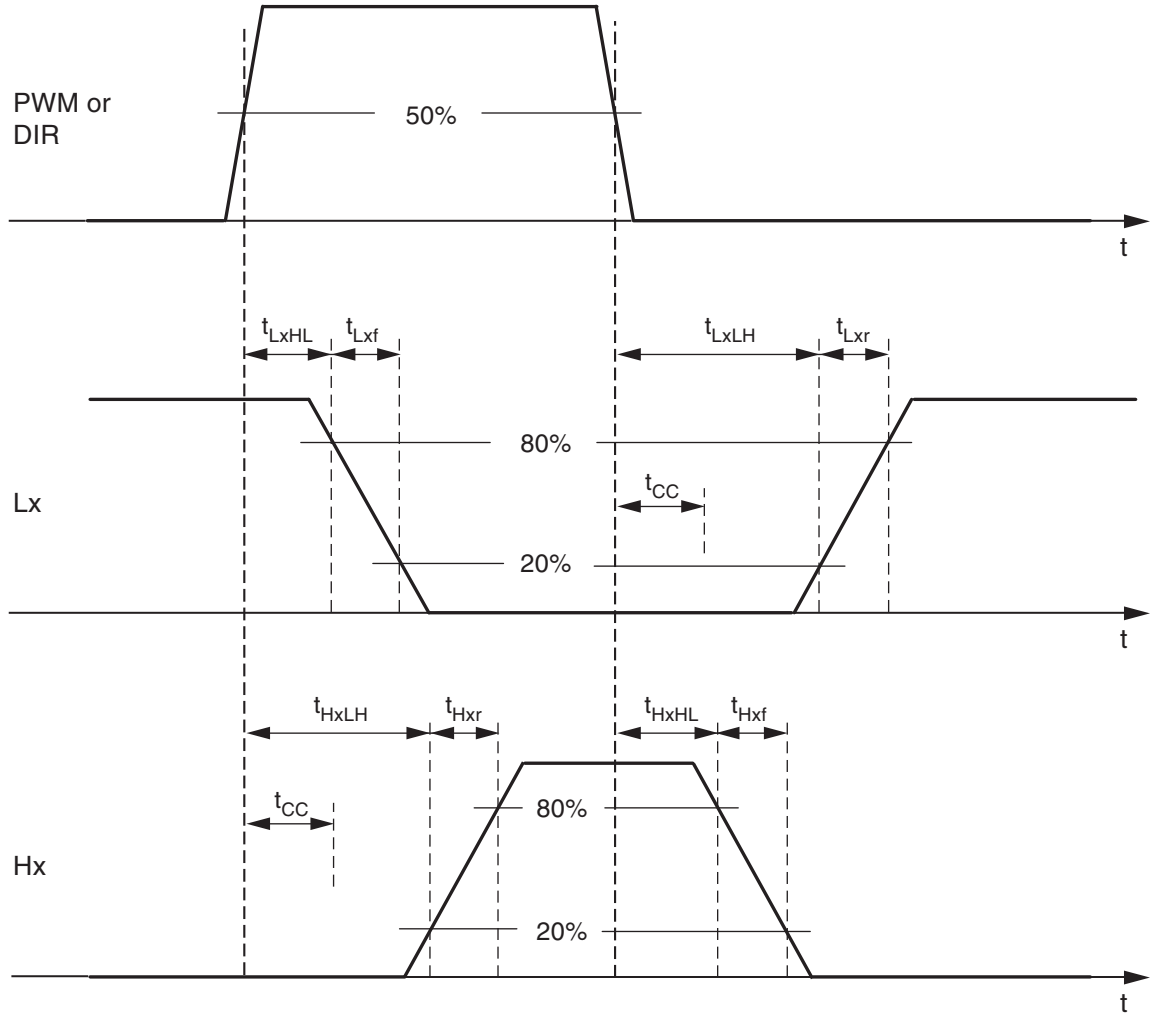
To prevent high peak currents in the H-bridge, a non-overlapping phase for switching the external power NMOS is realized. An external RC combination defines the cross conduction time in the following way:

t_{CC} (µs) = $0.36 \times R_{CC}$ (kΩ) $\times C_{CC}$ (nF) + 0.2 (tolerance: ±5% ±0.15 µs)

The RC combination is charged to 5V and the switching level of the internal comparator is 67% of the start level.

The time measurement is triggered by the PWM or DIR signal crossing the 50% level.

Figure 3-9. Timing of the Drivers



The delays t_{HxLH} and t_{LxLH} include the cross conduction time t_{CC}.

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Description	Pin Name	Min	Max	Unit
Ground	GND	0	0	V
Power ground	PGND	–0.3	+0.3	V
Reverse-protected battery voltage	VBAT	–0.3	+40	V
VBAT behind internal switch	VBAT_SWITCH	–0.3	V_{VBAT} + 0.3	V
Digital output	/RESET	–0.3	V_{VCC} + 0.3	V
Digital output	DG1, DG2	–0.3	V_{VCC} + 0.3	V
Analog input (LV)	VREF	–0.3	V_{VCC} + 0.3	V
5V output, external blocking capacitor	VINT	–0.3	+7	V
Base of external NPN for 5V regulator	VREG	–0.3	+7	V
Cross conduction time capacitor/resistor combination	CC	–0.3	V_{VCC} + 0.3	V
Digital input coming from microcontroller	WD	–0.3	V_{VCC} + 0.3	V
Watchdog timing resistor	CWD	–0.3	V_{VCC} + 0.3	V
Digital input direction control	DIR	–0.3	+25	V
Digital input PWM control and test mode	PWM	–0.3	+25	V
Digital input for enable control	EN	–0.3	+40	V
Digital input SCI mode control	SEM	–0.3	V_{VCC} + 0.3	V
5V regulator output	VCC	–0.3	+7	V
Sense of 5V regulator current	VSHUNT	–0.3	+7	V
Digital output	RX	–0.3	V_{VCC} + 0.3	V
Digital input	TX	–0.3	V_{VCC} + 0.3	V
SCI data pin	DATA	–27[1]	V_{VBAT} + 2	V
SCI data pin	/DATA	–27[1]	V_{VBAT} + 2	V
Bootstrap capacitor pin	CBI, CB2	–0.3	+45	V
Source external high-side NMOS	S1, S2	–2	V_{VBAT} + 2	V
Gates external low-side NMOS	L1, L2	V_{PGND} – 0.3	+25	V
Gates of external high-side NMOS	H1, H2	–2	+45	V
Charge pump	CP	–0.3	+50	V
Power dissipation	P_{tot}		0.5[2]	W
Storage temperature	ϑ_{STORE}	–40	+150	°C
Soldering temperature (10s)	$\vartheta_{SOLDERING}$		260	°C

Notes: 1. For $V_{VBAT} \leq 13.5V$

2. May be additionally limited by external thermal resistance

5. Operating Range

The operating conditions define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not implied unless otherwise stated explicitly.

Parameters	Symbol	Min	Max	Unit
Operating supply voltage(1)	V_{VBAT1}	7	18	V
Operating supply voltage(2)	V_{VBAT1_a}	18	25	V
Operating supply voltage(3)	V_{VBAT2}	6	< 7	V
Operating supply voltage(4)	V_{VBAT3}	3	< 6	V
Operating supply voltage(5)	V_{VBAT4}	0	< 3	V
Operating supply voltage(6)	V_{VBAT5}	> 25	40	V
Ambient temperature range under bias	$\vartheta_{ambient}$	–40	+125	°C

Note: 1. Full functionality
2. $t \leq 2$ min (jump start)
3. H-bridge drivers may be switched off (undervoltage detection)
4. H-bridge drivers are switched off, 5V regulator and charge pump with reduced parameters, RESET works correctly
5. H-bridge drivers are switched off, 5V regulator and charge pump not working, RESET not correct
6. H-bridge drivers are switched off, load dump

6. Temperature Conditions

Junction Temperature/°C	Status of IC
–40 to +150	Normal functionality
150 to 180	Drivers for H1, H2, L1, L2, DATA, /DATA may be switched OFF, (DG1 and DG2 will be HIGH in this case), parameters may depart from specified values
> 180	Drivers for H1, H2, L1, L2, DATA, /DATA are switched OFF and DG1 and DG2 will be HIGH (to signal overtemperature), parameters may depart from specified values. 180°C is the maximum switch-off temperature

7. Electrical Characteristics

All parameters given are valid for 7V ≤ VBAT ≤ 40V and for –40°C ≤ $\vartheta_{ambient}$ ≤ 125°C unless stated otherwise.
Conditions: SEM = HIGH (single-ended mode of SCI).

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
1	**Power Supply and Supervisor Functions (This Block Supplies Parts of the ATA6026 Used for Startup and Supervises the V_{BAT} Voltage (Battery Voltage Behind the Reverse Battery Protection Device))**								
1.1	Current consumption VBAT	V_{VBAT} = 13.5V(1)		I_{VBAT1}			7	mA	
1.2	Current consumption VCC	V_{VCC} = 5V(1)		I_{VCC}			3	mA	
1.3	Current consumption VBAT, in standby mode	V_{VBAT} = 13.5V(3)		I_{VBAT2}		35	70	µA	
1.4	Internal power supply	V_{VBAT} ≥ 5.2V		V_{INT}	4.75	5	5.25	V	
1.5	Buffered band-gap voltage	V_{VBAT} ≥ 5V(2)		V_{BG}	1.21	1.26	1.33	V	
1.6	Overvoltage threshold VBAT			V_{THOV}	25		29	V	
1.7	Delay time overvoltage			t_{OV}	16		35	µs	
1.8	Overvoltage threshold hysteresis VBAT	Measured during qualification only		V_{TOVhys}		0.7		V	
1.9	Undervoltage threshold VBAT			V_{THUV}	6	6.5	7	V	
1.10	Delay time undervoltage			t_{UV}	16		35	µs	
1.11	Undervoltage threshold hysteresis VBAT	Measured during qualification only		V_{TUVhys}		0.4		V	
1.12	ON resistance of VBAT switch	V_{VBAT} = 13.5V		R_{ON_VBATSW}			1	kΩ	
1.13	Resistor defining internal bias currents used for internal timings, regardless of watchdog timing	Tolerance: ≤ 1%		R_{VREF}		20		kΩ	

* Type: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. EN, DIR, PWM = HIGH
2. Internal band-gap voltage is valid for VBAT > 3V (not testable)
3. Valid for –40°C to +90°C
4. R_{SHUNT} = 1Ω
5. Tested during qualification only
6. For timing, see the formula in "Reset and Watchdog Management" on page 8. All times depend on external elements C_{CWD} and R_{CWD}, tolerances of these elements have to be added to the given tolerances in the above table
7. External parasitic capacitive load together with pull-up resistor at RX defines the time t_{RxH}
8. If single-ended mode is used (SEM = HIGH): DATA is not used and VBAT / 2 instead of DATA is the internal reference for parameters 4.10 and 4.11
9. Maximum voltage difference arises during slope, see Figure 7-1 on page 30
10. Parameters 4.16 to 4.19 are based on transmit voltage slopes at DATA and /DATA of 4V/µs ±50%

7. Electrical Characteristics (Continued)

All parameters given are valid for 7V ≤ VBAT ≤ 40V and for –40°C ≤ $\vartheta_{ambient}$ ≤ 125°C unless stated otherwise.
Conditions: SEM = HIGH (single-ended mode of SCI).

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
2	**2.2V-5V Regulator**								
2.1	Regulated output voltage	V_{VBAT} > 9V I_{load} = 0 mA to 100 mA		VCC_1	4.85		5.15	V	
2.2	Regulated output voltage	6V < V_{VBAT} ≤ 9V I_{load} = 0 mA to 50 mA		VCC_2	4.5		5.5	V	
2.3	Line regulation	I_{load} = 0 mA to 100 mA		linereg			100	mV	
2.4	Load regulation	V_{VBAT} > 9V I_{load} = 0 mA to 100 mA		loadreg			100	mV	
2.5	Output current limitation(4)	V_{VBAT} > 9V		I_{OS1}	100		400	mA	
2.6	Output current limitation(4)	6V < V_{VBAT} ≤ 9V		I_{OS2}	50		400	mA	
2.7	Output current VREG	V_{VREG} = 5V, V_{VCC} = 0V, V_{VBAT} = 9V		I_{VREG}	3		20	mA	
2.8	ESR value of used blocking capacitor			R_{ESR}	0.3		3	Ω	
2.9	Blocking capacitor at VCC	Combination with HF capacitor of 100 nF		C_{VCC}	40			µF	
2.10	Current gain of external NPN			BN	25				
3	**Reset and Watchdog**								
3.1	VCC threshold voltage level for /RESET			V_{tHRESH}	4.2		4.6	V	
3.2	VCC threshold voltage level for /RESET			V_{tHRESL}	3.8		4.15	V	
3.3	Hysteresis of /RESET level			HYS_{RESth}		0.4(5)		V	
3.4	Length of pulse at /RESET pin	/RESET pulse triggered by watchdog, C_{CWD} = 1 nF R_{CWD} = 56 kΩ		t_{RES}	2.58		2.96	ms	

* Type: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. EN, DIR, PWM = HIGH
2. Internal band-gap voltage is valid for VBAT > 3V (not testable)
3. Valid for –40°C to +90°C
4. R_{SHUNT} = 1Ω
5. Tested during qualification only
6. For timing, see the formula in "Reset and Watchdog Management" on page 8. All times depend on external elements C_{CWD} and R_{CWD}, tolerances of these elements have to be added to the given tolerances in the above table
7. External parasitic capacitive load together with pull-up resistor at RX defines the time t_{RxH}
8. If single-ended mode is used (SEM = HIGH): DATA is not used and VBAT / 2 instead of DATA is the internal reference for parameters 4.10 and 4.11
9. Maximum voltage difference arises during slope, see Figure 7-1 on page 30
10. Parameters 4.16 to 4.19 are based on transmit voltage slopes at DATA and /DATA of 4V/µs ±50%

7. Electrical Characteristics (Continued)

All parameters given are valid for 7V ≤ VBAT ≤ 40V and for –40°C ≤ $\vartheta_{ambient}$ ≤ 125°C unless stated otherwise.
Conditions: SEM = HIGH (single-ended mode of SCI).

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
3.5	Delay time of release /RESET after VCC exceeding V_{tHRESH}	C_{CWD} = 1 nF R_{CWD} = 56 kΩ(6)		$t_{delayRESH}$	2.58		2.96	ms	
3.6	Time for VCC < V_{tHRESL} before activating /RESET	Independent of C_{CWD} and R_{CWD}		$t_{delayRESL}$	0.5		2	µs	
3.7	Watchdog oscillator period	C_{CWD} = 1 nF R_{CWD} = 56 kΩ(6)		t	60.4		68.8	µs	
3.8	Time for VCC > V_{tHRESH} before release of /RESET	C_{CWD} = 1 nF R_{CWD} = 56 kΩ(6)		$t_{delayRESH}$	2.6		3.0	ms	
3.9	First open watchdog window width after power-on	C_{CWD} = 1 nF R_{CWD} = 56 kΩ(6)		t_{ow1}	50.2		57.2	ms	
3.10	Open watchdog window width	C_{CWD} = 1 nF R_{CWD} = 56 kΩ(6)		t_{ow}	11.2		12.7	ms	
3.11	Closed watchdog window width	C_{CWD} = 1 nF R_{CWD} = 56 kΩ(6)		t_{CW}	11.2		12.7	ms	
3.12	External watchdog resistor			R_{CWD}	10		100	kΩ	
3.13	External watchdog capacitor			C_{CWD}	470		3300	pF	
3.14	Watchdog input low voltage threshold			V_{ILWD}			0.3 × V_{VCC}	V	
3.15	Watchdog input high voltage threshold			V_{IHWD}	0.7 × V_{VCC}			V	
3.16	Hysteresis of watchdog input voltage threshold			V_{hysWD}		1		V	
3.17	Pulse length of watchdog pulse for proper triggering	Measured between 50% levels		t_{WpL} / t_{WpH}	1000			ns	
3.18	Rise time of watchdog trigger pulse			t_{WDr}			100	ns	
3.19	Fall time of watchdog trigger pulse			t_{WDf}			100	ns	

* Type: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. EN, DIR, PWM = HIGH
2. Internal band-gap voltage is valid for VBAT > 3V (not testable)
3. Valid for –40°C to +90°C
4. R_{SHUNT} = 1Ω
5. Tested during qualification only
6. For timing, see the formula in "Reset and Watchdog Management" on page 8. All times depend on external elements C_{CWD} and R_{CWD}, tolerances of these elements have to be added to the given tolerances in the above table
7. External parasitic capacitive load together with pull-up resistor at RX defines the time t_{RxH}
8. If single-ended mode is used (SEM = HIGH): DATA is not used and VBAT / 2 instead of DATA is the internal reference for parameters 4.10 and 4.11
9. Maximum voltage difference arises during slope, see Figure 7-1 on page 30
10. Parameters 4.16 to 4.19 are based on transmit voltage slopes at DATA and /DATA of 4V/µs ±50%

7. Electrical Characteristics (Continued)

All parameters given are valid for 7V ≤ VBAT ≤ 40V and for –40°C ≤ $\vartheta_{ambient}$ ≤ 125°C unless stated otherwise.
Conditions: SEM = HIGH (single-ended mode of SCI).

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
3.20	Output low voltage of /RESET	At I_{OLRES} = 1 mA		V_{OLRES}			0.4	V	
3.21	Internal pull-up resistor at pin /RESET			R_{PURES}	5	10	15	kΩ	
3.22	Leakage current WD pin	V_{WD} = 0V to VCC		I_{leakWD}	–10		+10	µA	
4	**SCI Transceiver**								
4.1	Rx output voltage HIGH	I_{Rx} = 0		V_{RxH}	4.5		5.5	V	
4.2	Internal pull-up resistance to VCC	V_{Rx} = 0, driver set to HIGH		R_{RXH}	5	10	20	kΩ	
4.3	R_{DS_ON} of low-side driver transistor of RX output	Driver set to LOW		R_{RXL}		40	90	Ω	
4.4	Output HIGH delay time	See Figure 3-7 and Figure 3-8 on page 12(7)		t_{RxH}		0.5		µs	
4.5	Output LOW delay time	See Figure 3-7 and Figure 3-8 on page 12		t_{RxL}		0.5		µs	
4.6	Tx input LOW level			V_{TxL}			0.3 × V_{VCC}	V	
4.7	Tx input HIGH level			V_{TxH}	0.7 × V_{VCC}			V	
4.8	Input hysteresis Tx	(5)		V_{hysTx}		1		V	
4.9	Internal pull-up resistance to VCC			R_{TXH}	10	20	40	kΩ	
4.10	Input high voltage difference between DATA and /DATA	(8)		V_{RDATH}			5% of V_{VBAT}	V	
4.11	Input low voltage difference between DATA and /DATA	(8)		V_{RDATL}	–5% of V_{VBAT}			V	
4.12	Hysteresis between V_{DATH} and V_{DATL}	(5)		V_{DAThys}		5% of V_{VBAT}		V	

* Type: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. EN, DIR, PWM = HIGH
2. Internal band-gap voltage is valid for VBAT > 3V (not testable)
3. Valid for –40°C to +90°C
4. R_{SHUNT} = 1Ω
5. Tested during qualification only
6. For timing, see the formula in "Reset and Watchdog Management" on page 8. All times depend on external elements C_{CWD} and R_{CWD}, tolerances of these elements have to be added to the given tolerances in the above table
7. External parasitic capacitive load together with pull-up resistor at RX defines the time t_{RxH}
8. If single-ended mode is used (SEM = HIGH): DATA is not used and VBAT / 2 instead of DATA is the internal reference for parameters 4.10 and 4.11
9. Maximum voltage difference arises during slope, see Figure 7-1 on page 30
10. Parameters 4.16 to 4.19 are based on transmit voltage slopes at DATA and /DATA of 4V/µs ±50%

7. Electrical Characteristics (Continued)

All parameters given are valid for 7V ≤ VBAT ≤ 40V and for –40°C ≤ $\vartheta_{ambient}$ ≤ 125°C unless stated otherwise.
Conditions: SEM = HIGH (single-ended mode of SCI).

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
4.13	Output HIGH voltage pin DATA	TX = LOW, I_{DATA} = –20 mA		$V_{TDATAH1}$	V_{VBAT} – 1.2			V	
4.14	Output HIGH voltage pin DATA	TX = LOW, I_{DATA} = –40 mA		$V_{TDATAH2}$	V_{VBAT} – 1.5			V	
4.15	Output LOW voltage pin /DATA	TX = LOW, $I_{/DATA}$ = 20 mA		$V_{T/DATAL1}$			1.2	V	
4.16	Output LOW voltage pin /DATA	TX = LOW, $I_{/DATA}$ = 40 mA		$V_{T/DATAL2}$			1.5	V	
4.17	Short-circuit current /DATA			$I_{/DATASC}$	40	75	150	mA	
4.18	Short-circuit current DATA			I_{DATASC}	–40	–75	–150	mA	
4.19	SEM input LOW level			V_{SEML}			0.3 × V_{VCC}	V	
4.20	SEM input HIGH level			V_{SEMH}	0.7 × V_{VCC}			V	
4.21	Input hysteresis SEM	(5)		V_{hysSEM}		1		V	
4.22	Internal pull-up resistance to VCC			R_{SEM}	10	20	40	kΩ	
4.23	Transmit delay HIGH to LOW(10)	V_{VBAT} = 13.5V		t_{SCL}	0	1	1.5	µs	
4.24	Transmit fall time(10)	V_{VBAT} = 13.5V		t_{SCf}	1.5		4.1	µs	
4.25	Transmit delay LOW to HIGH(10)	V_{VBAT} = 13.5V		t_{SCH}	0	1	1.5	µs	
4.26	Transmit rise time(10)	V_{VBAT} = 13.5V		t_{SCr}	1.5		4.1	µs	
4.27	Activation voltage on /DATA of SCI receive part			$V_{/DATwake}$			V_{VBAT} – 2	V	
4.28	Input current pin DATA for passive transmit	–2V < V_{DATA} < V_{VBAT} – 2V		I_{DATA1}	–20		+20	µA	
4.29	Filter time for wake-up via SCI			$t_{wakeSCI}$	30		80	µs	
4.30	Input current pin DATA for passive transmit	V_{DATA} ≥ V_{VBAT} – 0.5		I_{DATA2}			500	µA	

* Type: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. EN, DIR, PWM = HIGH
2. Internal band-gap voltage is valid for VBAT > 3V (not testable)
3. Valid for –40°C to +90°C
4. R_{SHUNT} = 1Ω
5. Tested during qualification only
6. For timing, see the formula in "Reset and Watchdog Management" on page 8. All times depend on external elements C_{CWD} and R_{CWD}, tolerances of these elements have to be added to the given tolerances in the above table
7. External parasitic capacitive load together with pull-up resistor at RX defines the time t_{RxH}
8. If single-ended mode is used (SEM = HIGH): DATA is not used and VBAT / 2 instead of DATA is the internal reference for parameters 4.10 and 4.11
9. Maximum voltage difference arises during slope, see Figure 7-1 on page 30
10. Parameters 4.16 to 4.19 are based on transmit voltage slopes at DATA and /DATA of 4V/µs ±50%

7. Electrical Characteristics (Continued)

All parameters given are valid for 7V ≤ VBAT ≤ 40V and for –40°C ≤ $\vartheta_{ambient}$ ≤ 125°C unless stated otherwise.
Conditions: SEM = HIGH (single-ended mode of SCI).

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
4.31	Input current pin /DATA for passive transmit	–2V < $V_{/DATA}$ < V_{VBAT} + 2V		$I_{/DATA}$	–20		+20	µA	
4.32	Symmetry of DATA and /DATA during transmit	V_{VBAT} = 13.5V[9]		V_{SYM}		2.5		V	
5	**Control Inputs EN, DIR, PWM**								
5.1	Enable input low-voltage threshold			V_{ILEN}			2	V	
5.2	Enable input high-voltage threshold			V_{IHEN}	3.5			V	
5.3	Hysteresis of EN switching level	Tested during characterization only		HYS_{ENth}		0.7		V	
5.4	Pull-down resisistor at Enable pin			R_{PDEN}	30		100	kΩ	
5.5	DIR input low-voltage threshold			V_{ILDIR}			0.3 × V_{VCC}	V	
5.6	DIR input high-voltage threshold			V_{IHDIR}	0.7 × V_{VCC}			V	
5.7	Hysteresis of DIR switching level	Tested during characterization only		HYS_{DIRth}		1		V	
5.8	Pull-down resisistor at DIR pin			R_{PDDIR}	30		100	kΩ	
5.9	PWM input low-voltage threshold			V_{ILPWM}			0.3 × V_{VCC}	V	
5.10	PWM input high-voltage threshold			V_{IHPWM}	0.7 × V_{VCC}			V	
5.11	Hysteresis of PWM switching level	Tested during characterization only		HYS_{PWMth}		1		V	
5.12	Pull-down resisistor at PWM pin			R_{PDPWM}	30		100	kΩ	
5.13	Rise/fall time, pin EN			t_{rf_EN}			100	ns	
5.14	Rise/fall time, pin PWM			t_{rf_PWM}			100	ns	

* Type: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. EN, DIR, PWM = HIGH
2. Internal band-gap voltage is valid for VBAT > 3V (not testable)
3. Valid for –40°C to +90°C
4. R_{SHUNT} = 1Ω
5. Tested during qualification only
6. For timing, see the formula in "Reset and Watchdog Management" on page 8. All times depend on external elements C_{CWD} and R_{CWD}, tolerances of these elements have to be added to the given tolerances in the above table
7. External parasitic capacitive load together with pull-up resistor at RX defines the time t_{RxH}
8. If single-ended mode is used (SEM = HIGH): DATA is not used and VBAT / 2 instead of DATA is the internal reference for parameters 4.10 and 4.11
9. Maximum voltage difference arises during slope, see Figure 7-1 on page 30
10. Parameters 4.16 to 4.19 are based on transmit voltage slopes at DATA and /DATA of 4V/µs ±50%

7. Electrical Characteristics (Continued)

All parameters given are valid for 7V ≤ VBAT ≤ 40V and for –40°C ≤ $\vartheta_{ambient}$ ≤ 125°C unless stated otherwise.
Conditions: SEM = HIGH (single-ended mode of SCI).

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
5.15	Rise/fall time, pin DIR			t_{rf_DIR}			100	ns	
5.16	Delay time for “Go to Active” by Enable			t_{delON_EN}	30		80	µs	
5.17	Delay time for “Go to Sleep” by Enable			$t_{gotosleep}$	30		80	µs	
6	**Charge Pump**								
6.1	Charge pump voltage	7V ≤ V_{VBAT} ≤ 9V		VCP	V_{VBAT} + 7		V_{VBAT} + 14	V	
6.2	Charge pump voltage	V_{VBAT} > 9V		VCP	V_{VBAT} + 8		V_{VBAT} + 14	V	
6.3	Charge pump current driving capability under valid parameters 6.1/6.2			I_{CP}	50			µA	
6.4	Charge pump oscillator frequency			f_{cposc}		2.2		MHz	
6.5	Serial resistance between charge pump and gate of external reverse battery protection NMOS			R_{CP}		10		kΩ	
6.6	Charge pump voltage in case of EN = 0	EN = “0” (Sleep mode)		VCP_{sleep}		V_{VBAT} – 0.7V			
7	**H-bridge Driver**								
7.1	Low-side driver HIGH output voltage	6V< V_{VBAT} ≤ 9V		V_{LxH1}	V_{VBAT} – 1		16	V	
7.2	Low-side driver HIGH output voltage	V_{VBAT} > 9V (with V_{VBAT} > 25V drivers may be switched off)		V_{LxH2}	8		16	V	
7.3	ON resistance of sink stage of pins L1, L2			R_{DSON_LxL}, x = 1,2			20	Ω	
7.4	ON resistance of source stage of pins L1, L2	Related to pin CBx		R_{DSON_LxH}, x = 1,2			30	Ω	

* Type: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. EN, DIR, PWM = HIGH
2. Internal band-gap voltage is valid for VBAT > 3V (not testable)
3. Valid for –40°C to +90°C
4. R_{SHUNT} = 1Ω
5. Tested during qualification only
6. For timing, see the formula in “Reset and Watchdog Management” on page 8. All times depend on external elements C_{CWD} and R_{CWD}, tolerances of these elements have to be added to the given tolerances in the above table
7. External parasitic capacitive load together with pull-up resistor at RX defines the time t_{RxH}
8. If single-ended mode is used (SEM = HIGH): DATA is not used and VBAT / 2 instead of DATA is the internal reference for parameters 4.10 and 4.11
9. Maximum voltage difference arises during slope, see Figure 7-1 on page 30
10. Parameters 4.16 to 4.19 are based on transmit voltage slopes at DATA and /DATA of 4V/µs ±50%

7. Electrical Characteristics (Continued)

All parameters given are valid for 7V ≤ VBAT ≤ 40V and for –40°C ≤ $\vartheta_{ambient}$ ≤ 125°C unless stated otherwise.
Conditions: SEM = HIGH (single-ended mode of SCI).

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
7.5	Output peak current at pins L1, L2 switched to LOW	V_{Lx} = 3V		I_{LxL}, x = 1,2	100			mA	
7.6	Output peak current at pins L1, L2 switched to HIGH	V_{Lx} = 3V		I_{LxH}, x = 1,2			–100	mA	
7.7	Pull-down resistance at pins L1, L2			R_{PDLx}, x = 1,2	30		100	kΩ	
7.8	ON resistance of sink stage of pins H1, H2	V_{Sx} = 0		R_{DSON_HxL}, x = 1,2			20	Ω	
7.9	ON resistance of source stage of pins H1, H2	Related to pin CBx, $V_{Sx} = V_{VBAT}$		R_{DSON_HxH}, x = 1,2			30	Ω	
7.10	Output peak current at pins Hx, switched to LOW	V_{VBAT} = 13.5V $V_{Sx} = V_{VBAT}$ $V_{CBx} = V_{VBAT}$ + 7V $V_{Hx} = V_{VBAT}$ + 3V		I_{HxL}, x = 1,2	100			mA	
7.11	Output peak current at pins Hx, switched to HIGH	V_{VBAT} = 13.5V $V_{Sx} = V_{VBAT}$ $V_{CBx} = V_{VBAT}$ + 7V $V_{Hx} = V_{VBAT}$ + 3V		I_{HxH}, x = 1,2			–100	mA	
7.12	Static high-side switch output low-voltage pins Hx	V_{Sx} = 0V I_{Hx} = 1 mA		V_{HxL}, x = 1,2			0.3	V	
7.13	Static high-side switch output high-voltage pins H1, H2	I_{Lx} = –10 µA (PWM = static) 7V ≤ V_{VBAT} ≤ 9V		$V_{HxHstat1}$ (supplied by charge pump)	V_{VBAT} + 7		V_{VBAT} + 14	V	
7.14	Static high-side switch output high-voltage pins H1, H2	I_{Lx} = –10 µA (PWM = static) V_{VBAT} > 9V (with V_{VBAT} > 25V, drivers may be switched off)		$V_{HxHstat1}$ (supplied by charge pump)	V_{VBAT} + 8		V_{VBAT} + 14	V	
7.15	Sink resistance between Hx and Ground in Sleep mode			$R_{Hxsleep}$	3		10	kΩ	

* Type: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. EN, DIR, PWM = HIGH
2. Internal band-gap voltage is valid for VBAT > 3V (not testable)
3. Valid for –40°C to +90°C
4. R_{SHUNT} = 1Ω
5. Tested during qualification only
6. For timing, see the formula in "Reset and Watchdog Management" on page 8. All times depend on external elements C_{CWD} and R_{CWD}, tolerances of these elements have to be added to the given tolerances in the above table
7. External parasitic capacitive load together with pull-up resistor at RX defines the time t_{RxH}
8. If single-ended mode is used (SEM = HIGH): DATA is not used and VBAT / 2 instead of DATA is the internal reference for parameters 4.10 and 4.11
9. Maximum voltage difference arises during slope, see Figure 7-1 on page 30
10. Parameters 4.16 to 4.19 are based on transmit voltage slopes at DATA and /DATA of 4V/µs ±50%

7. Electrical Characteristics (Continued)

All parameters given are valid for 7V ≤ VBAT ≤ 40V and for –40°C ≤ $\vartheta_{ambient}$ ≤ 125°C unless stated otherwise.
Conditions: SEM = HIGH (single-ended mode of SCI).

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
7.16	Voltage at pin Sx for open pin if Hx and Lx are both switched off	I_{sx} = 0		V_{SxOFF}			2	V	
7.17	CB1 voltage for H1 = OFF	V_{VBAT} = 6V		V_{CB1}	5		14	V	
7.18	CB1 voltage for H1 = OFF	V_{VBAT} = 8V		V_{CB1}	7		14	V	
7.19	CB1 voltage for H1 = OFF	V_{VBAT} = 10V		V_{CB1}	9		14	V	
7.20	CB1 voltage for H1 = OFF	V_{VBAT} = 25V		V_{CB1}	9		14	V	
7.21	CB2 voltage for H2 = OFF	V_{VBAT} = 6V		V_{CB2}	5		14	V	
7.22	CB2 voltage for H2 = OFF	V_{VBAT} = 8V		V_{CB2}	7		14	V	
7.23	CB2 voltage for H2 = OFF	V_{VBAT} = 10V		V_{CB2}	9		14	V	
7.24	CB2 voltage for H2 = OFF	V_{VBAT} = 25V		V_{CB2}	9		14	V	
	Dynamic Parameters								
7.14	Dynamic high-side switch output for high-voltage pins H1, H2 (bootstrap voltage)	C_{Hx} = 5 nF C_{CBx} = 100 nF f_{PWM} = 20 kHz V_{VBAT} = 6V		$V_{HxHdyn1}$	V_{VBAT} + 4.5		V_{VBAT} + 14	V	
7.15	Dynamic high-side switch output for high-voltage pins H1, H2 (bootstrap voltage)	C_{Hx} = 5 nF C_{CBx} = 100 nF f_{PWM} = 20 kHz V_{VBAT} = 8V		$V_{HxHdyn2}$	V_{VBAT} + 6		V_{VBAT} + 14	V	
7.16	Dynamic high-side switch output for high-voltage pins H1, H2 (bootstrap voltage)	C_{Hx} = 5nF C_{CBx} = 100 nF f_{PWM} = 20 kHz V_{VBAT} ≥ 10V		$V_{HxHdyn3}$	V_{VBAT} + 8		V_{VBAT} + 14	V	
7.17	Propagation delay time for low-side driver from HIGH to LOW	V_{VBAT} = 13.5V C_{CBx} = 100 nF Figure 3-9 on page 17		t_{LxHL}			0.5	µs	
7.18	Propagation delay time for low-side driver from LOW to HIGH			t_{LxLH}			0.5 + t_{CC}	µs	
7.19	Fall time for low-side driver	V_{VBAT} = 13.5V C_{Gx} = 5 nF		t_{Lxf}			0.5	µs	

* Type: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. EN, DIR, PWM = HIGH
2. Internal band-gap voltage is valid for VBAT > 3V (not testable)
3. Valid for –40°C to +90°C
4. R_{SHUNT} = 1Ω
5. Tested during qualification only
6. For timing, see the formula in "Reset and Watchdog Management" on page 8. All times depend on external elements C_{CWD} and R_{CWD}, tolerances of these elements have to be added to the given tolerances in the above table
7. External parasitic capacitive load together with pull-up resistor at RX defines the time t_{RxH}
8. If single-ended mode is used (SEM = HIGH): DATA is not used and VBAT / 2 instead of DATA is the internal reference for parameters 4.10 and 4.11
9. Maximum voltage difference arises during slope, see Figure 7-1 on page 30
10. Parameters 4.16 to 4.19 are based on transmit voltage slopes at DATA and /DATA of 4V/µs ±50%

7. Electrical Characteristics (Continued)

All parameters given are valid for 7V ≤ VBAT ≤ 40V and for –40°C ≤ $\vartheta_{ambient}$ ≤ 125°C unless stated otherwise.
Conditions: SEM = HIGH (single-ended mode of SCI).

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
7.20	Rise time for low-side driver			t_{Lxr}			0.5	µs	
7.21	Propagation delay time for high-side driver from HIGH to LOW	V_{VBAT} = 13.5V C_{CBx} = 100 nF Figure 3-9 on page 17		t_{HxHL}			0.5	µs	
7.22	Propagation delay time for high-side driver from LOW to HIGH			t_{HxLH}			0.5 + t_{CC}	µs	
7.23	Fall time for high-side driver	V_{VBAT} = 13.5V C_{Gx} = 5 nF		t_{Hxf}			0.5	µs	
7.24	Rise time for high-side driver			t_{Hxr}			0.5	µs	
7.25	Cross conduction time	See "Cross Conduction Time" on page 16		t_{CC}			10	µs	
7.26	External resistor			R_{CC}	5			kΩ	
7.27	External capacitor			C_{CC}			5	nF	
7.28	R_{ON} of t_{CC} switching transistor			R_{ONCC}			100	Ω	
7.29	Switching level of t_{CC} comparator			V_{swtcc}	3.2 × V_{VCC}	3.4 × V_{VCC}	3.6 × V_{VCC}	V	
7.30	Short circuit detection voltage	Voltage between source-drain of external switching transistor in active case		V_{SC}	3.5	4	4.5	V	

* Type: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. EN, DIR, PWM = HIGH
2. Internal band-gap voltage is valid for VBAT > 3V (not testable)
3. Valid for –40°C to +90°C
4. R_{SHUNT} = 1Ω
5. Tested during qualification only
6. For timing, see the formula in "Reset and Watchdog Management" on page 8. All times depend on external elements C_{CWD} and R_{CWD}, tolerances of these elements have to be added to the given tolerances in the above table
7. External parasitic capacitive load together with pull-up resistor at RX defines the time t_{RxH}
8. If single-ended mode is used (SEM = HIGH): DATA is not used and VBAT / 2 instead of DATA is the internal reference for parameters 4.10 and 4.11
9. Maximum voltage difference arises during slope, see Figure 7-1 on page 30
10. Parameters 4.16 to 4.19 are based on transmit voltage slopes at DATA and /DATA of 4V/µs ±50%

7. Electrical Characteristics (Continued)

All parameters given are valid for 7V ≤ VBAT ≤ 40V and for –40°C ≤ $\vartheta_{ambient}$ ≤ 125°C unless stated otherwise.
Conditions: SEM = HIGH (single-ended mode of SCI).

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
7.31	Short circuit detection time	For switch-on time < t_{sc}, the short circuit message will never be generated		t_{SC}	5	10	15	µs	
7.32	Charging time for bootstrap capacitors	Time for Lx = ON (plus cross conduction time if inductive load is applied), this time limits the PWM ratio to values of about 95% if 20 kHz is used		t_{CHBOOT}	1.3			µs	
7.33	Maximum PWM frequency			f_{PWMmax}			30	kHz	

* Type: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. EN, DIR, PWM = HIGH
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7. External parasitic capacitive load together with pull-up resistor at RX defines the time t_{RxH}
8. If single-ended mode is used (SEM = HIGH): DATA is not used and VBAT / 2 instead of DATA is the internal reference for parameters 4.10 and 4.11
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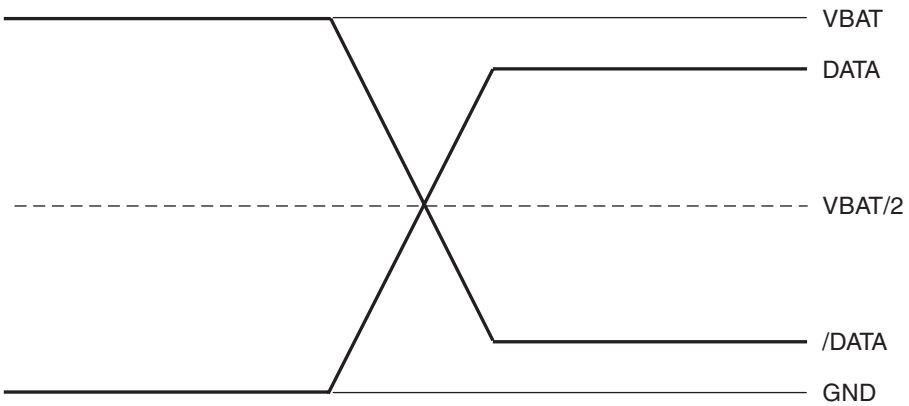
10. Parameters 4.16 to 4.19 are based on transmit voltage slopes at DATA and /DATA of 4V/µs ±50%

Figure 7-1. Principal Dynamic Behavior of SCI, V_{SYM} is the Symmetry of DATA and /DATA to VBAT / 2



V_{SYM} = (VBAT – /DATA) – DATA, ideally it should always be 0

8. ESD and Latch-up Requirements

The device withstands pulses when tested according to ESD STM 5.1-1998:

- Constant voltage 2 kV
- R = 1.5 kΩ
- C = 100 pF
- 1 pulse per polarity and per pin
- 3 samples, 0 failures
- Electrical post-stress testing at room temperature

Static latch-up tested according to AEC-Q100-004 and JESD78.

- 3-6 samples, 0 failures
- Electrical post-stress testing at room temperature

In test, the voltage at the pins VBAT, DATA, /DATA, CP, VBAT_SWITCH, Hx, Sx, CBx must not exceed 45V in case of not being able to drive the specified current; for the pins Lx the voltage must not exceed 25V.

9. Ordering Information

Extended Type Number	Package	Remarks
ATA6026-PHQW	QFN32, 7 mm × 7 mm	Pb-free

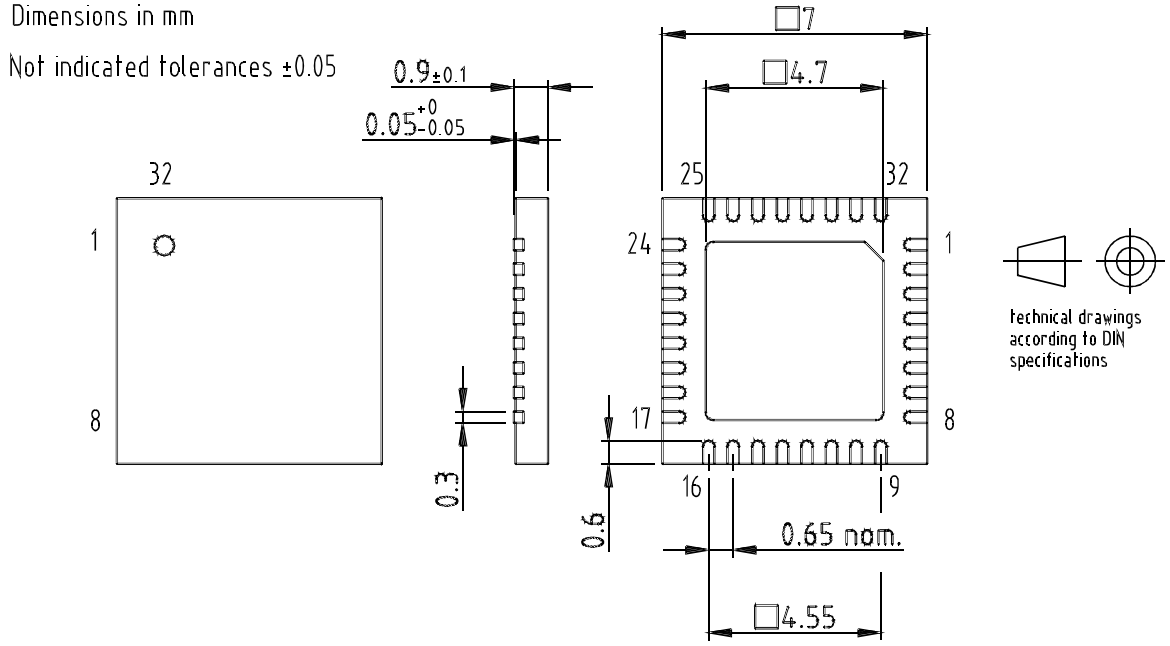
10. Package Information

Package: QFN 32 7x7

Exposed pad 4.7 x 4.7

Dimensions in mm

Not indicated tolerances ±0.05



Drawing-No.: 6.543-5097.01-4

Issue: 1; 24.02.03

Thermal resistance junction ambient: 29 K/W (at airflow of 0 LFPM), valid for JEDEC Standard Four-layer Thermal Test Board with 5 x 5 Thermal Via Matrix (100 µm Drill Hole, Filled Vias).

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