

Features

- EE Programmable 262,144 x 1-, 524,288 x 1-, 1,048,576 x 1-, 2,097,152 x 1-, and 4,194,304 x 1-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)
- Available as a 3.3V ($\pm 10\%$) Commercial and Industrial Version
- Simple Interface to SRAM FPGAs
- Pin Compatible with Xilinx[®] XC17SXXXA and XC17SXXXXL PROMs
- Compatible with Xilinx Spartan[®]-II, Spartan-IIe and Spartan XL FPGAs in Master Serial Mode
- Very Low-power CMOS EEPROM Process
- Available in 6 mm x 6 mm x 1 mm 8-lead LAP (Pin-compatible with 8-lead SOIC/VOIC Packages), 8-lead PDIP, 8-lead SOIC, 20-lead SOIC and 44-lead TQFP Packages for a Specific Density
- Low-power Standby Mode
- High-reliability
 - Endurance: Minimum 10 Write Cycles
 - Data Retention: 20 Years at 85°C

Description

The AT17N series FPGA Configuration EEPROM (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The AT17N series device is packaged in the 8-lead LAP, 8-lead PDIP, 8-lead SOIC, 20-lead SOIC and 44-lead TQFP, see Table 1. The AT17N series Configurators uses a simple serial-access procedure to configure one or more FPGA devices.

The AT17N series configurators can be programmed with industry-standard programmers, Atmel's ATDH2200E Programming Kit or Atmel's ATDH2225 ISP Cable and factory programming.

Table 1. AT17N Series Packages

| Package | AT17N256 | AT17N512/ AT17N010 | AT17N002 | AT17N040 |
|--------------|----------|-------------------------------|-------------------------------|----------|
| 8-lead LAP | – | Yes | Yes | – |
| 8-lead PDIP | Yes | Yes | – | – |
| 8-lead SOIC | Yes | Use 8-lead LAP ⁽¹⁾ | Use 8-lead LAP ⁽¹⁾ | – |
| 20-lead SOIC | Yes | Yes | Yes | – |
| 44-lead TQFP | – | – | Yes | Yes |

Note: 1. The 8-lead LAP package has the same footprint as the 8-lead SOIC. Since an 8-lead SOIC package is not available for the AT17N512/010/002 devices, it is possible to use an 8-lead LAP package instead.



FPGA Configuration Memory

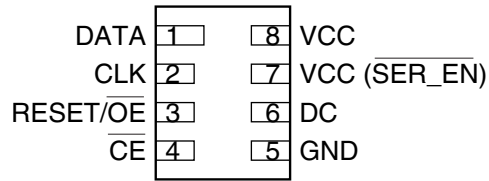
AT17N256
AT17N512
AT17N010
AT17N002
AT17N040

3.3V System Support

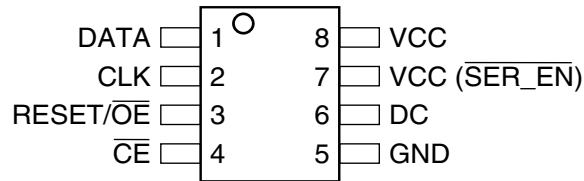


Pin Configuration

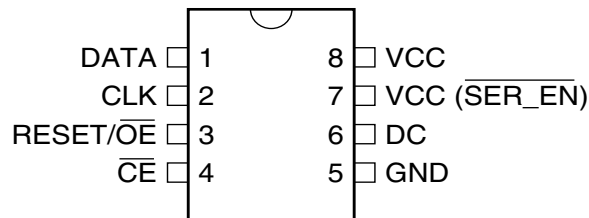
8-lead LAP



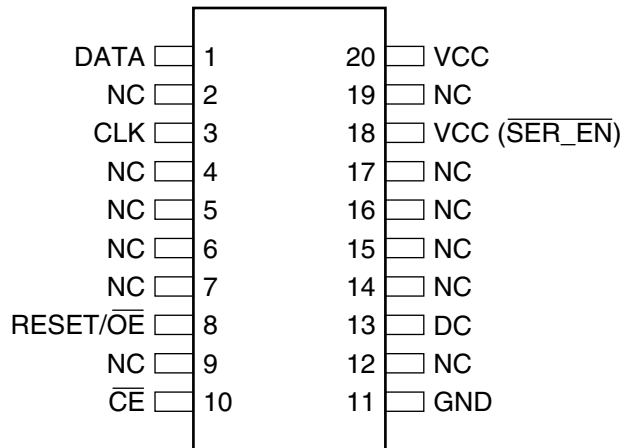
8-lead SOIC



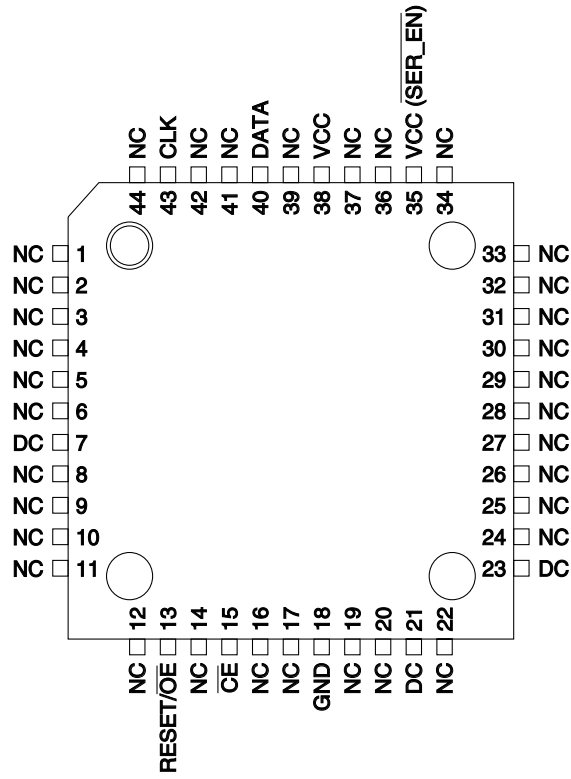
8-lead PDIP



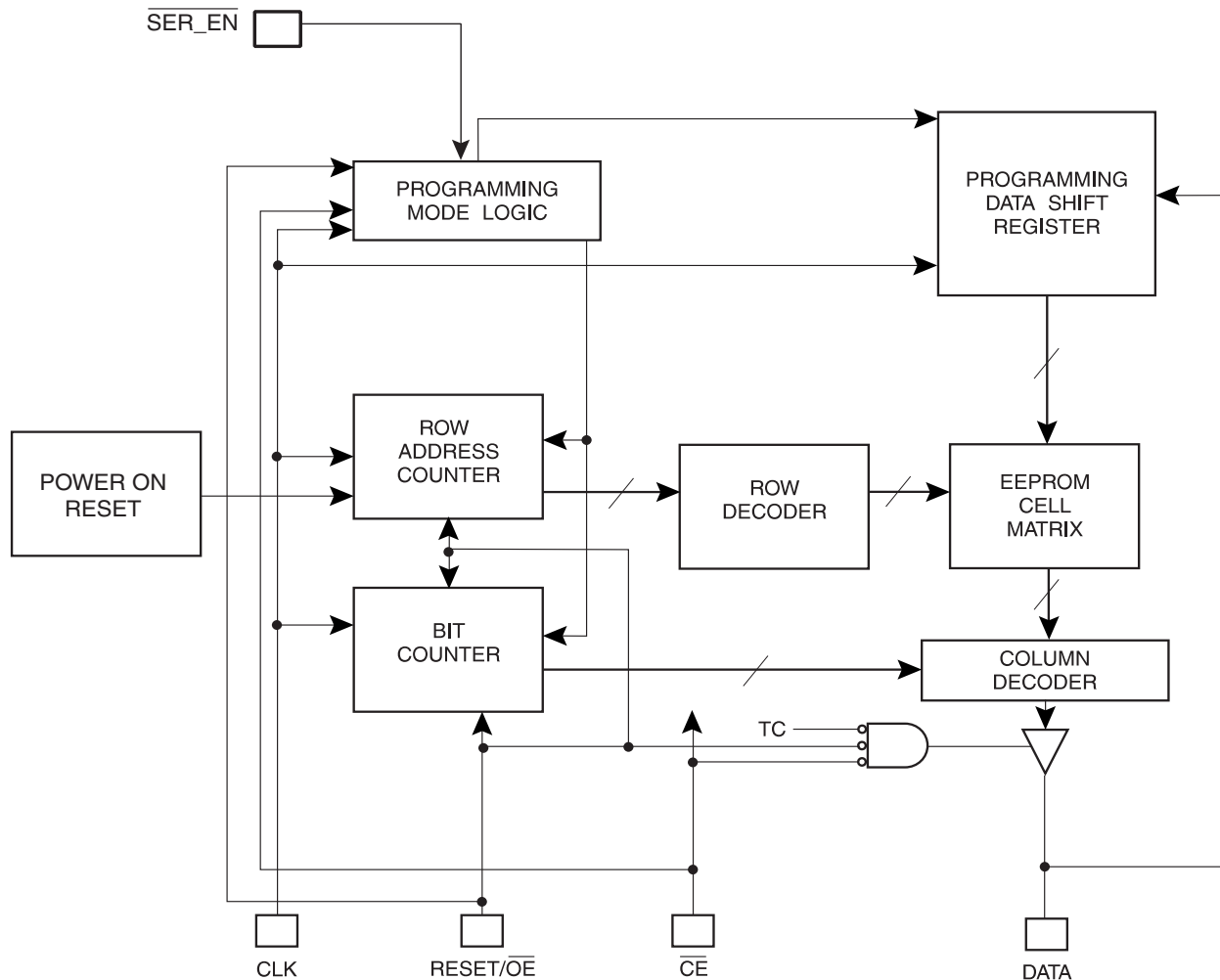
20-lead SOIC



44 TQFP



Block Diagram



Device Description

The control signals for the configuration EEPROM (\overline{CE} , $\overline{RESET/OE}$ and $CCLK$) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration EEPROM without requiring an external intelligent controller.

The configuration EEPROM $\overline{RESET/OE}$ and \overline{CE} pins control the tri-state buffer on the DATA output pin and enable the address counter. When $\overline{RESET/OE}$ is driven High, the configuration EEPROM resets its address counter and tri-states its DATA pin. The \overline{CE} pin also controls the output of the AT17N series configurator. If \overline{CE} is held High after the $\overline{RESET/OE}$ reset pulse, the counter is disabled and the DATA output pin is tri-stated. When \overline{OE} is subsequently driven Low, the counter and the DATA output pin are enabled. When $\overline{RESET/OE}$ is driven High again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of \overline{CE} . Upon power-up, the address counter is automatically reset.

Pin Description

| Name | I/O | AT17N256 | | AT17N512/ AT17N010 | | AT17N002 | | | AT17N040 |
|-----------------------------|-----|-------------------|------------|-----------------------|------------|----------|------------|------------|------------|
| | | 8 DIP/ SOIC | 20 SOIC | 8 DIP/ LAP | 20 SOIC | 8 LAP | 20 SOIC | 44 TQFP | 44 TQFP |
| DATA | I/O | 1 | 1 | 1 | 1 | 1 | 1 | 40 | 40 |
| CLK | I | 2 | 3 | 2 | 3 | 2 | 3 | 43 | 43 |
| RESET/ \overline{OE} | I | 3 | 8 | 3 | 8 | 3 | 8 | 13 | 13 |
| \overline{CE} | I | 4 | 10 | 4 | 10 | 4 | 10 | 15 | 15 |
| GND | | 5 | 11 | 5 | 11 | 5 | 11 | 18 | 18 |
| DC | O | 6 | 13 | 6 | 13 | 6 | 13 | 21 | 21 |
| DC | O | – | – | – | – | – | – | 23 | 23 |
| VCC($\overline{SER_EN}$) | I | 7 | 18 | 7 | 18 | 7 | 18 | 35 | 35 |
| V _{CC} | | 8 | 20 | 8 | 20 | 8 | 20 | 38 | 38 |

DATA

Three-state DATA output for configuration. Open-collector bi-directional pin for programming.

CLK

Clock input. Used to increment the internal address and bit counter for reading and programming.

RESET/ \overline{OE}

Output Enable (active High) and RESET (active Low) when $\overline{SER_EN}$ is High. A Low level on RESET/OE resets both the address and bit counters. A High level (with \overline{CE} Low) enables the data output driver. The logic polarity of this input is programmable as either RESET/ \overline{OE} or $\overline{RESET/OE}$. For most applications, RESET should be programmed active Low. This document describes the pin as RESET/OE.

\overline{CE}

Chip Enable input (active Low). A Low level (with OE High) allows CLK to increment the address counter and enables the data output driver. A High level on \overline{CE} disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will *not* enable/disable the device in the Two-Wire Serial Programming mode ($\overline{SER_EN}$ Low).

GND

Ground pin. A 0.2 μ F decoupling capacitor between V_{CC} and GND is recommended.

VCC($\overline{SER_EN}$)

Serial enable must be held High during FPGA loading operations. Bringing $\overline{SER_EN}$ Low enables the Two-Wire Serial Programming Mode. For non-ISP applications, $\overline{SER_EN}$ should be tied to V_{CC}.

V_{CC}

3.3V ($\pm 10\%$) Commercial and Industrial power supply pin.

NC

NC pins are No Connect pins, which are not internally bonded out to the die.

DC

DC pins are No Connect pins internally connected to the die. It is not recommended to connect these pins to any external signal.

FPGA Master Serial Mode Summary

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master mode, the FPGA automatically loads the configuration program from an external memory. The AT17N Serial Configuration EEPROM has been designed for compatibility with the Master Serial mode.

This document discusses the master serial mode configuration of Atmel AT17N series configuration memories, pin compatible with Spartan-II, Spartan-IIe and Spartan XL OTP PROMs.

Control of Configuration

Most connections between the FPGA device and the AT17N Serial EEPROM are simple and self-explanatory.

- The DATA output of the AT17N series configurator drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17N series configurator.
- $\overline{\text{SER_EN}}$ must be connected to V_{CC} (except during ISP).
- The $\overline{\text{CE}}$ and $\text{OE}/\overline{\text{Reset}}$ are driven by the FPGA to enable output data buffer of the EEPROM.

Programming Mode

The programming mode is entered by bringing $\overline{\text{SER_EN}}$ Low. In this mode the chip can be programmed by the Two-Wire serial bus. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip.

Standby Mode

The AT17N series configurators enter a low-power standby mode whenever $\overline{\text{CE}}$ is asserted High. In this mode, the AT17N256 configurator consumes less than 50 μA of current at 3.3V (100 μA for the AT17N512/010 and 200 μA for the AT17N002/040).

Absolute Maximum Ratings*

| | |
|---|--------------------------|
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -0.1V to $V_{CC} + 0.5V$ |
| Supply Voltage (V_{CC}) | 3.0V to +3.6V |
| Maximum Soldering Temp. (10 sec. @ 1/16 in.)..... | 260°C |
| ESD ($R_{ZAP} = 1.5K, C_{ZAP} = 100 \text{ pF}$)..... | 2000V |

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Conditions

| Symbol | Description | | 3.3V | | Units |
|----------|-------------|--|------|-----|-------|
| | | | Min | Max | |
| V_{CC} | Commercial | Supply voltage relative to GND -0°C to +70°C | 3.0 | 3.6 | V |
| | Industrial | Supply voltage relative to GND -40°C to +85°C | 3.0 | 3.6 | V |



DC Characteristics

$$V_{CC} = 3.3V \pm 10\%$$

| Symbol | Description | AT17N256 | | AT17N512/ AT17N010 | | AT17N002/ AT17N040 | | Units |
|-----------|--|------------|----------|-----------------------|----------|-----------------------|----------|---------|
| | | Min | Max | Min | Max | Min | Max | |
| V_{IH} | High-level Input Voltage | 2.0 | V_{CC} | 2.0 | V_{CC} | 2.0 | V_{CC} | V |
| V_{IL} | Low-level Input Voltage | 0 | 0.8 | 0 | 0.8 | 0 | 0.8 | V |
| V_{OH} | High-level Output Voltage ($I_{OH} = -2.5$ mA) | 2.4 | | 2.4 | | 2.4 | | V |
| V_{OL} | Low-level Output Voltage ($I_{OL} = +3$ mA) | | | | | | | |
| V_{OH} | High-level Output Voltage ($I_{OH} = -2$ mA) | 2.4 | | 2.4 | | 2.4 | | V |
| V_{OL} | Low-level Output Voltage ($I_{OL} = +3$ mA) | | | | | | | |
| I_{CCA} | Supply Current, Active Mode | | 5 | | 5 | | 5 | mA |
| I_L | Input or Output Leakage Current ($V_{IN} = V_{CC}$ or GND) | -10 | 10 | -10 | 10 | -10 | 10 | μ A |
| I_{CCS} | Supply Current, Standby Mode | Commercial | 50 | | 100 | | 150 | μ A |
| | | Industrial | 100 | | 100 | | 150 | μ A |

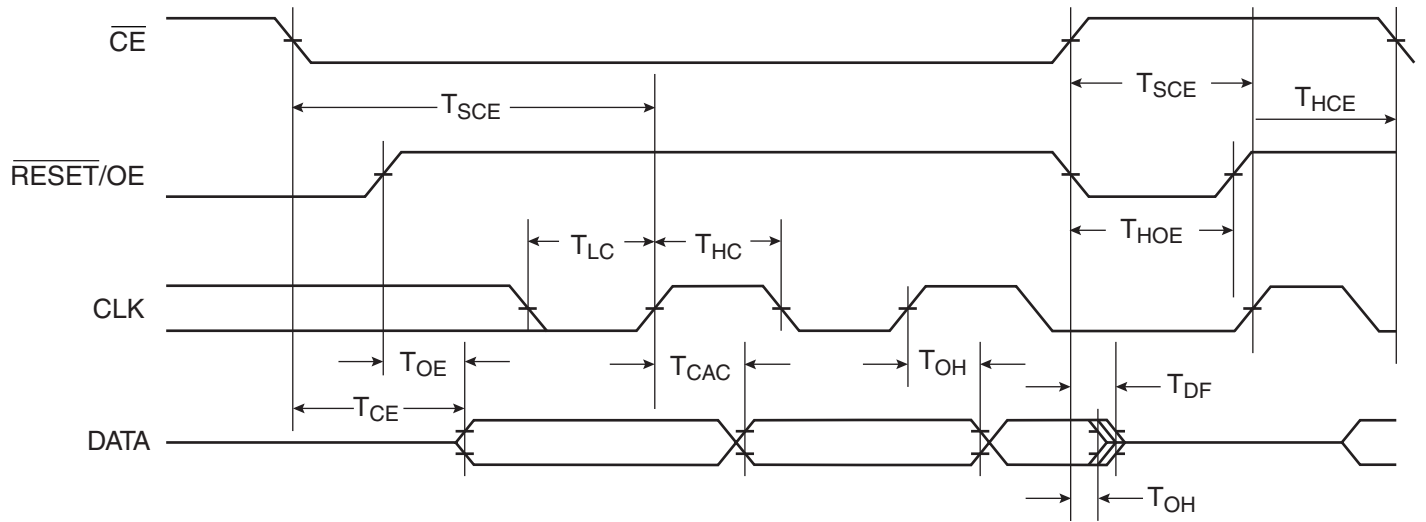
AC Characteristics

$$V_{CC} = 3.3V \pm 10\%$$

| Symbol | Description | AT17N256 | | | | AT17N512/010/002/040 | | | | Units |
|-----------------|--|------------|-----|------------|-----|----------------------|-----|------------|-----|-------|
| | | Commercial | | Industrial | | Commercial | | Industrial | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $T_{OE}^{(1)}$ | OE to Data Delay | | 50 | | 55 | | 50 | | 55 | ns |
| $T_{CE}^{(1)}$ | \overline{CE} to Data Delay | | 60 | | 60 | | 55 | | 60 | ns |
| $T_{CAC}^{(1)}$ | CLK to Data Delay | | 75 | | 80 | | 55 | | 60 | ns |
| T_{OH} | Data Hold from \overline{CE} , OE, or CLK | 0 | | 0 | | 0 | | 0 | | ns |
| $T_{DF}^{(2)}$ | \overline{CE} or OE to Data Float Delay | | 55 | | 55 | | 50 | | 50 | ns |
| T_{LC} | CLK Low Time | 25 | | 25 | | 25 | | 25 | | ns |
| T_{HC} | CLK High Time | 25 | | 25 | | 25 | | 25 | | ns |
| T_{SCE} | \overline{CE} Setup Time to CLK (to guarantee proper counting) | 35 | | 60 | | 30 | | 35 | | ns |
| T_{HCE} | \overline{CE} Hold Time from CLK (to guarantee proper counting) | 0 | | 0 | | 0 | | 0 | | ns |
| T_{HOE} | OE High Time (guarantees counter is reset) | 25 | | 25 | | 25 | | 25 | | ns |
| F_{MAX} | Maximum Clock Frequency | | 10 | | 10 | | 15 | | 10 | MHz |

- Notes: 1. AC test lead = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

AC Characteristics

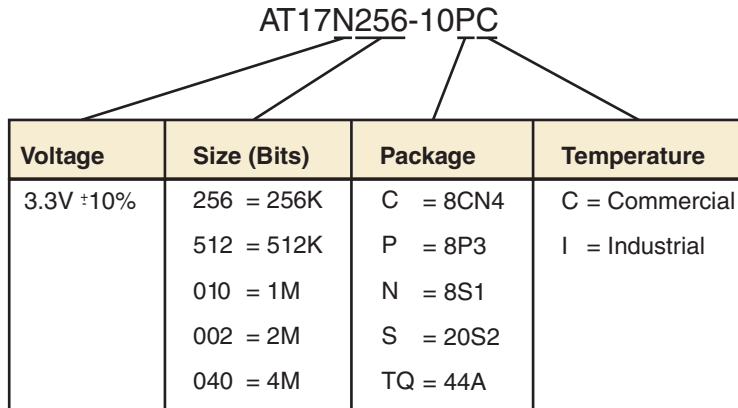


Thermal Resistance Coefficients⁽¹⁾

| Package Type | | | AT17N256 | AT17N512/ AT17N010 | AT17N002 | AT17N040 |
|--------------|--|--|----------|-----------------------|----------|----------|
| 8CN4 | Leadless Array Package (LAP) | θ_{JC} [$^{\circ}\text{C}/\text{W}$] | – | 45 | 45 | – |
| | | θ_{JA} [$^{\circ}\text{C}/\text{W}$] ⁽²⁾ | – | 135.71 | 159.60 | – |
| 8P3 | Plastic Dual Inline Package (PDIP) | θ_{JC} [$^{\circ}\text{C}/\text{W}$] | 37 | 37 | – | – |
| | | θ_{JA} [$^{\circ}\text{C}/\text{W}$] ⁽²⁾ | 107 | 107 | – | – |
| 8S1 | Plastic Gull Wing Small Outline (SOIC) | θ_{JC} [$^{\circ}\text{C}/\text{W}$] | 45 | – | – | – |
| | | θ_{JA} [$^{\circ}\text{C}/\text{W}$] ⁽²⁾ | 150 | – | – | – |
| 20S2 | Plastic Gull Wing Small Outline (SOIC) | θ_{JC} [$^{\circ}\text{C}/\text{W}$] | | | | – |
| | | θ_{JA} [$^{\circ}\text{C}/\text{W}$] ⁽²⁾ | | | | – |
| 44A | Thin Plastic Quad Flat Package (TQFP) | θ_{JC} [$^{\circ}\text{C}/\text{W}$] | – | – | 17 | 17 |
| | | θ_{JA} [$^{\circ}\text{C}/\text{W}$] ⁽²⁾ | – | – | 62 | 62 |

- Notes: 1. For more information refer to the “Thermal Characteristics of Atmel’s Packages”, available on the Atmel web site.
 2. Airflow = 0 ft/min.

Figure 1. Ordering Code



| Package Type | |
|--------------|--|
| 8CN4 | 8-lead, 6 mm x 6 mm x 1 mm, Leadless Array Package (LAP) – Pin-compatible with 8-lead SOIC/VOID Packages |
| 8P3 | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 8S1 | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| 20S2 | 20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| 44A | 44-lead, Thin (1.0 mm) Plastic Quad Flat Package Carrier (TQFP) |

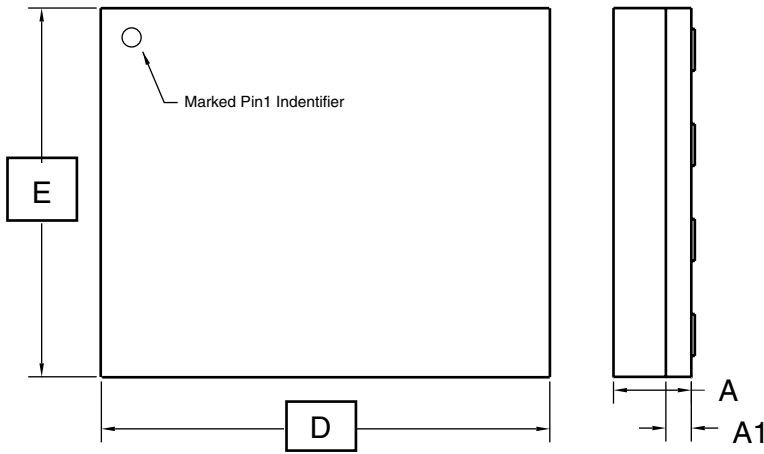


Ordering Information

| Memory Size | Ordering Code | Package | Operation Range |
|-------------|--|---------------------|-------------------------------|
| 256-Kbit | AT17N256-10PC AT17N256-10NC AT17N256-10SC | 8P3 8S1 20S2 | Commercial (0°C to 70°C) |
| | AT17N256-10PI AT17N256-10NI AT17N256-10SI | 8P3 8S1 20S2 | Industrial (-40°C to 85°C) |
| 512-Kbit | AT17N512-10CC AT17N512-10PC AT17N512-10SC | 8CN4 8P3 20S2 | Commercial (0°C to 70°C) |
| | AT17N512-10CI AT17N512-10PI AT17N512-10SI | 8CN4 8P3 20S2 | Industrial (-40°C to 85°C) |
| 1-Mbit | AT17N010-10CC AT17N010-10PC AT17N010-10SC | 8CN4 8P3 20S2 | Commercial (0°C to 70°C) |
| | AT17N010-10CI AT17N010-10PI AT17N010-10SI | 8CN4 8P3 20S2 | Industrial (-40°C to 85°C) |
| 2-Mbit | AT17N002-10CC AT17N002-10SC AT17N002-10TQC | 8CN4 20S2 44A | Commercial (0°C to 70°C) |
| | AT17N002-10CI AT17N002-10SI AT17N002-10TQI | 8CN4 20S2 44A | Industrial (-40°C to 85°C) |
| 4-Mbit | AT17N040-10TQC | 44A | Commercial (0°C to 70°C) |
| | AT17N040-10TQI | 44A | Industrial (-40°C to 85°C) |

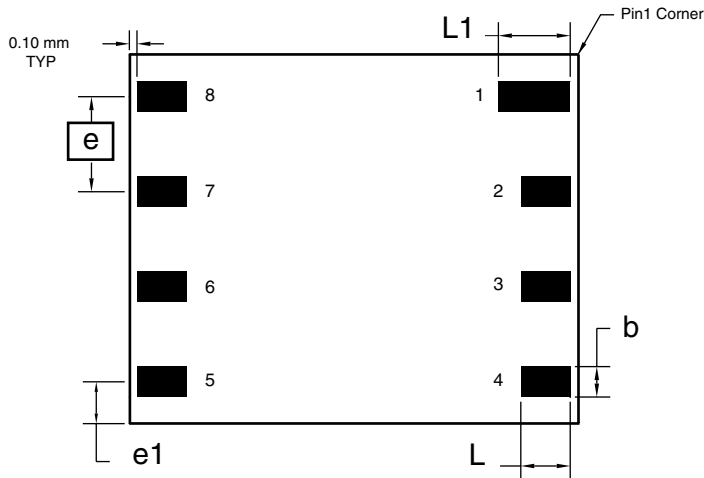
Packaging Information

8CN4 – LAP



Top View

Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|------|------|------|
| A | 0.94 | 1.04 | 1.14 | |
| A1 | 0.30 | 0.34 | 0.38 | |
| b | 0.45 | 0.50 | 0.55 | 1 |
| D | 5.89 | 5.99 | 6.09 | |
| E | 4.89 | 5.99 | 6.09 | |
| e | 1.27 BSC | | | |
| e1 | 1.10 REF | | | |
| L | 0.95 | 1.00 | 1.05 | 1 |
| L1 | 1.25 | 1.30 | 1.35 | 1 |

Note: 1. Metal Pad Dimensions.

11/14/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

8CN4, 8-lead (6 x 6 x 1.04 mm Body), Lead Pitch 1.27 mm,
Leadless Array Package (LAP)

DRAWING NO.

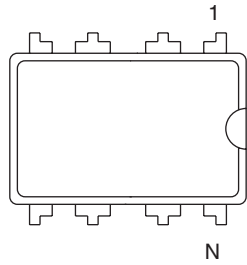
8CN4

REV.

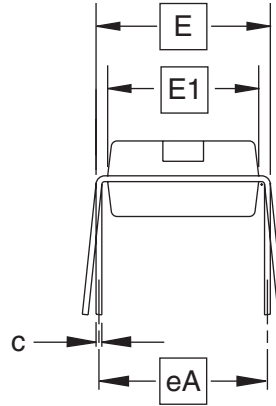
A



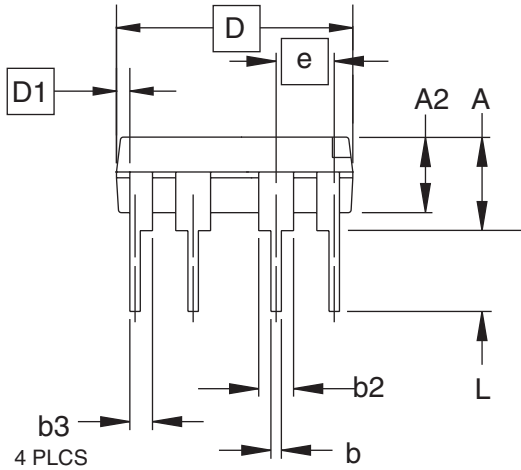
8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-------|-------|------|
| A | | | 0.210 | 2 |
| A2 | 0.115 | 0.130 | 0.195 | |
| b | 0.014 | 0.018 | 0.022 | 5 |
| b2 | 0.045 | 0.060 | 0.070 | 6 |
| b3 | 0.030 | 0.039 | 0.045 | 6 |
| c | 0.008 | 0.010 | 0.014 | |
| D | 0.355 | 0.365 | 0.400 | 3 |
| D1 | 0.005 | | | 3 |
| E | 0.300 | 0.310 | 0.325 | 4 |
| E1 | 0.240 | 0.250 | 0.280 | 3 |
| e | 0.100 BSC | | | |
| eA | 0.300 BSC | | | 4 |
| L | 0.115 | 0.130 | 0.150 | 2 |

- Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
 2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
 3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
 4. E and eA measured with the leads constrained to be perpendicular to datum.
 5. Pointed or rounded lead tips are preferred to ease insertion.
 6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

01/09/02



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San Jose, CA 95131

TITLE

8P3, 8-lead, 0.300" Wide Body, Plastic Dual
In-line Package (PDIP)

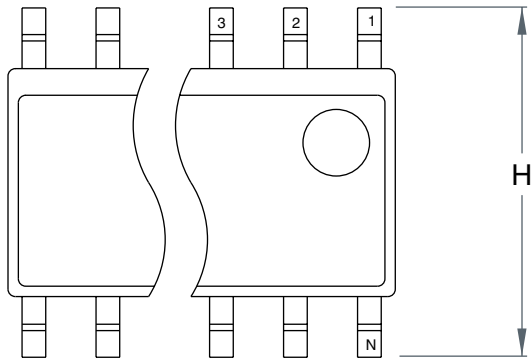
DRAWING NO.

8P3

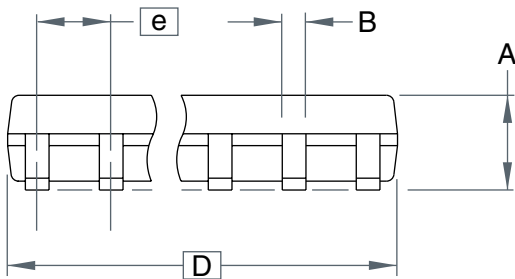
REV.

B

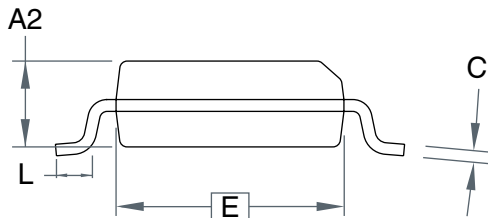
8S1 – SOIC



Top View



Side View



End View

COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|-----|------|------|
| A | – | – | 1.75 | |
| B | – | – | 0.51 | |
| C | – | – | 0.25 | |
| D | – | – | 5.00 | |
| E | – | – | 4.00 | |
| e | 1.27 BSC | | | |
| H | – | – | 6.20 | |
| L | – | – | 1.27 | |

Note: This drawing is for general information only. Refer to JEDEC Drawing MS-012 for proper dimensions, tolerances, datums, etc.

10/10/01



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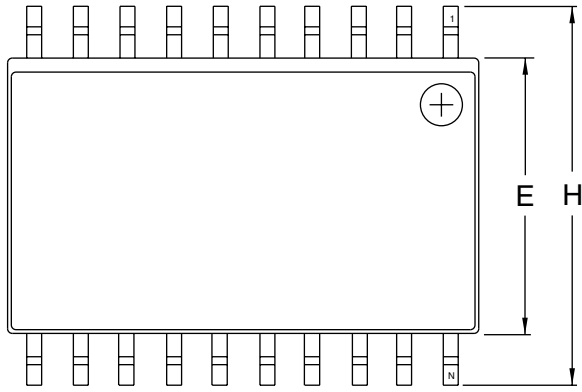
TITLE
8S1, 8-lead (0.150" Wide Body), Plastic Gull Wing
Small Outline (JEDEC SOIC)

DRAWING NO.
8S1

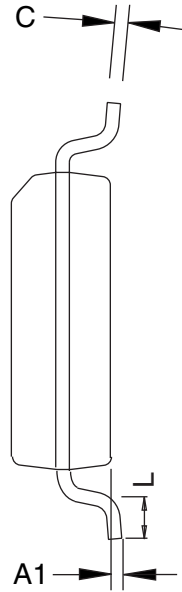
REV.
A



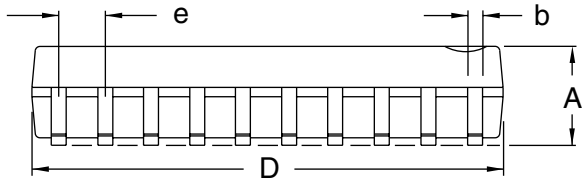
20S2 – SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|------|
| A | 0.0926 | | 0.1043 | |
| A1 | 0.0040 | | 0.0118 | |
| b | 0.0130 | | 0.0200 | 4 |
| C | 0.0091 | | 0.0125 | |
| D | 0.4961 | | 0.5118 | 1 |
| E | 0.2914 | | 0.2992 | 2 |
| H | 0.3940 | | 0.4190 | |
| L | 0.0160 | | 0.050 | 3 |
| e | 0.050 BSC | | | |

- Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
 2. Dimension "D" does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006") per side.
 3. Dimension "E" does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010") per side.
 4. "L" is the length of the terminal for soldering to a substrate.
 5. The lead width "b", as measured 0.36 mm (0.014") or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024") per side. 1/9/02



2325 Orchard Parkway
San Jose, CA 95131

TITLE

20S2, 20-lead, 0.300" Wide Body, Plastic Gull
Wing Small Outline Package (SOIC)

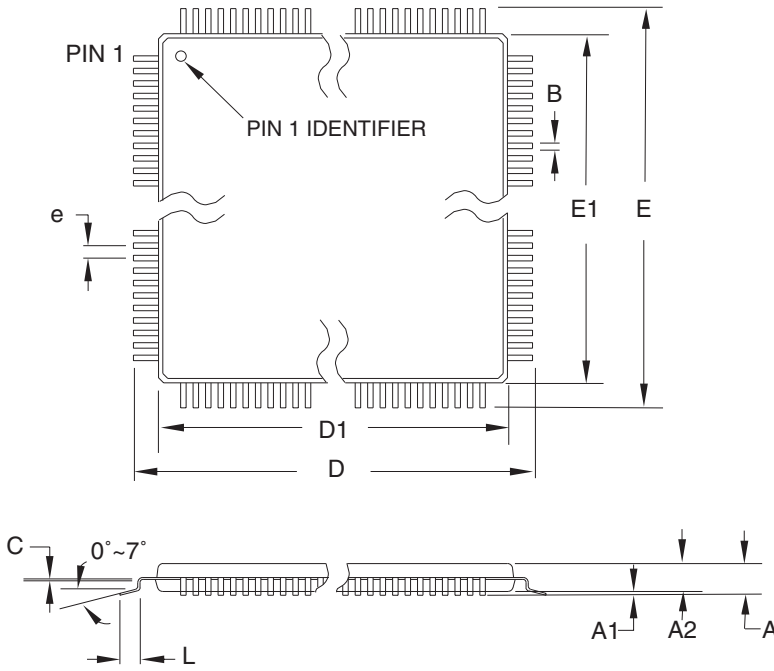
DRAWING NO.

20S2

REV.

A

44A – TQFP




COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|-------|-------|--------|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 11.75 | 12.00 | 12.25 | |
| D1 | 9.90 | 10.00 | 10.10 | Note 2 |
| E | 11.75 | 12.00 | 12.25 | |
| E1 | 9.90 | 10.00 | 10.10 | Note 2 |
| B | 0.30 | – | 0.45 | |
| C | 0.09 | – | 0.20 | |
| L | 0.45 | – | 0.75 | |
| e | 0.80 TYP | | | |

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

| | | | |
|--|--|---------------------------|------------------|
|  2325 Orchard Parkway San Jose, CA 95131 | TITLE 44A, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) | DRAWING NO. 44A | REV. B |
| | | | |



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenalux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Atmel Programmable SLI Hotline
(408) 436-4119

Atmel Programmable SLI e-mail
configurator@atmel.com

FAQ
Available on web site

e-mail
literature@atmel.com

Web Site
<http://www.atmel.com>

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