3.3 V 'SpreadTrak' Zero Delay Buffer

Features

- Zero input - output propagation delay, adjustable by capacitive load on FBK input.
- Multiple configurations - Refer "ASM5P23S04A Configurations Table".
- Input frequency range: 10MHz to 133MHz
- Multiple low-skew outputs.
- Output-output skew less than 200 ps.
- Device-device skew less than 500 ps.
- Two banks of four outputs.
- Less than 200 ps cycle-to-cycle jitter
- Available in space saving, 8-pin 150-mil SOIC packages.
- 3.3V operation.
- Advanced 0.35µ CMOS technology.
- Industrial temperature available.
- 'SpreadTrak'

Functional Description

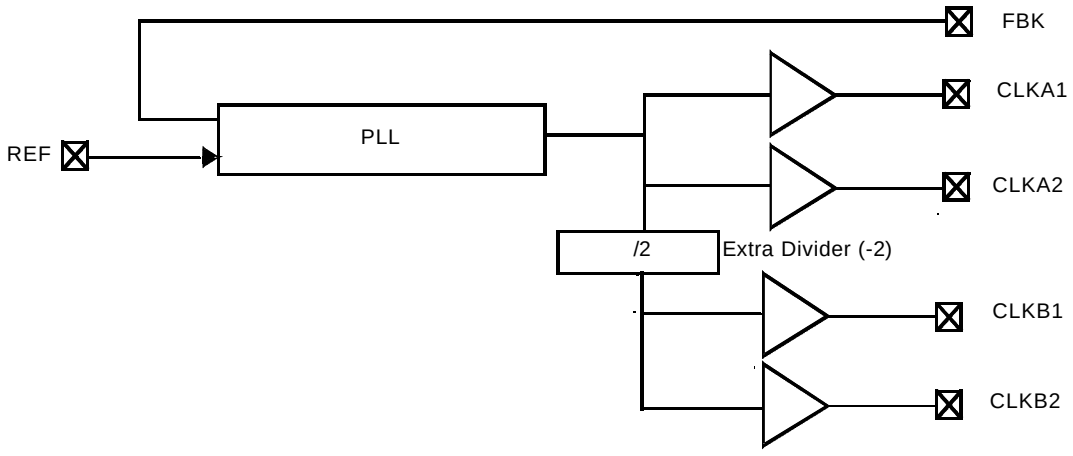
ASM5P23S04A is a versatile, 3.3V zero-delay buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom and other high-performance applications. It is available in a 8-pin package. The part has an on-chip PLL which locks to an input clock presented on the REF pin. The PLL feedback is required to be driven to FBK pin, and can be obtained from one of the outputs. The input-to-output propagation delay is guaranteed to be less than 250ps, and the output-to-output skew is guaranteed to be less than 200ps.

The ASM5P23S04A has two banks of two outputs each. Multiple ASM5P23S04A devices can accept the same input clock and distribute it. In this case the skew between the outputs of the two devices is guaranteed to be less than 500ps.

The ASM5P23S04A is available in two different configurations (Refer "ASM5P23S04A Configurations Table). The ASM5P23S04A-1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path. The ASM5P23S04A-1H is the high-drive version of the -1 and the rise and fall times on this device are much faster.

The ASM5P23S04A-2 allows the user to obtain Ref, 1/2 X and 2X frequencies on each output bank. The exact configuration and output frequencies depend on which output drives the feedback pin. The ASM5P23S04A-5H is a high-drive version with REF/2 on both banks

Block Diagram



ASM5P23S04A Configurations

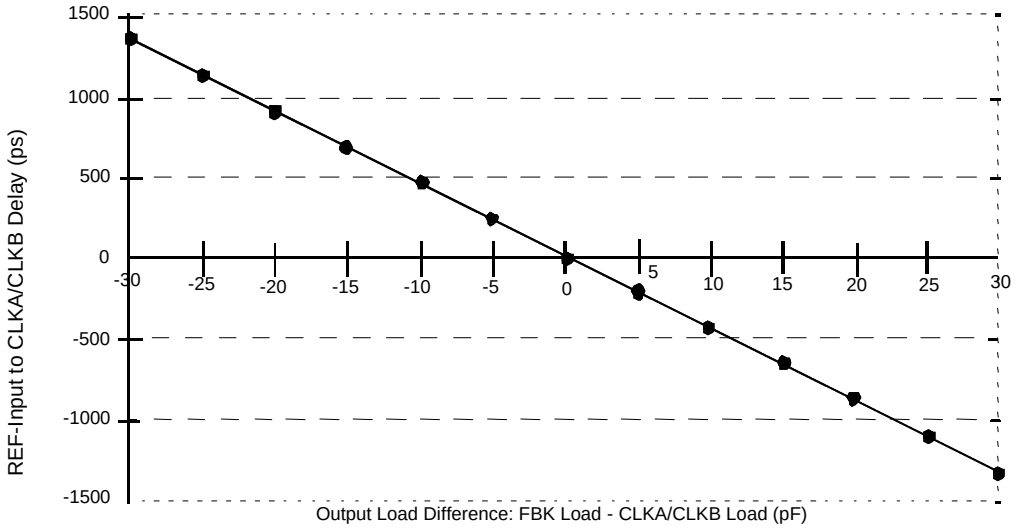
Device	Feedback From	Bank A Frequency	Bank B Frequency
ASM5P23S04A-1	Bank A or Bank B	Reference	Reference
ASM5P23S04A-1H	Bank A or Bank B	Reference	Reference
ASM5P23S04A-2	Bank A	Reference	Reference /2
ASM5P23S04A-2	Bank B	2 X Reference	Reference
ASM5P23S04A-5H	Bank A or Bank B	Reference /2	Reference /2

'SpreadTrak'

Many systems being designed now utilize a technology called Spread Frequency Timing Generation. ASM3P23S04A is designed so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the Spread Spectrum feature through, the result is a significant amount of tracking skew which may cause problems in the systems requiring synchronization.

Zero Delay and Skew Control

For applications requiring zero input-output delay, all outputs must be equally loaded.

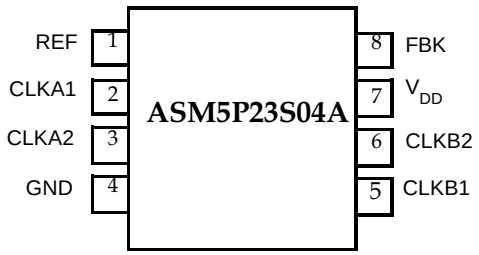


REF Input to CLKA/CLKB Delay Vs Difference in Loading between FBK pin and CLKA/CLKB pins

To close the feedback loop of the ASM5P23S04A, the FBK pin can be driven from any of the four available output pins. The output driving the FBK pin will be driving a total load of 7 pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input output delay. This is shown in the above graph.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. If input-output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs. For zero output-output skew, be sure to load outputs equally.

Pin Configuration



Pin Description for ASM5P23S04A

Pin #	Pin Name	Description
1	REF[1]	Input reference frequency, 5V tolerant input
2	CLKA1[2]	Buffered clock output, bank A
3	CLKA2[2]	Buffered clock output, bank A
4	GND	Ground
5	CLKB1[2]	Buffered clock output, bank B
6	CLKB2 [2]	Buffered clock output, bank B
7	V_{DD}	3.3V supply
8	FBK	PLL feedback input

Notes:
1. Weak pull-down.
2. Weak pull-down on all outputs.

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	-0.5	+7.0	V
DC Input Voltage (Except REF)	-0.5	V_{DD} + 0.5	V
DC Input Voltage (REF)	-0.5	7	V
Storage Temperature	-65	+150	°C
Max. Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)		>2000	V

Note: These are stress ratings only and functional usage is not implied. Exposure to absolute maximum ratings for prolonged periods can affect device reliability.

Operating Conditions for ASM5P23S04A Commercial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, below 100 MHz		30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz		15	pF
C_{IN}	Input Capacitance[3]		7	pF

Note: 3. Applies to both Ref Clock and FBK.

Electrical Characteristics for ASM5P23S04A Commercial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	µA
V_{OL}	Output LOW Voltage [4]	I_{OL} = 8mA (-1, -2) I_{OH} = 12mA (-1H, -5H)		0.4	V
V_{OH}	Output HIGH Voltage [4]	I_{OL} = -8mA (-1, -2) I_{OH} = -12mA (-1H, -5H)	2.4		V
I_{DD}	Supply Current	Unloaded outputs 100MHz REF, Select inputs at V_{DD} or GND		TBD	mA
				TBD	
		Unloaded outputs, 66MHz REF (-1, -2)		TBD	
		Unloaded outputs, 33MHz REF (-1, -2)		TBD	

Note: 4. Parameter is guaranteed by design and characterization. Not 100% tested in production.
5. REF Input Vth = ~ VDD/2

Switching Characteristics for ASM5P23S04A Commercial Temperature Devices

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30-pF load, All devices	10		100	MHz
t_1	Output Frequency	20-pF load, -1H, -5H devices	10		133.3	MHz
t_1	Output Frequency	15-pF load, -1, -2 devices	10		133.3	MHz
	Duty Cycle [4]= (t_2 / t_1) * 100 (-1, -2, -1H, -5H)	Measured at 1.4V, F_{OUT} = 66.66 MHz 30-pF load	40.0	50.0	60.0	%
	Duty Cycle [4] = (t_2 / t_1) * 100 (-1, -2,-1H, -5H)	Measured at 1.4V, F_{OUT} = <50 MHz 15-pF load	45.0	50.0	55.0	%
t_3	Output Rise Time [4] (-1, -2)	Measured between 0.8V and 2.0V 30-pF load			2.20	ns
t_3	Output Rise Time [4] (-1, -2)	Measured between 0.8V and 2.0V 15-pF load			1.50	ns
t_3	Output Rise Time [4] (-1H, -5H)	Measured between 0.8V and 2.0V 30-pF load			1.50	ns
t_4	Output Fall Time [4] (-1, -2)	Measured between 2.0V and 0.8V 30-pF load			2.20	ns
t_4	Output Fall Time [4] (-1, -2)	Measured between 2.0V and 0.8V 15-pF load			1.50	ns
t_4	Output Fall Time [4] (-1H, -5H)	Measured between 2.0V and 0.8V 30-pF load			1.25	ns
t_5	Output-to-output skew on same bank (-1, -2) [4]	All outputs equally loaded			200	ps
	Output-to-output skew (-1H, -5H)	All outputs equally loaded			200	
	Output bank A -to- output bank B skew (-1, -5H)	All outputs equally loaded			200	
	Output bank A to output bank b skew (-2)	All outputs equally loaded			400	
t_6	Delay, REF Rising Edge to FBK Rising Edge [3]	Measured at V_{DD} /2		0	±250	ps
t_7	Device-to-Device Skew [4]	Measured at V_{DD}/2 on the FBK pins of the device		0	500	ps
t_8	Output Slew Rate[4]	Measured between 0.8V and 2.0V using Test Circuit #2	1			V/ns
t_J	Cycle-to-cycle jitter [4] (-1, -1H, -5H)	Measured at 66.67 MHz, loaded outputs, 15 pF load			175	ps
		Measured at 66.67 MHz, loaded outputs, 30 pF load			200	
		Measured at 133.3 MHz, loaded outputs, 15 pF load			100	
t_J	Cycle-to-cycle jitter [4] (-2,)	Measured at 66.67 MHz, loaded outputs, 30pF load			400	ps
		Measured at 66.67 MHz, loaded outputs, 15 pF load			375	
t_{LOCK}	PLL Lock Time [4]	Stable power supply, valid clock presented on REF and FBK pins			1.0	ms

Operating Conditions for ASM5I23S04A Industrial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	-40	85	°C
C_L	Load Capacitance, below 100 MHz		30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz		15	pF
C_{IN}	Input Capacitance[3]		7	pF

Electrical Characteristics for ASM5I23S04A Industrial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	µA
V_{OL}	Output LOW Voltage [4]	I_{OL} = 8mA (-1, -2) I_{OH} = 12mA (-1H, -5H)		0.4	V
V_{OH}	Output HIGH Voltage [4]	I_{OL} = -8mA (-1, -2) I_{OH} = -12mA (-1H, -5H)	2.4		V
I_{DD}	Supply Current	Unloaded outputs 100MHz REF, Select inputs at V_{DD} or GND		TBD	mA
				TBD	
		Unloaded outputs, 66MHz REF (-1, -2)		TBD	
		Unloaded outputs, 33MHz REF (-1, -2)		TBD	

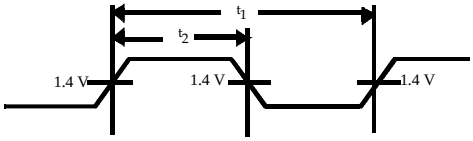
Switching Characteristics for ASM5I23S04A Industrial Temperature Devices

All parameters are specified with loaded outputs

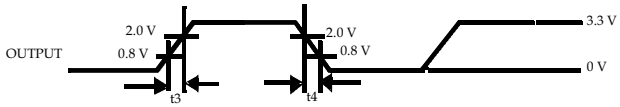
Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30-pF load, All devices	10		100	MHz
t_1	Output Frequency	20-pF load, -1H, -5H devices	10		133.3	MHz
t_1	Output Frequency	15-pF load, -1 and -2 devices	10		133.3	MHz
	Duty Cycle [4] = (t_2 / t_1) * 100 (-1, -2, -1H, -5H)	Measured at 1.4V, F_{OUT} = <66.66 MHz 30-pF load	40.0	50.0	60.0	%
	Duty Cycle [4]= (t_2 / t_1) * 100 (-1, -2, -1H, -5H)	Measured at 1.4V, F_{OUT} = <50 MHz 15-pF load	45.0	50.0	55.0	%
t_3	Output Rise Time [4] (-1, -2)	Measured between 0.8V and 2.0V 30-pF load			2.50	ns
t_3	Output Rise Time [4] (-1, -2)	Measured between 0.8V and 2.0V 15-pF load			1.50	ns
t_3	Output Rise Time [4] (-1H, -5H)	Measured between 0.8V and 2.0V 30-pF load			1.50	ns
t_4	Output Fall Time [4] (-1, -2)	Measured between 2.0V and 0.8V 30-pF load			2.50	ns
t_4	Output Fall Time [4] (-1, -2)	Measured between 2.0V and 0.8V 15-pF load			1.50	ns
t_4	Output Fall Time [4] (-1H, -5H)	Measured between 2.0V and 0.8V 30-pF load			1.25	ns
t_5	Output-to-output skew on same bank (-1, -2) [4]	All outputs equally loaded			200	ps
	Output-to-output skew (-1H, -5H)	All outputs equally loaded			200	
	Output bank A -to- output bank B skew (-1, -5H)	All outputs equally loaded			200	
	Output bank A -to- output bank B skew (-2)	All outputs equally loaded			400	
t_6	Delay, REF Rising Edge to FBK Rising Edge [4]	Measured at V_{DD} /2		0	±250	ps
t_7	Device-to-Device Skew [4]	Measured at V_{DD}/2 on the FBK pins of the device		0	500	ps
t_8	Output Slew Rate[4]	Measured between 0.8V and 2.0V using Test Circuit #2	1			V/ns
t_J	Cycle-to-cycle jitter [4] (-1, -1H, -5H)	Measured at 66.67 MHz, loaded outputs, 15 pF load			180	ps
		Measured at 66.67 MHz, loaded outputs, 30 pF load			200	
		Measured at 133.3 MHz, loaded outputs, 15 pF load			100	
t_J	Cycle-to-cycle jitter [4] (-2)	Measured at 66.67 MHz, loaded outputs, 30pF load			400	ps
		Measured at 66.67 MHz, loaded outputs, 15 pF load			380	
t_{LOCK}	PLL Lock Time [4]	Stable power supply, valid clock presented on REF and FBK pins			1.0	ms

Switching Waveforms

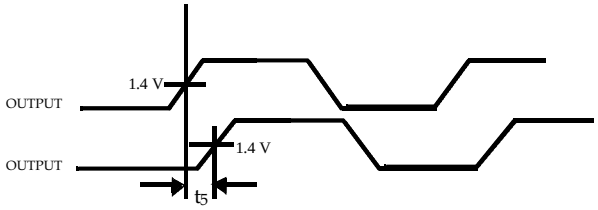
Duty Cycle Timing



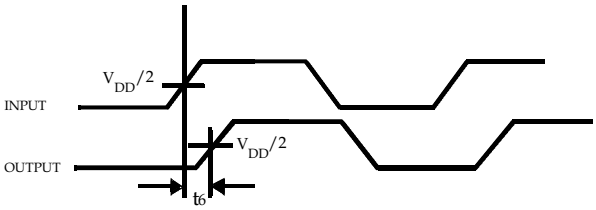
All Outputs Rise/Fall Time



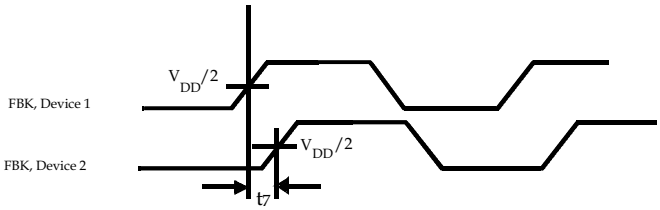
Output - Output Skew



Input - Output Propagation Delay

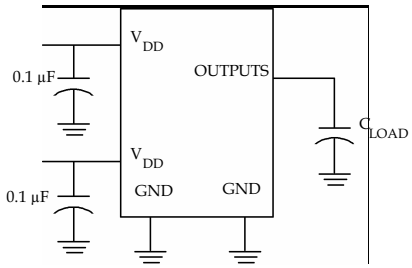


Device - Device Skew

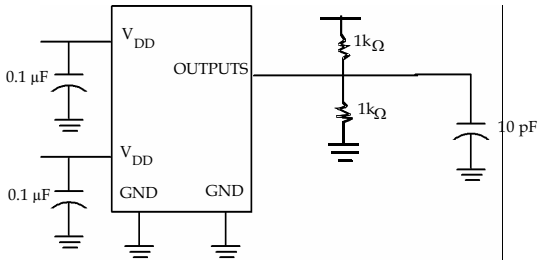


Test Circuits

Test Circuit #1

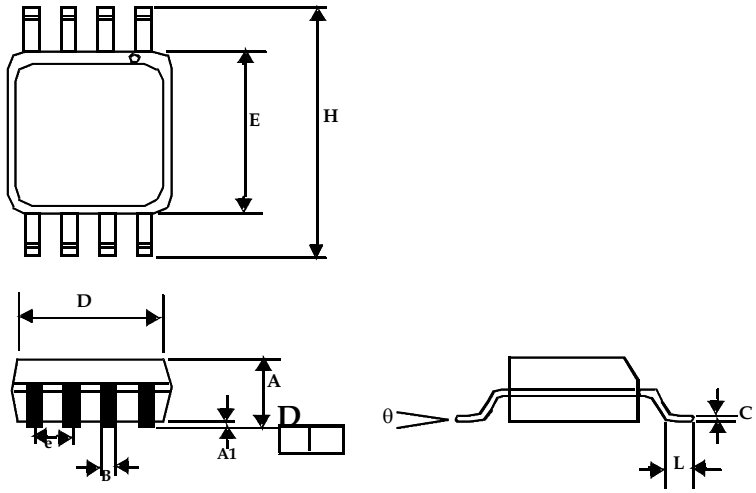


Test Circuit #2



For parameter t_8 (output slew rate) on -1H devices

Package Information: 8-lead (150 Mil) Molded SOIC



Symbol	Dimensions in inches		Dimensions in millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.022	0.33	0.53
C	0.007	0.012	0.18	0.27
D	0.188	0.197	4.78	5.00
E	0.150	0.158	3.80	4.01
H	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.035	0.40	0.89
θ	0°	8°	0°	8°

Ordering Information

Ordering Code	Package Type	Operating Range
ASM5P23S04A-1-08-SR	8-pin 150-mil SOIC-TAPE & REEL	Commercial
ASM5P23S04A-1-08-ST	8-pin 150-mil SOIC-TUBE	Commercial
ASM5I23S04A-1-08-SR	8-pin 150-mil SOIC-TAPE & REEL	Industrial
ASM5I23S04A-1-08-ST	8-pin 150-mil SOIC-TUBE	Industrial
ASM5P23S04A-1H-08-SR	8-pin 150-mil SOIC-TAPE & REEL	Commercial
ASM5P23S04A-1H-08-ST	8-pin 150-mil SOIC-TUBE	Commercial
ASM5I23S04A-1H-08-SR	8-pin 150-mil SOIC-TAPE & REEL	Industrial
ASM5I23S04A-1H-08-ST	8-pin 150-mil SOIC-TUBE	Industrial
ASM5P23S04A-2-08-SR	8-pin 150-mil SOIC-TAPE & REEL	Commercial
ASM5P23S04A-2-08-ST	8-pin 150-mil SOIC-TUBE	Commercial
ASM5I23S04A-2-08-SR	8-pin 150-mil SOIC-TAPE & REEL	Industrial
ASM5I23S04A-2-08-ST	8-pin 150-mil SOIC-TUBE	Industrial
ASM5P23S04A-5H-08-SR	8-pin 150-mil SOIC-TAPE & REEL	Commercial
ASM5P23S04A-5H-08-ST	8-pin 150-mil SOIC-TUBE	Commercial
ASM5I23S04A-5H-08-SR	8-pin 150-mil SOIC-TAPE & REEL	Industrial
ASM5I23S04A-5H-08-ST	8-pin 150-mil SOIC-TUBE	Industrial

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Document Version: 2.0 8_30_2004

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003