

74FR900 9-Bit, 3-Port Latchable Datapath Multiplexer

General Description

The 74FR900 is a data bus multiplexer routing any of three 9-bit ports to any other one of the three ports. Readback of data latched from any port onto itself is also possible. The 74FR900 maintains separate control of all latch-enable, output enable and select inputs for maximum flexibility. PINV allows inversion of the data from the C₈ to A₈ or B₈ path. This is useful for control of the parity bit in systems diagnostics.

Fairchild's 74FR25900 includes 25Ω resistors in series with port A and B outputs. Resistors minimize undershoot and ringing which may damage or corrupt sensitive device inputs driven by these ports.

Features

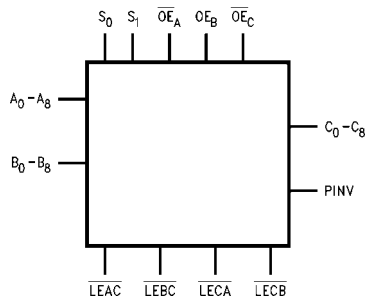
- 9-bit data ports for systems carrying parity bits
- Readback capability for system self checks.
- Independent control lines for maximum flexibility
- Guaranteed multiple output switching and 250 pF load delays
- Outputs optimized for dynamic bus drive capability
- PINV parity control facilitates system diagnostics
- FR25900 resistor option for driving MOS inputs such as DRAM arrays

Ordering Code:

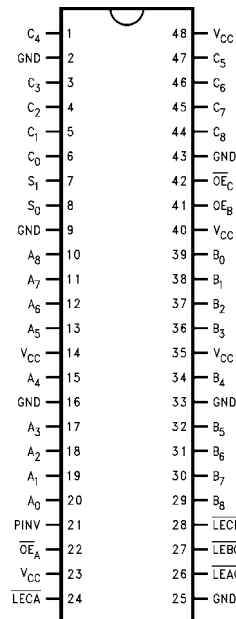
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74FR900SSC | MS48A | 48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Description

| Pin Names | Description |
|---------------------------------|----------------------------------|
| \overline{LE}_{xx} | Latch Enable Inputs |
| OE_x | Output Enable Inputs |
| PINV | Parity Invert Input |
| S ₀ , S ₁ | Select Inputs |
| A ₀ -A ₈ | Port A Inputs or 3-STATE Outputs |
| B ₀ -B ₈ | Port B Inputs or 3-STATE Outputs |
| C ₀ -C ₈ | Port C Inputs or 3-STATE Outputs |

Functional Description

The 74FR900 allows 9-bit data to be transferred from any of three 9-bit I/O ports to either of the two remaining I/O ports. The device employs latches in all paths for either transparent or synchronous operation. Readback capability from any port to itself is also possible.

Data transfer within the 74FR900 is controlled through use of the select (S_0 and S_1) and output-enable (\overline{OE}_A , \overline{OE}_B and \overline{OE}_C) inputs as described in Table 1. Additional control is available by use of the latch-enable inputs (\overline{LEAC} , \overline{LECA} , \overline{LEBC} , \overline{LECB}) allowing either synchronous or transparent transfers (see Table 2). Table 1 indicates several readback conditions. By latching data on a given port and initiating the readback control configuration, previous data may be read for system verification or diagnostics. This mode may be useful in implementing system diagnostics.

Data at the port to be readback must be latched prior to enabling the outputs on that port. If this is not done, a closed data loop will result causing possible data integrity problems. Note that the A and B ports allow readback without affecting any other port. Port C, however, requires interruption of either port A or B to complete its readback path.

PINV controls inversion of the C_8 bit. A low on PINV allows C_8 data to pass unaltered. A high causes inversion of the data. See Table 3. This feature allows forcing of parity errors for use in system diagnostics. This is particularly helpful in 486 processor designs as the 486 does not provide odd/even parity selection internally.

TABLE 1. Datapath Control

| Inputs | | | | | Function |
|--------|-------|-------------------|-------------------|-------------------|----------------------------------|
| S_0 | S_1 | \overline{OE}_A | \overline{OE}_B | \overline{OE}_C | |
| L | X | H | L | L | Port A to Port C |
| L | L | H | H | H | Port A to Port B |
| L | O | H | H | L | Port A to B+C |
| H | L | L | L | H | Port B to Port A |
| H | X | H | L | L | Port B to Port C |
| H | O | L | L | L | Port B to A+C |
| X | H | L | L | H | Port C to Port A |
| X | H | H | H | H | Port C to Port B |
| X | H | L | H | H | Port C to A+B |
| X | X | H | L | H | Outputs Disabled |
| L | L | L | X | X | (Readback to A) (Note 1) |
| L | H | L | X | L | (Readback to A or C) (Note 1) |
| H | L | X | H | X | (Readback to B) (Note 1) |
| H | H | X | H | L | (Readback to B or C) (Note 1) |

Note 1: Readback operation in latched mode only. Transparent operation could result in unpredictable results.

TABLE 2. Latch-Enable Control

| \overline{LE}_{xx} | Input | Output |
|----------------------|-------|--------|
| L | L | L |
| L | H | H |
| H | X | Q_0 |

L = LOW Voltage

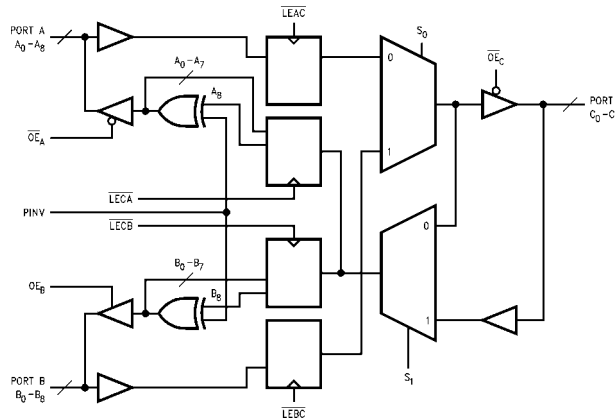
H = HIGH Voltage Level

TABLE 3. PINV Control

| PINV | C_8 | A_8 or B_8 |
|------|-------|----------------|
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

Q_0 = Output state prior to \overline{LE}_{xx} LOW-to-HIGH transition

Logic Diagram



Absolute Maximum Ratings (Note 2)

| | |
|--|--------------------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 3) | -0.5V to +7.0V |
| Input Current (Note 3) | -30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | -0.5V to V _{CC} |
| 3-STATE Output | -0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated I _{OL} (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

Recommended Operating Conditions

| | |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | V _{CC} | Conditions |
|------------------------------------|--|------|-----|------|-------|-----------------|--|
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 2.4 | | | V | Min | I _{OH} = -3 mA (A _n , B _n , C _n) |
| | | 2.0 | | | V | Min | I _{OH} = -15 mA (A _n , B _n , C _n) |
| V _{OL} | Output LOW Voltage | | | 0.50 | V | Min | I _{OL} = 24 mA (A _n , B _n , C _n) |
| I _{IH} | Input HIGH Current | | | 5 | μA | Max | V _{IN} = 2.7V (Control Inputs) |
| I _{BVI} | Input HIGH Current Breakdown Test | | | 7 | μA | Max | V _{IN} = 7.0V (Control Inputs) |
| I _{BVIT} | Input HIGH Current Breakdown Test (I/O) | | | 100 | μA | Max | V _{IN} = 5.5V (A _n , B _n , C _n) |
| I _{IL} | Input LOW Current | | | -150 | μA | Max | V _{IN} = 0.5V (Control Inputs) |
| V _{ID} | Input Leakage Test | 4.75 | | | V | 0.0 | I _{ID} = 1.9 μA, All Other Pins Grounded |
| I _{OD} | Output Circuit Leakage Test | | | 3.75 | V | 0.0 | V _{IOD} = 150 mV, All Other Pins Grounded |
| I _{IH} + I _{OZH} | Output Leakage Current | | | 25 | μA | Max | V _{OUT} = 2.7V (A _n , B _n , C _n) |
| I _{IL} + I _{OZL} | Output Leakage Current | | | -150 | μA | Max | V _{OUT} = 0.5V (A _n , B _n , C _n) |
| I _{OS} | Output Short Circuit Current | -100 | | -225 | mA | Max | V _{OUT} = 0.0V (A _n , B _n , C _n) |
| I _{CEx} | Output HIGH Leakage Current | | | 50 | μA | Max | V _{OUT} = V _{CC} (A _n , B _n , C _n) |
| I _{ZZ} | Bus Drainage Test | | | 100 | μA | 0.0 | V _{OUT} = 5.25V (A _n , B _n , C _n) |
| I _{CCH} | Power Supply Current | | 115 | 150 | mA | Max | All Outputs HIGH (Note 4) |
| I _{CCL} | Power Supply Current | | 170 | 200 | mA | Max | All Outputs LOW (Note 4) |
| I _{CCZ} | Power Supply Current | | 147 | 175 | mA | Max | Outputs in 3-STATE |

Note 4: 2 ports active only

| AC Electrical Characteristics | | | | | | | |
|--|---|--|------|---|--|-------|-------|
| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF | | Units |
| | | Min | Typ | Max | Min | Max | |
| t _{PLH} t _{PHL} | Propagation Delay A _n or B _n to C _n C _n to A _n or B _n | 2.0 | 4.2 | 7.0 | 2.0 | 7.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay C ₈ to A ₈ or B ₈ (PINV HIGH) | 2.5 | 4.8 | 7.5 | 2.5 | 7.5 | ns |
| t _{PLH} t _{PHL} | Propagation Delay A _n to B _n , B _n to A _n | 4.5 | 6.4 | 10.0 | 4.5 | 10.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay LEAC to C _n , LEBC to C _n | 4.5 | 6.8 | 10.0 | 4.5 | 10.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay LECA to A _n , LECB to B _n | 3.0 | 6.0 | 9.5 | 3.0 | 9.5 | ns |
| t _{PLH} t _{PHL} | Propagation Delay S ₀ to C _n | 3.0 | 6.0 | 10.0 | 3.0 | 10.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay S ₁ to A _n or B _n | 3.5 | 6.5 | 11.0 | 3.5 | 11.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay PINV to A ₈ or B ₈ | 2.0 | 5.0 | 9.0 | 2.0 | 9.0 | ns |
| t _{PZH} t _{PZL} | Output Enable Time A _n , C _n | 2.0 | 4.0 | 6.5 | 2.0 | 6.5 | ns |
| t _{PHZ} t _{PLZ} | Output Disable Time A _n , C _n | 1.5 | 4.0 | 6.0 | 1.5 | 6.0 | ns |
| t _{PZH} t _{PZL} | Output Enable Time B _n | 2.0 | 5.0 | 7.0 | 2.0 | 7.0 | ns |
| t _{PHZ} t _{PLZ} | Output Disable Time B _n | 2.0 | 5.0 | 7.0 | 2.0 | 7.0 | ns |
| AC Operating Requirements | | | | | | | |
| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF | | Units |
| | | Min | Typ | Max | Min | Max | |
| t _S (H) t _S (L) | Setup Time, HIGH or LOW A _n to LEAC, B _n to LEBC | 4.0 | 2.0 | | 4.0 | | ns |
| t _H (H) t _H (L) | Hold Time, HIGH or LOW A _n to LEAC, B _n to LEBC | 1.0 | -2.0 | | 1.0 | | ns |
| t _S (H) t _S (L) | Setup Time, HIGH or LOW C _n to LECA or LECB | 3.0 | 1.0 | | 3.0 | | ns |
| t _H (H) t _H (L) | Hold Time, HIGH or LOW C _n to LECA or LECB | 1.0 | -1.0 | | 1.0 | | ns |
| t _W (H) | LE Pulse Width LOW | 8.0 | 4.0 | | 8.0 | | ns |
| Extended AC Electrical Characteristics | | | | | | | |
| Symbol | Parameter | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF Nine Outputs Switching (Note 5) | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 250 pF (Note 6) | | Units | |
| | | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay | | | | | | |

Extended AC Electrical Characteristics (Continued)

| Symbol | Parameter | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF Nine Outputs Switching (Note 5) | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 250 pF (Note 6) | | Units |
|------------------|--|--|------|---|------|-------|
| | | Min | Max | Min | Max | |
| t _{PHL} | A _n or B _n to C _n C _n to A _n or B _n | 2.0 | 9.0 | 2.5 | 10.5 | ns |
| t _{PLH} | Propagation Delay C ₈ to A ₈ or B ₈ (PINV HIGH) | | | 3.5 | 11.0 | ns |
| t _{PLH} | Propagation Delay A _n to B _n , B _n to A _n | 4.5 | 12.0 | 5.5 | 13.5 | ns |
| t _{PLH} | Propagation Delay LEAC to C _n , LEBC to C _n | 4.5 | 12.0 | 5.5 | 13.5 | ns |
| t _{PLH} | Propagation Delay LECA to A _n , LECB to B _n | 3.0 | 11.5 | 4.0 | 13.5 | ns |
| t _{PLH} | Propagation Delay S ₀ to C _n | 3.0 | 11.0 | 3.0 | 14.0 | ns |
| t _{PLH} | Propagation Delay S ₁ to A _n or B _n | 3.5 | 12.0 | 4.5 | 15.0 | ns |
| t _{PLH} | Propagation Delay PINV to A ₈ or B ₈ | | | 2.5 | 12.0 | ns |
| t _{PZH} | Output Enable Time A _n , C _n | 2.0 | 8.0 | | | ns |
| t _{PHZ} | Output Disable Time A _n , C _n | 1.5 | 6.0 | | | ns |
| t _{PZH} | Output Enable Time B _n | 2.0 | 8.0 | | | ns |
| t _{PHZ} | Output Disable Time B _n | 2.0 | 7.0 | | | ns |

Note 5: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all LOW-to-HIGH, HIGH-to-LOW, 3-STATE-to-HIGH, etc.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors standard AC load. This specification pertains to single output switching only.

