CEM2005

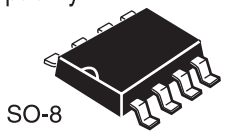
PRELIMINARY

Dual Enhancement Mode Field Effect Transistor(N and P Channel)

5

FEATURES

- 20V , 5A , $R_{DS(ON)}$=32m Ω @V_{GS}=4.5V.
  $R_{DS(ON)}$=43m Ω @V_{GS}=2.5V.
  -20V , -4A , $R_{DS(ON)}$=95m Ω @V_{GS}=-4.5V.
  $R_{DS(ON)}$=125m Ω @V_{GS}=-2.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Surface Mount Package.



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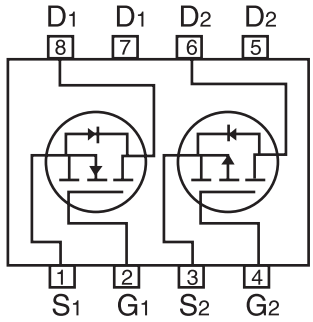

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	±8	±8	V
Drain Current-Continuous[a] @T_J=125°C	I_D	±5	±4	A
-Pulsed[b]	I_{DM}	±30	±16	A
Drain-Source Diode Forward Current[a]	I_S	1.7	-2.5	A
Maximum Power Dissipation[a]	P_D	2		W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient[a]	$R_{\theta JA}$	62.5	°C/W

N-Channel ELECTRICAL CHARACTERISTICS (TA 25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V, V_{GS}=0V			1	μA
Gate-Body Leakage	I_{GSS}	V_{GS}=±8V, V_{DS}=0V			±100	nA
ON CHARACTERISTICS[b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D = 250μA	0.5	0.68	1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D= 5.0A		26	32	mΩ
		V_{GS}=2.5V, I_D= 4.2A		30	43	mΩ
On-State Drain Current	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 4.5V	20			A
Forward Transconductance	g_{FS}	V_{DS} = 10V, I_D =5.0A	7	24		S
DYNAMIC CHARACTERISTICS[c]						
Input Capacitance	C_{ISS}	V_{DS} =8V, V_{GS} = 0V f =1.0MHz		1128	1500	pF
Output Capacitance	C_{OSS}			480	630	pF
Reverse Transfer Capacitance	C_{RSS}			119	160	pF
SWITCHING CHARACTERISTICS[c]						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 10V, I_D = 1A, V_{GEN} = 4.5V, R_L = 10Ω R_{GEN} = 6Ω		29	60	ns
Rise Time	t_r			65	140	ns
Turn-Off Delay Time	$t_{D(OFF)}$			60	140	ns
Fall Time	t_f			50	60	ns
Total Gate Charge	Q_g	V_{DS} =10V, I_D = 5A, V_{GS} =4.5V		47	60	nC
Gate-Source Charge	Q_{gs}			6		nC
Gate-Drain Charge	Q_{gd}			8		nC

CEM2005

P-Channel ELECTRICAL CHARACTERISTICS (TA 25°C unless otherwise **noted)**

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-20	-26		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-16V, V_{GS}=0V			-1	μA
Gate-Body Leakage	I_{GSS}	V_{GS}=±8V, V_{DS}=0V			±100	nA
ON CHARACTERISTICS[b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-0.6			V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-2.2A		55	95	mΩ
		V_{GS}=-2.5V, I_D=-1.8A		90	125	mΩ
On-State Drain Current	$I_{D(ON)}$	V_{DS}=-5V, V_{GS}=-4.5V	-20			A
Forward Transconductance	g_{FS}	V_{DS}=-16V, I_D=-2.2A	4			S
DYNAMIC CHARACTERISTICS[c]						
Input Capacitance	C_{ISS}	V_{DS}=-15V, V_{GS}=0V f=1.0MHz		1490	1950	pF
Output Capacitance	C_{OSS}			480	630	pF
Reverse Transfer Capacitance	C_{RSS}			135	180	pF
SWITCHING CHARACTERISTICS[c]						
Turn-On Delay Time	$t_{D(ON)}$	V_D=-10V, I_D=-2.2A, V_{GEN}=-4.5V, R_{GEN}=6Ω		8		ns
Rise Time	t_r			26		ns
Turn-Off Delay Time	$t_{D(OFF)}$			51		ns
Fall Time	t_f			33		ns
Total Gate Charge	Q_g	V_{DS}=-6V, I_D=-2.2A, V_{GS}=-4.5V		19	60	nC
Gate-Source Charge	Q_{gs}			2.5		nC
Gate-Drain Charge	Q_{gd}			6		nC

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition		Min	Typ[c]	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS [b]							
Diode Forward Voltage	V_{SD}	VGS = 0V, Is =1.7A	N-Ch		0.72	1.2	V
		VGS = 0V, Is =-1.8A	P-Ch		-0.9	-1.0	

Notes

a.Surface Mounted on FR4 Board, t ≤10sec.
b.Pulse Test:Pulse Width ≤300 μs, Duty Cycle ≤2%.
c.Guaranteed by design, not subject to production testing.

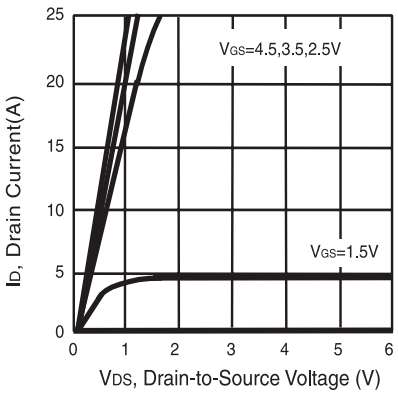

Figure 1. Output Characteristics

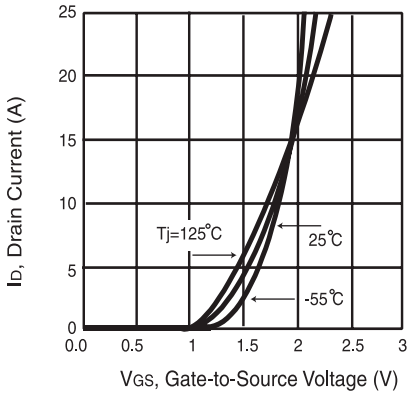

Figure 2. Transfer Characteristics

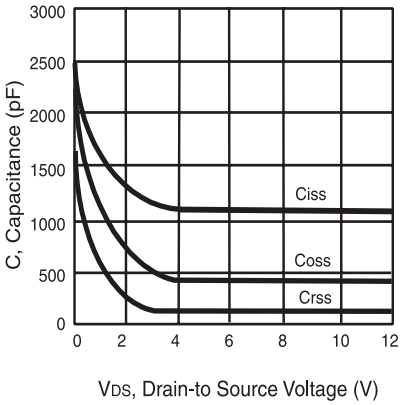

Figure 3. Capacitance

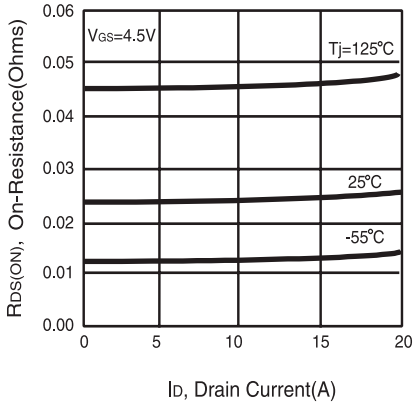

Figure 4. On-Resistance Variation with Drain Current and Temperature

N-Channel

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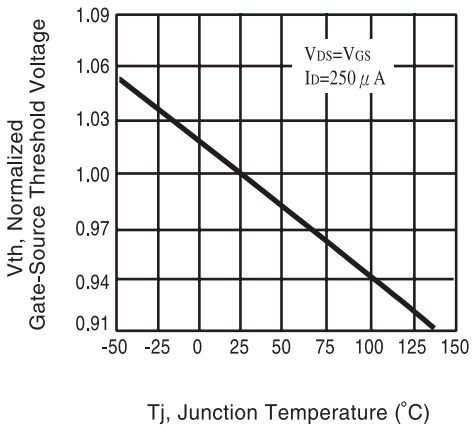


Figure 5. Gate Threshold Variation with Temperature

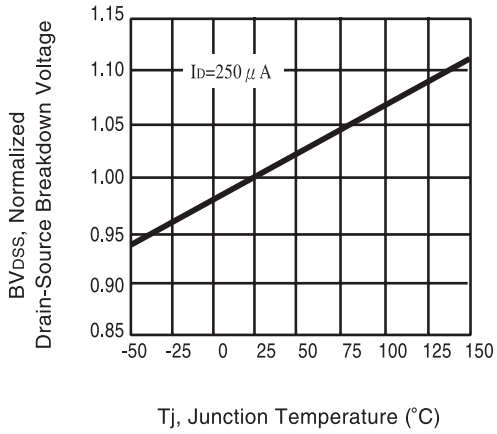


Figure 6. Breakdown Voltage Variation with Temperature

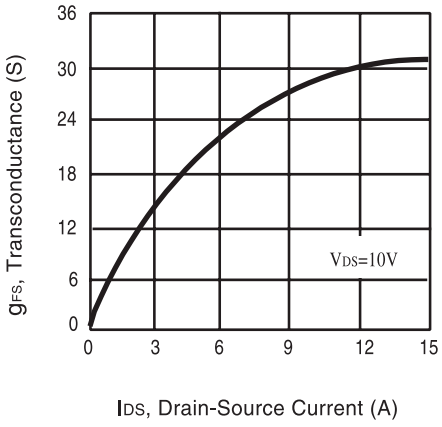


Figure 7. Transconductance Variation with Drain Current

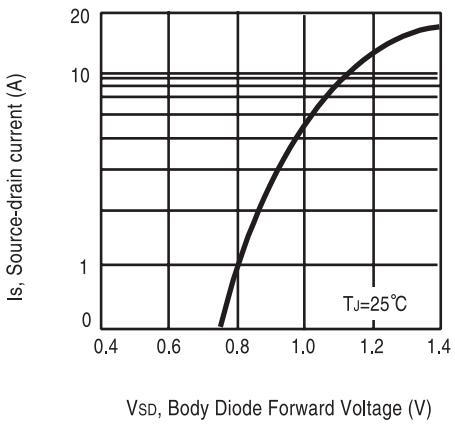


Figure 8. Body Diode Forward Voltage Variation with Source Current

P-Channel

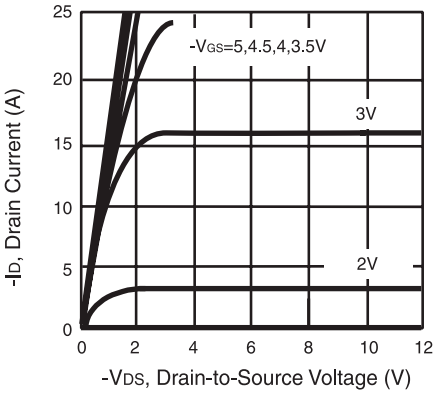


Figure 1. Output Characteristics

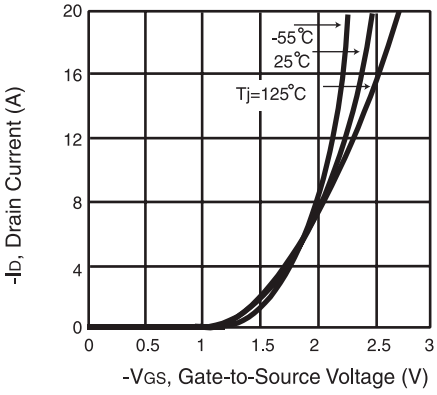


Figure 2. Transfer Characteristics

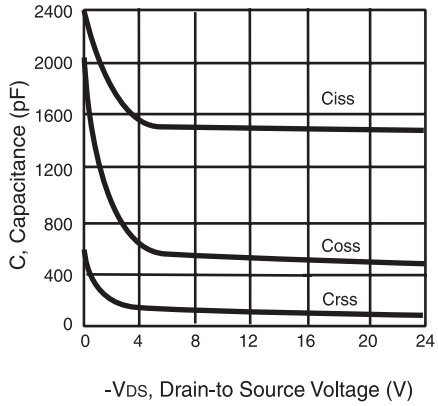


Figure 3. Capacitance

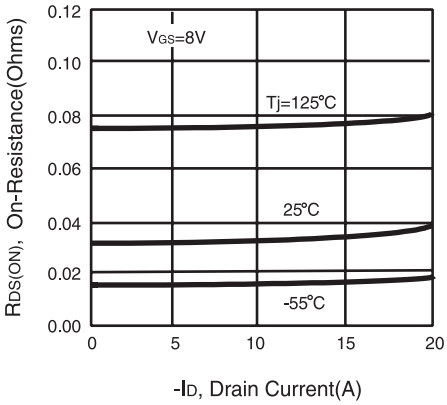


Figure 4. On-Resistance Variation with Drain Current and Temperature

P-Channel

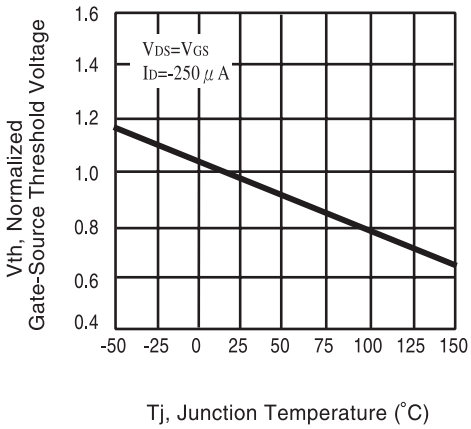


Figure 5. Gate Threshold Variation with Temperature

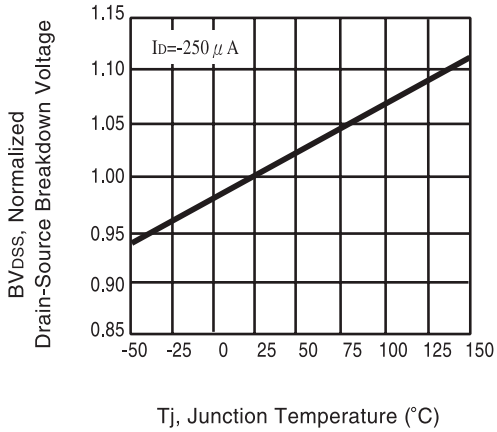


Figure 6. Breakdown Voltage Variation with Temperature

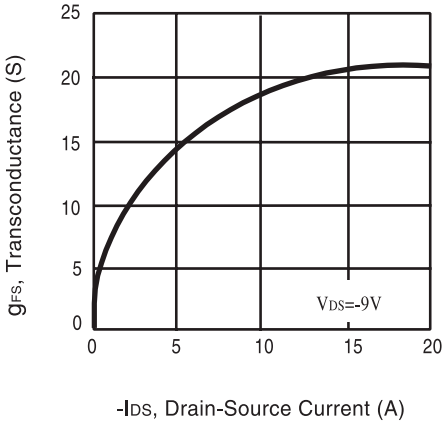


Figure 7. Transconductance Variation with Drain Current

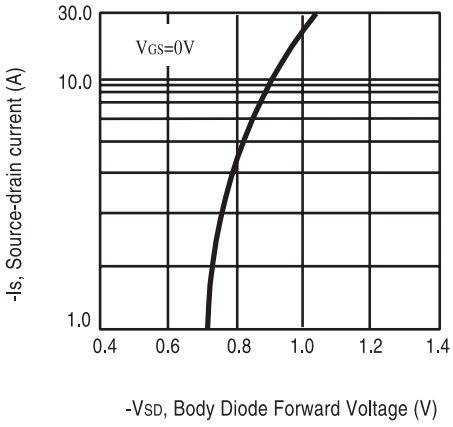


Figure 8. Body Diode Forward Voltage Variation with Source Current

N-Channel

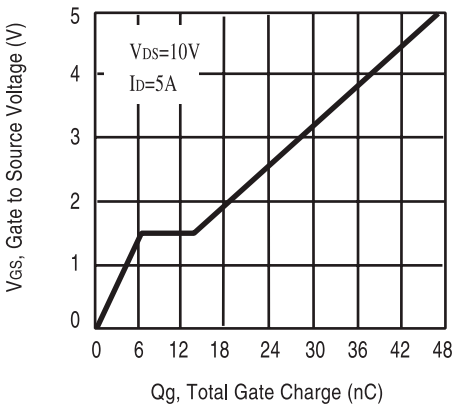


Figure 9. Gate Charge

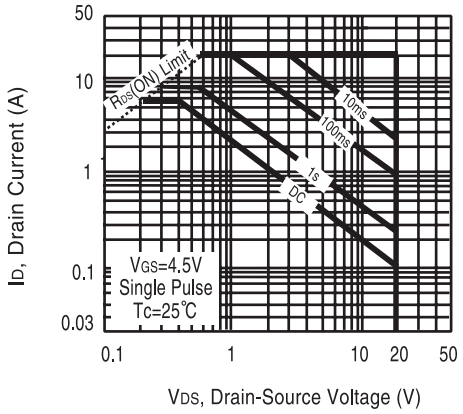
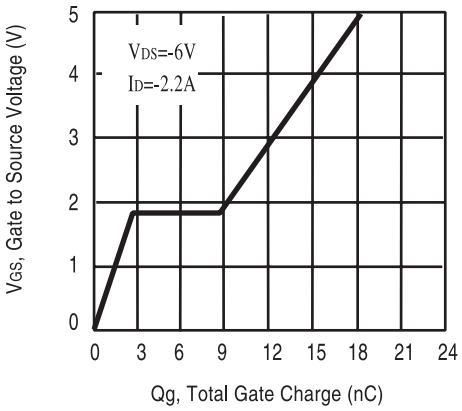


Figure 10. Maximum Safe Operating Area

P-Channel



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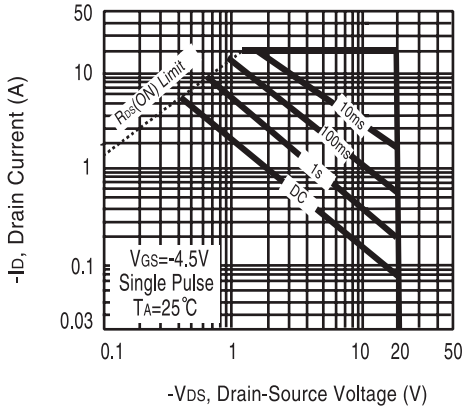

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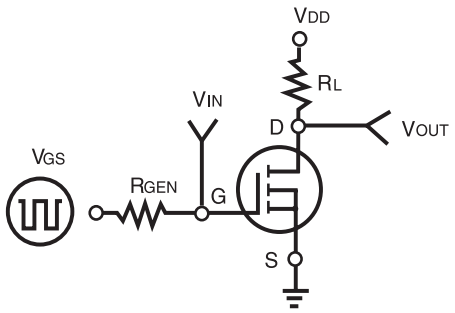

Figure 11. Switching Test Circuit

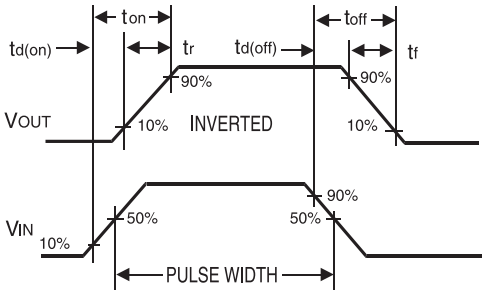

Figure 12. Switching Waveforms

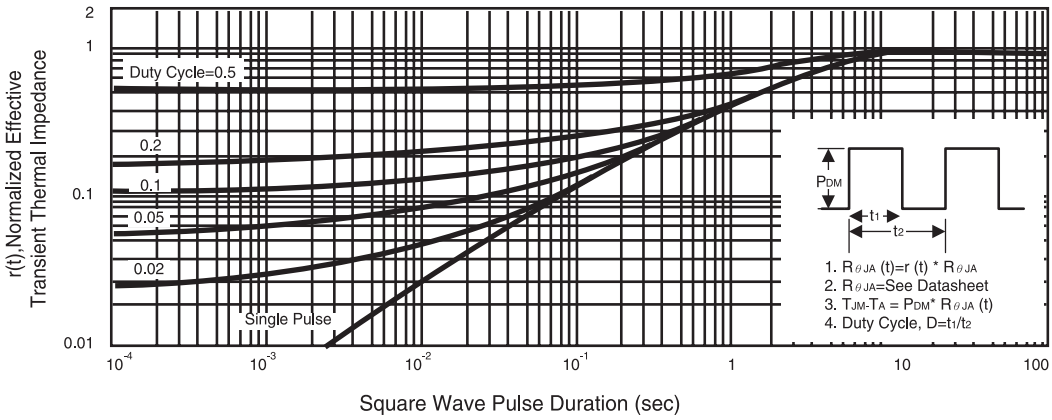

Figure 13. Normalized Thermal Transient Impedance Curve