AO4801A
Dual P-Channel Enhancement Mode Field Effect Transistor

General Description

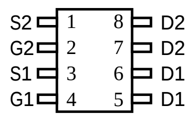
The AO4801A uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use as a load switch or in PWM applications. Standard Product AO4801A is Pb-free (meets ROHS & Sony 259 specifications)

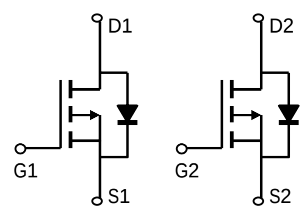
Features

V_{DS} (V) = -30V
I_D =-5.6A (V_{GS} = 10V)
$R_{DS(ON)}$ < 42mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 52mΩ (V_{GS} = 4.5V)
$R_{DS(ON)}$ < 75mΩ (V_{GS} = 2.5V)

UIS TESTED!
Rg,Ciss,Coss,Crss Tested

SOIC-8
Top View





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	10 Sec	Steady State	Units
Drain-Source Voltage		V_{DS}	-30		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain Current [AF]	T_A=25°C	I_{DSM}	5.6	4.2	A
	T_A=70°C		4.5	3.4	
Pulsed Drain Current [B]		I_{DM}	-30		
Avalanche Current [B]		I_{AR}	11		
Repetitive avalanche energy L=0.3mH [B]		E_{AR}	18		mJ
Power Dissipation	T_A=25°C	P_{DSM}	2.0	1.1	W
	T_A=70°C		1.3	0.7	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	48	62.5	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		74	110	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	35	40	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250uA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	uA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-0.6	-0.95	-1.3	V
$I_{D(ON)}$	On state drain current	V_{GS}=-4.5V, V_{DS}=-5V	-25			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-5.6A		34	42	mΩ
		T_J=125°C		48	60	
		V_{GS}=-4.5V, I_D=-3.5A		41	52	mΩ
		V_{GS}=-2.5V, I_D=-2.5A		60	75	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-5.6A		14		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.74	-1	V
I_S	Maximum Body-Diode Continuous Current				-2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		933	1200	pF
C_{oss}	Output Capacitance			108		pF
C_{rss}	Reverse Transfer Capacitance			81		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		6	9	Ω
SWITCHING PARAMETERS						
Q_g(4.5V)	Total Gate Charge	V_{GS}=-4.5V, V_{DS}=-15V, I_D=-5.6A		9.3	12.2	nC
Q_{gs}	Gate Source Charge			1.5		nC
Q_{gd}	Gate Drain Charge			3.7		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=2.7Ω, R_{GEN}=6Ω		5.2		ns
t_r	Turn-On Rise Time			6.8		ns
$t_{D(off)}$	Turn-Off DelayTime			42		ns
t_f	Turn-Off Fall Time			15		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-5.6A, dI/dt=100A/µs		21	28	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-5.6A, dI/dt=100A/µs		14.3		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.
F. The current rating is based on the t≤ 10s junction to ambient thermal resistance rating.
Rev0: Mar. 2007

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

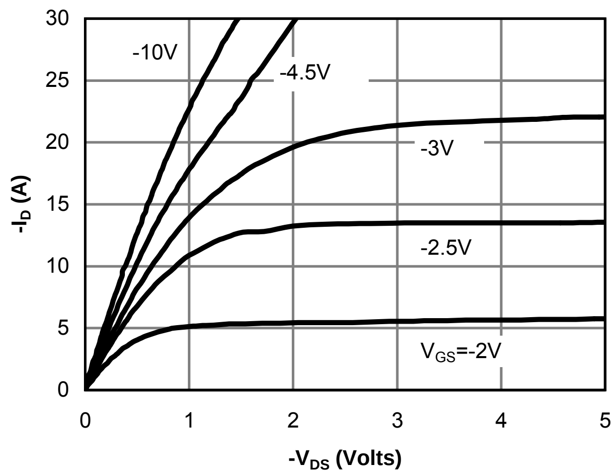


Figure 1: On-Region Characteristics

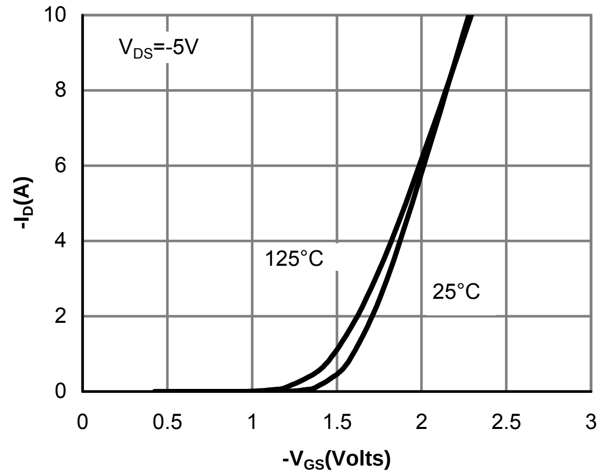


Figure 2: Transfer Characteristics

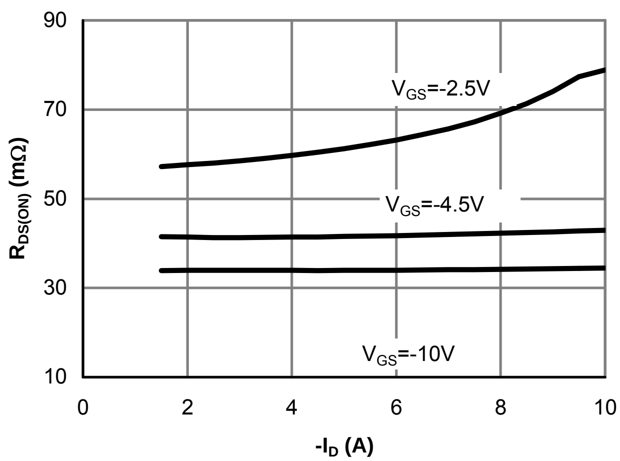


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

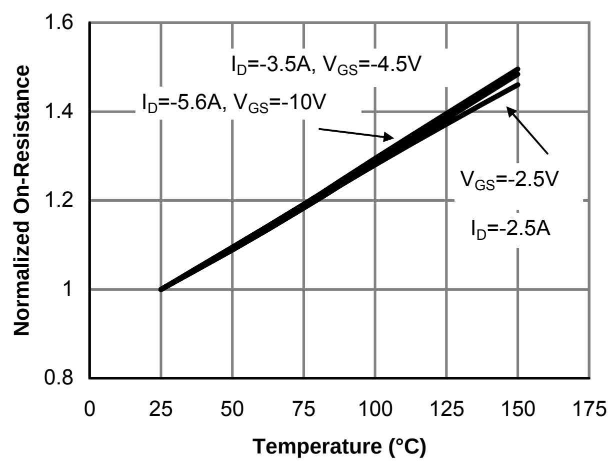


Figure 4: On-Resistance vs. Junction Temperature

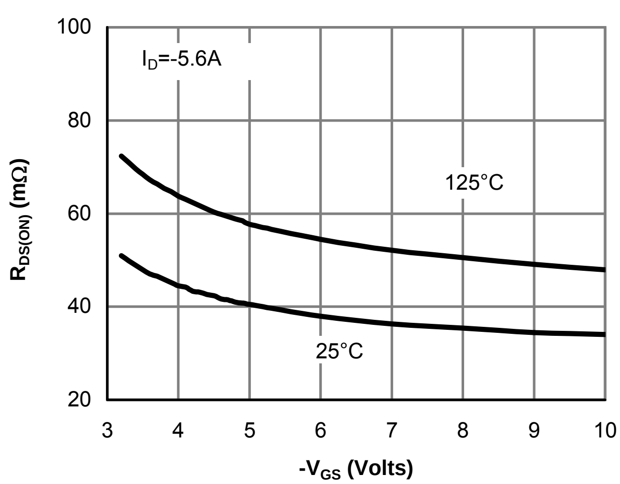


Figure 5: On-Resistance vs. Gate-Source Voltage

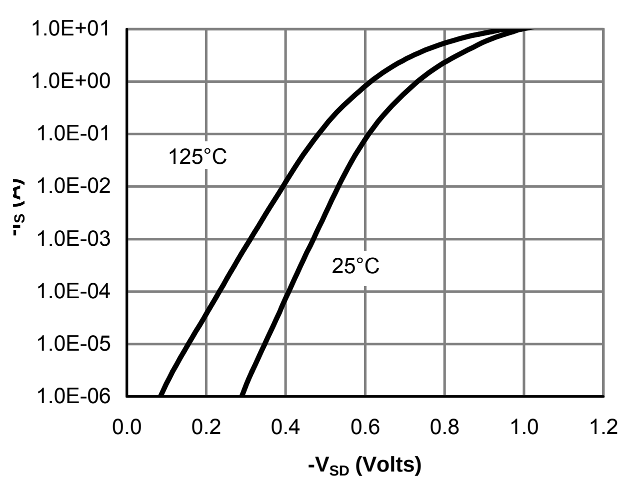


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

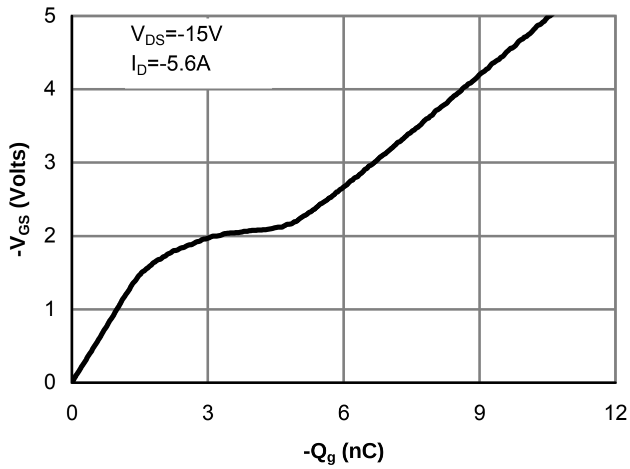


Figure 7: Gate-Charge Characteristics

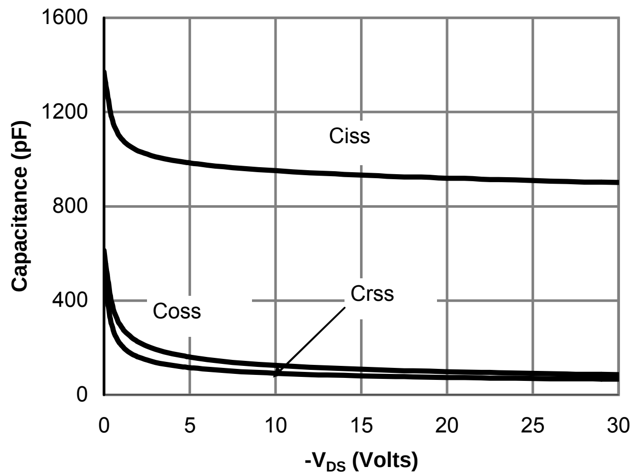


Figure 8: Capacitance Characteristics

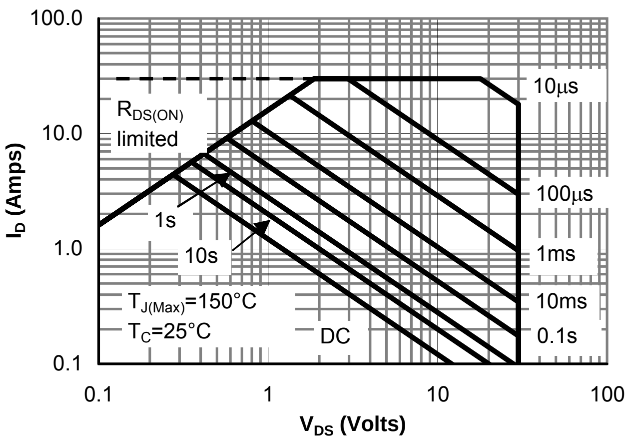


Figure 9: Maximum Forward Biased Safe Operating Area (NoteE)

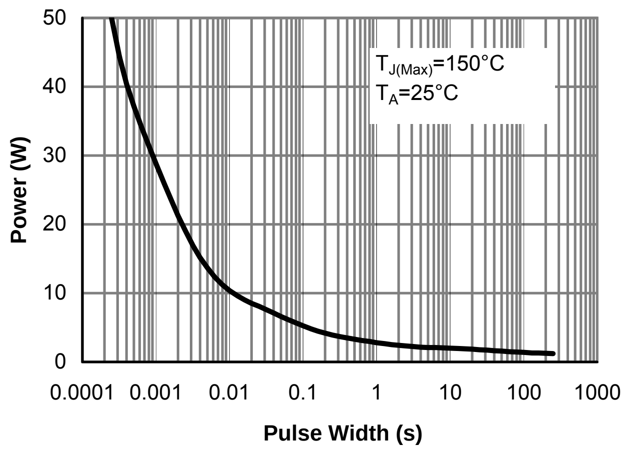


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

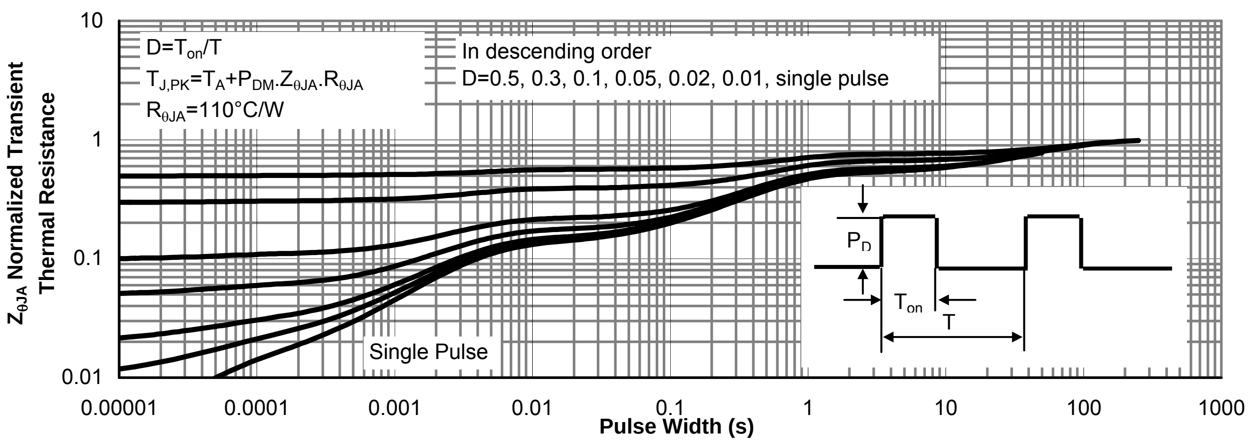


Figure 11: Normalized Maximum Transient Thermal Impedance