DATA SHEET

SKY77148 PA Module for CDMA2000 (450–460 MHz)

Applications

- Digital cellular (CDMA2000)
- Wireless Local Loop (WLL)

Features

- Low voltage positive bias supply
  - (3.2 V to 4.2 V)
- Good linearity
- High efficiency across wide dynamic range
- Dual-mode operation
- 7-pin package
  - 6 mm x 6 mm x 1.5 mm
- Power down control
- Low power state control
- CDMA2000

NEW

Skyworks offers lead (Pb)-free "environmentally friendly" packaging that is RoHS compliant (European Parliament for the Restriction of Hazardous Substances).

Description

The SKY77148 Power Amplifier Module (PAM) is a fully matched 7-pin surface mount module developed for Code Division Multiple Access (CDMA2000) handset and Wireless Local Loop applications. This small and efficient power amplifier packs full coverage of the 450–460 MHz bandwidth into a single compact package. The device meets the stringent CDMA2000 linearity requirements to and exceeding 29 dBm output power. A low current pin (VCONT) provides improved efficiency for the low RF power range of operation.

The single Gallium Arsenide (GaAs) Microwave Monolithic Integrated Circuit (MMIC) contains all active circuitry within the module, which includes on-board bias circuitry as well as input and interstage matching circuits. Output match into a 50 Ω load is realized off-chip within the module package to optimize efficiency and power performance. This device is manufactured with Skyworks' GaAs Heterojunction Bipolar Transistor (HBT) process that provides for all positive voltage DC supply operation while maintaining high efficiency and good linearity. Primary bias to the SKY77148 is supplied directly from a three-cell Ni-Cd, a single-cell Li-Ion, or other suitable battery with a rated output in the 3.2 to 4.2 volt range. Setting the voltage on the low current reference pin to zero volts accomplishes power down. No external supply side switch is needed as typical "off" leakage is a few microamperes with full primary voltage from the battery.

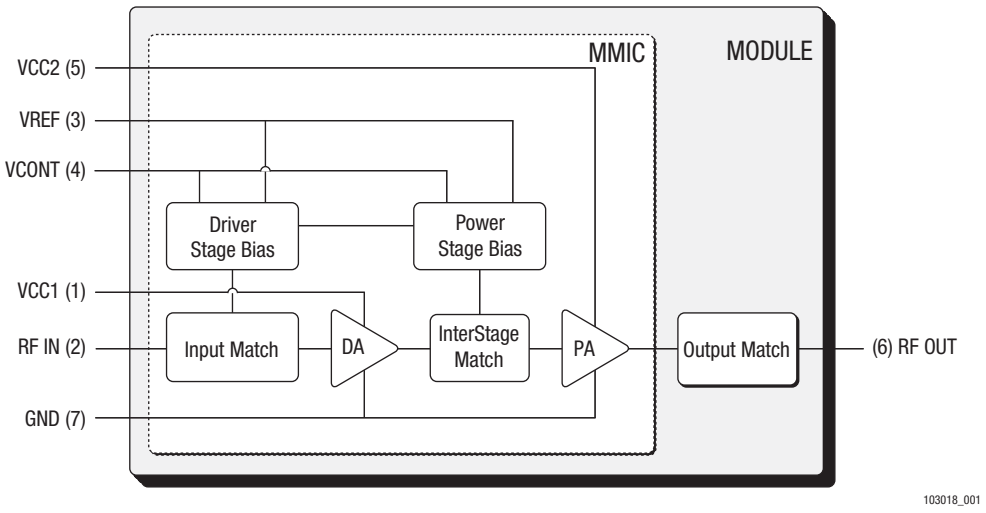


Figure 1. Functional Block Diagram

Electrical Specifications

The following tables list the electrical characteristics of the SKY77148 Power Amplifier Module. Table 1 lists the absolute maximum ratings while Table 2 shows the recommended operating conditions to achieve the performance characteristics listed in Table 4. A truth table for the power ranges is shown in Table 3.

Table 1. Absolute Maximum Ratings [1]

Parameter		Symbol	Minimum	Nominal	Maximum	Unit
RF Input Power		PIN	—	0.0	6.0	dBm
Supply Voltage		VCC	—	3.4	6.0	Volts
Reference Voltage		VREF	—	3.0	3.1	Volts
Case Temperature [2]	Operating	TC	–30	+25	+110	°C
	Storage	TSTG	–55	—	+125	

[1] No damage assuming only one parameter at a time is set at limit with all other parameters set at or below nominal value.

[2] Case Operating Temperature refers to the temperature of the GROUND PAD at the underside of the package.

Table 2. Recommended Operating Conditions

Parameter		Symbol	Minimum	Nominal	Maximum	Unit
Supply Voltage		VCC	3.2	3.4	4.2	Volts
Reference Voltage		VREF	2.95	3.0	3.05	Volts
Control voltage	LOW	VCONT	2.5	—	3.0	Volts
	HIGH	VCONT	0.0	—	0.5	
Operating Frequency		FO	450.0	455	460	MHz
Case Operating Temperature		TC	–30	+25	+85	°C

Table 3. Power Range Truth Table

Power Mode	VREF	VCONT	Range
High Power	3.0 V	0.0–0.5 V	16 dBm to 29 dBm
Low Power	3.0 V	2.5–3.0 V	≤ 16 dBm
Shut Down	0.0 V	0.0 V	—

Table 4. Electrical Specifications for CDMA Nominal Operating Conditions [1]

Characteristics		Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain conditions	Digital Mode	G_{LOW}	$V_{CONT} \geq 2.5$ V P_O = 16 dBm	24.5	26.5	28.2	dB
		G_{HIGH}	$V_{CONT} \leq 0.5$ V P_O = 29 dBm	29.0	31.0	32.5	
Power Added Efficiency	Digital Mode	PAE_{LOW}	$V_{CONT} \geq 2.5$ V P_O = 16 dBm	7.0	8.0	—	%
		PAE_{HIGH}	$V_{CONT} \leq 0.5$ V P_O = 29 dBm	35.0	38.0	—	
Total Supply Current		I_{CC_LOW}	P_O = 16 dBm	—	155	175	mA
		I_{CC_HIGH}	P_O = 29 dBm	—	650	705	
Quiescent Current		I_{Q_LOW}	$V_{CONT} \geq 2.5$ V	50	65	75	mA
		I_{Q_HIGH}	$V_{CONT} \leq 0.5$ V	70	90	105	
Reference Current		I_{REF}		—	0.75	1.0	mA
Control Current		I_{CONT}	V_{CONT} = 2.5 V	—	.95	1.2	µA
Total Supply Current in Power-down Mode		I_{PD}	V_{CC} = 3.4 V V_{REF} = 0 V	—	2.0	4.5	µA
Adjacent Channel Power [2,3]	885 kHz offset	$ACP1_{LOW}$	$V_{CONT} \geq 2.5$ V $P_O \leq$ 16 dBm	—	–47.0	–45.5	dBc
		$ACP1_{HIGH}$	$V_{CONT} \leq 0.5$ V $P_O \leq$ 29 dBm	—	–50.0	–46.5	
	1.98 MHz offset	$ACP2_{LOW}$	$V_{CONT} \geq 2.5$ V $P_O \leq$ 16 dBm	—	–65.0	–58.0	
		$ACP2_{HIGH}$	$V_{CONT} \leq 0.5$ V $P_O \leq$ 29 dBm	—	–59.0	–57.0	
Harmonic Suppression	Second	F_O2	$P_O \leq$ 29 dBm	—	–45.0	–35.0	dBc
	Third	F_O3	$P_O \leq$ 29 dBm	—	–55.0	–40.0	
Noise Power in RX Band 460-470 MHz		RxBN	$P_O \leq$ 29 dBm	—	–129	–127	dBm/Hz
Noise Figure		NF		—	5.0	5.5	dB
Input Voltage Standing Wave Ratio		VSWR		—	1.6:1	2.0:1	—
Stability (Spurious output)		S	5:1 VSWR all phases	—	—	–65.0	dBc
Ruggedness—No damage [4]		Ru	$P_O \leq$ 29 dBm	10:1	—	—	VSWR

[1] Unless otherwise specified:
V_{CC} = +3.4 V,
V_{REF} = +3.0 V,
Freq = 455 MHz,
T_C = 25 °C

[2] ACP is specified per CDMA2000 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

[3] CDMA2000 is configured as DCCH = 9600, SCHO = 9600, PCH (Walsh 0) = –3.75 dB, and Peak-to-Average Ratio (CCDF = 1%) = 4.5 dB.

[4] All phases, time = 10 seconds.

Table 5. Electrical Specifications for CDMA Recommended Operating Conditions [1]

Characteristics		Symbol	Condition	Minimum	Maximum	Unit
Gain conditions	Digital Mode	G_{LOW}	$V_{CONT} \geq 2.5$ V $P_O = 16$ dBm	24.5	29.0	dB
		G_{HIGH}	$V_{CONT} \leq 0.5$ V $P_O = 29$ dBm	28.0	34.0	
Adjacent Channel Power [2,3]	885 kHz offset	$ACP1_{LOW}$	$V_{CONT} \geq 2.5$ V $P_O \leq 16$ dBm	—	–44.0	dBc
		$ACP1_{HIGH}$	$V_{CONT} \leq 0.5$ V $P_O \leq 28.5$ dBm	—	–44.0	
	1.98 MHz offset	$ACP2_{LOW}$	$V_{CONT} \geq 2.5$ V $P_O \leq 16$ dBm	—	–58.0	
		$ACP2_{HIGH}$	$V_{CONT} \leq 0.5$ V $P_O \leq 28.5$ dBm	—	–56.0	
Harmonic Suppression	Second	F_O2	$P_O \leq 29$ dBm	—	–35.0	dBc
	Third	F_O3	$P_O \leq 29$ dBm	—	–40.0	
Noise Power in RX Band 460-470 MHz		RxBN	$P_O \leq 29$ dBm	—	–126.5	dBm/Hz
Noise Figure		NF		—	6.5	dB
Input Voltage Standing Wave Ratio		VSWR		—	2.0:1	—
Stability (Spurious output)		S	5:1 VSWR all phases		–60.0	dBc
Ruggedness—No damage [4]		Ru	$P_O \leq 29$ dBm	10:1		VSWR

[1] Per Table 2.

[2] ACP is specified per CDMA2000 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

[3] CDMA2000 is configured as DCCH = 9600, SCHO = 9600, PCH (Walsh 0) = –3.75 dB, and Peak-to-Average Ratio (CCDF = 1%) = 4.5 dB.

[4] All phases, time = 10 seconds.

Characterization Data

The graphs from Figure 2 through Figure 8 illustrate the characteristics of a typical SKY77148 power amplifier designed for operation in the PCS frequency band (450–460 MHz). This amplifier was selected by characterizing a group of devices and choosing a part with average electrical performance for both nominal and the full range of recommended operating conditions, including worst case limits.

The graphs illustrate the digital signal characteristics of the SKY77148. Shown are power sweep characteristics for key performance parameters over temperature and frequency, up to 29.5 dBm output power. The data was taken up to and including 16 dBm output power with the bias mode control pin setting of V_{CONT} = 2.5 volts. Beyond 16 dBm output power, the V_{CONT} was set to zero volts.

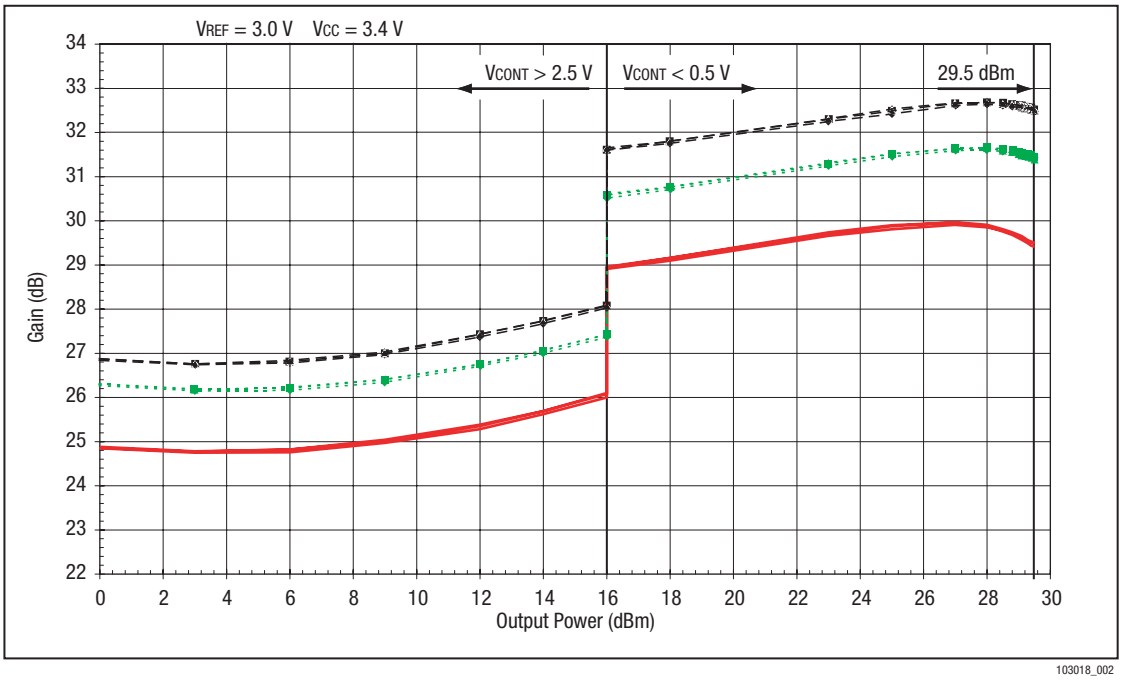


Figure 2. SKY77148 Gain vs. Output Power

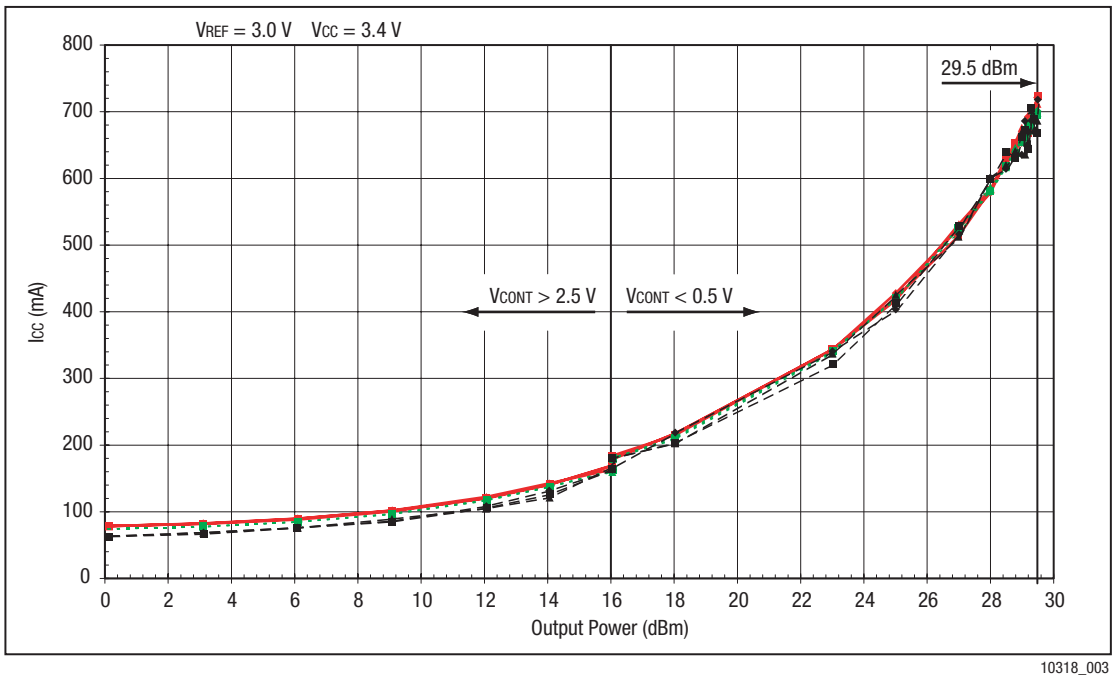


Figure 3. SKY77148 Primary Bias current vs. Output Power

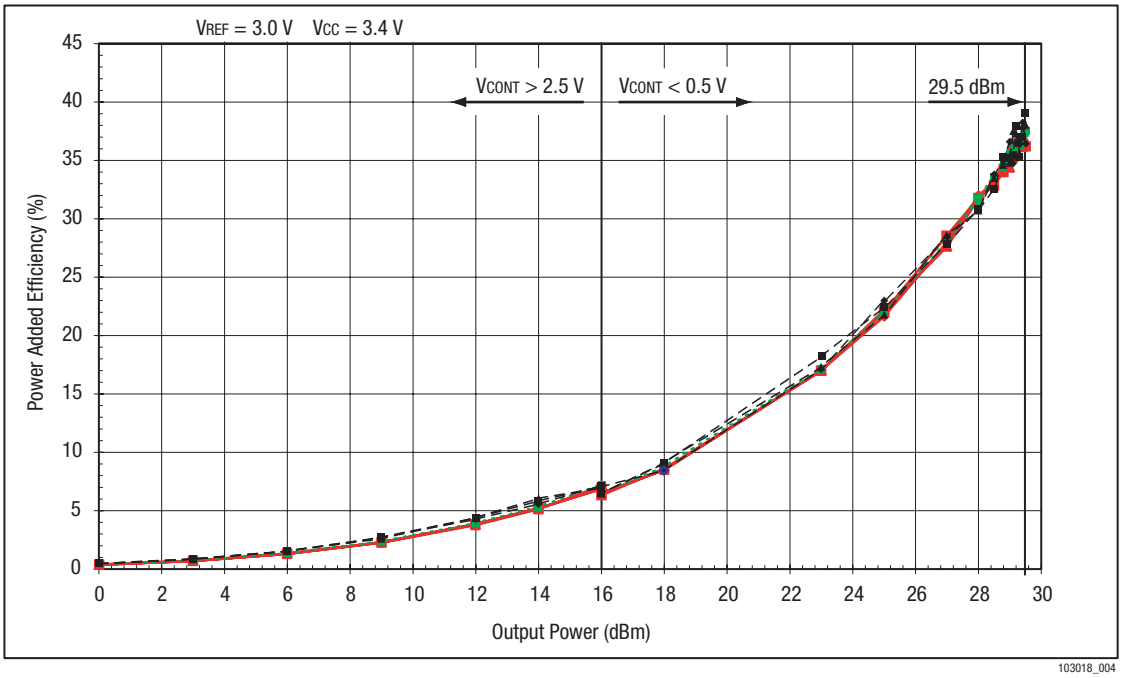


Figure 4. SKY77148 Power Added Efficiency vs. Output Power

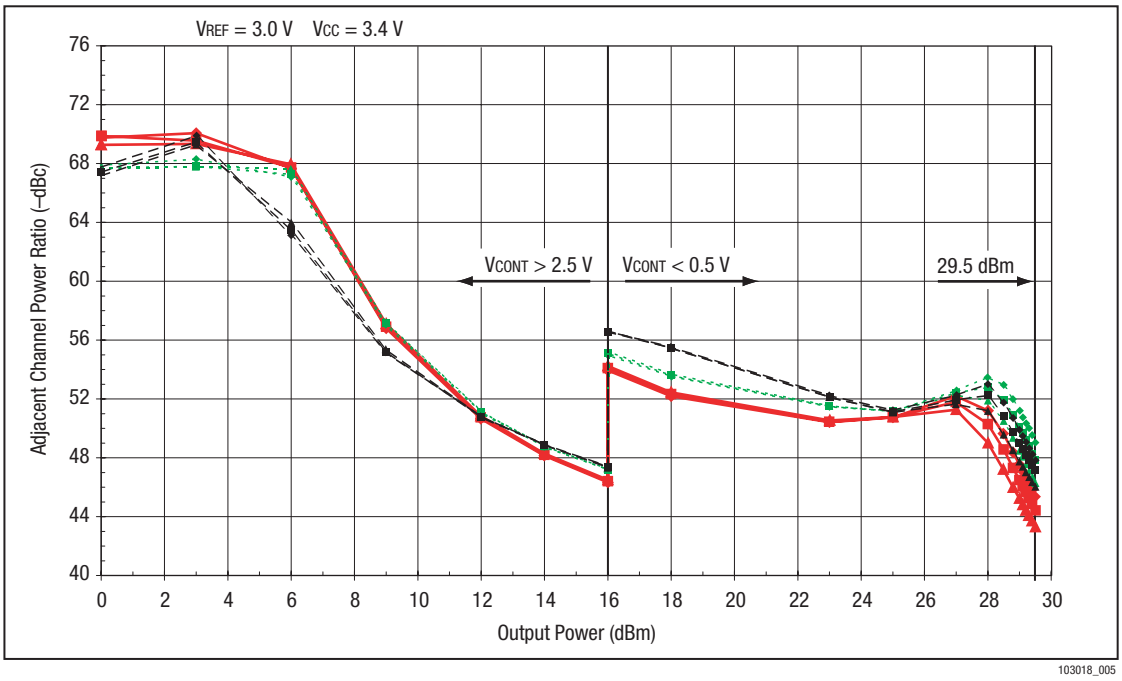


Figure 5. SKY77148 Adjacent Channel Power (885 kHz) vs. Output Power

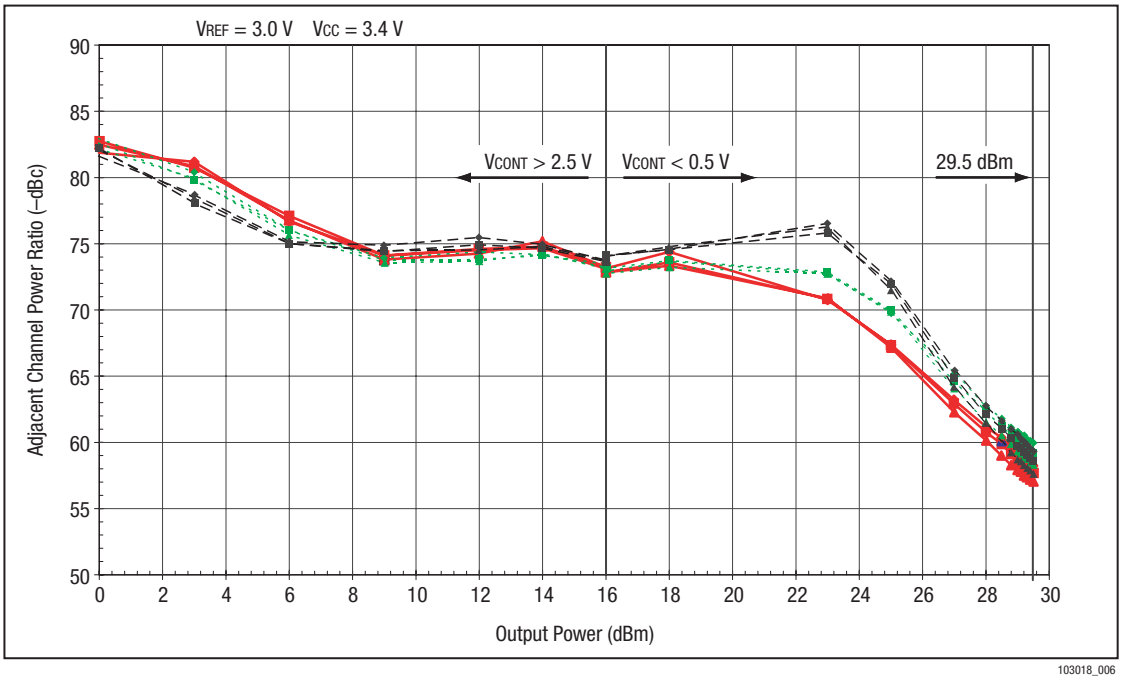


Figure 6. SKY77149 Adjacent Channel Power (1.98 MHz) vs. Output Power

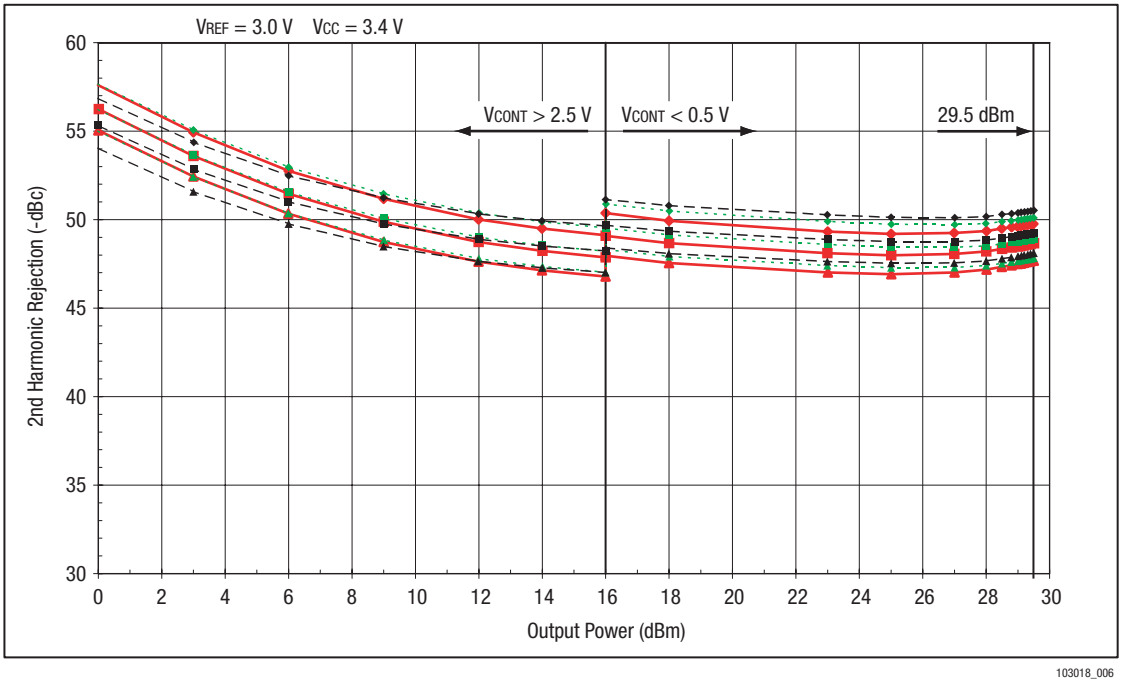


Figure 7. SKY77149 Second Harmonic Rejection vs. Output Power

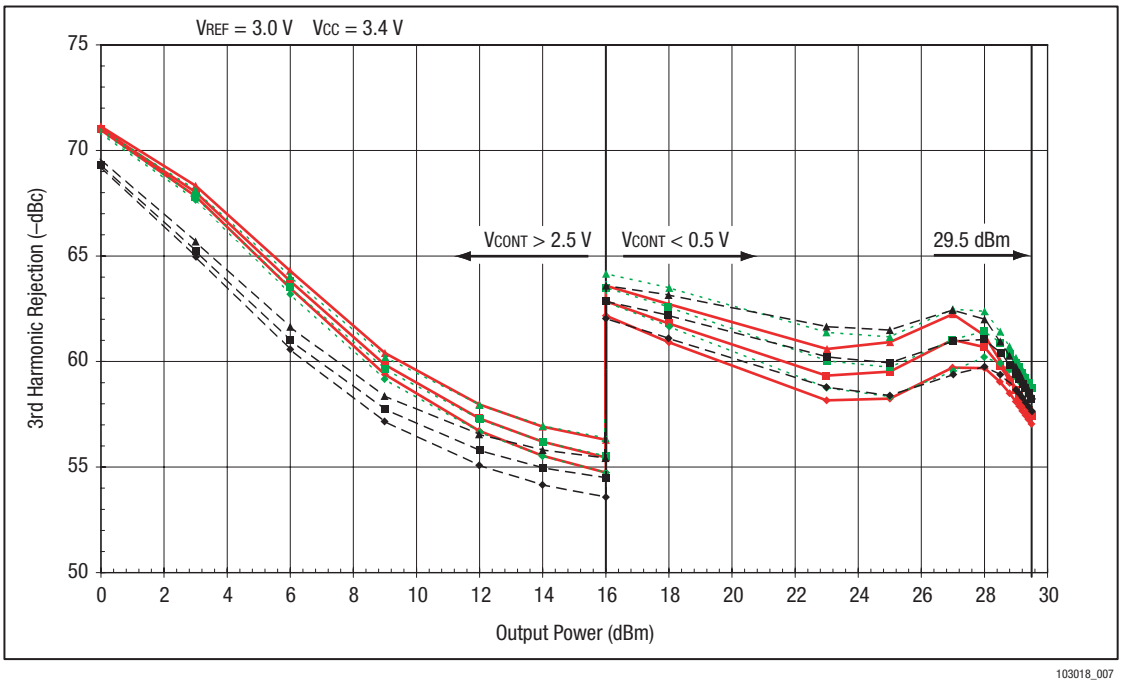
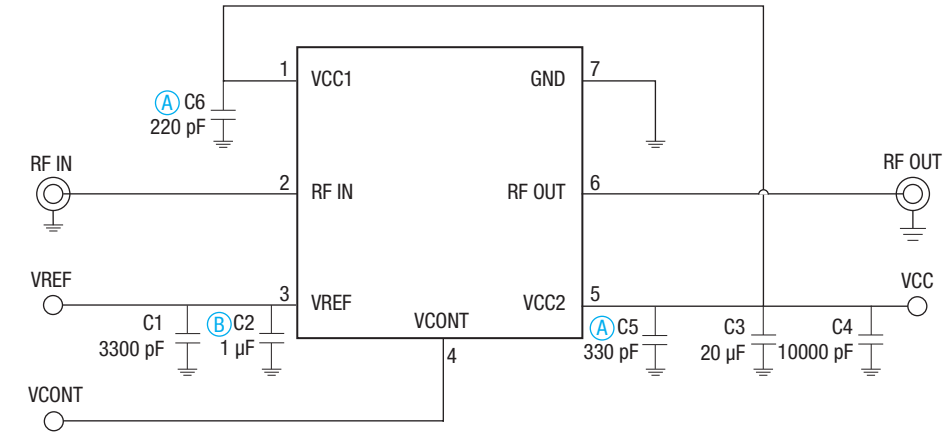


Figure 8. SKY77148 Third Harmonic Rejection vs. Output Power

Evaluation Board Description

The evaluation board is a platform for testing and interfacing design circuitry. To accommodate the interface testing of the SKY77148, the evaluation board schematic and assembly diagrams are included for preliminary analysis and design. In Figure 9, the basic schematic of the evaluation board for the 450 MHz to 460 MHz range is shown.



A Place caps at closest proximity to PA module with the capacitor grounds directly connected to the PAM grounds.
B (decoupling capacitor) is not required when a voltage regulator is present.

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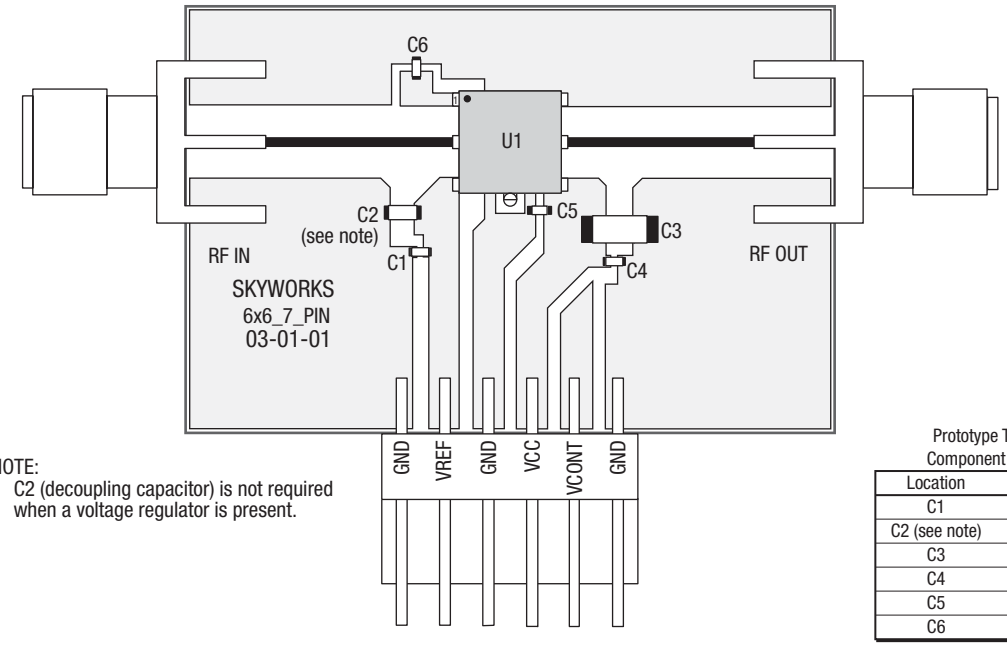
Figure 9. Evaluation Board Schematic



NOTE:
C2 (decoupling capacitor) is not required when a voltage regulator is present.

Prototype Test-Board
Component Description

Location	Value
C1	3300 pF
C2 (see note)	1 µF
C3	20 µF
C4	10,000 pF
C5	330 pF
C6	220 pF

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Figure 10. Evaluation Board Assembly Diagram

Package Dimensions and Pin Descriptions

The SKY77148 is a multi-layer laminate base, overmold encapsulated modular package designed for surface-mounted solder attachment to a printed circuit board. Figure 11 is a mechanical drawing of the pad layout for this package. Figure 12 provides a recommended phone board layout footprint for the PAM to help the designer attain optimum thermal conductivity, good grounding, and minimum RF discontinuity for the 50-ohm terminals. Figure 13 shows each pin name and the pin numbering convention, which starts with pin 1 in the upper left, as indicated, and increments counter-clockwise around the package. Figure 14 illustrates typical case markings.

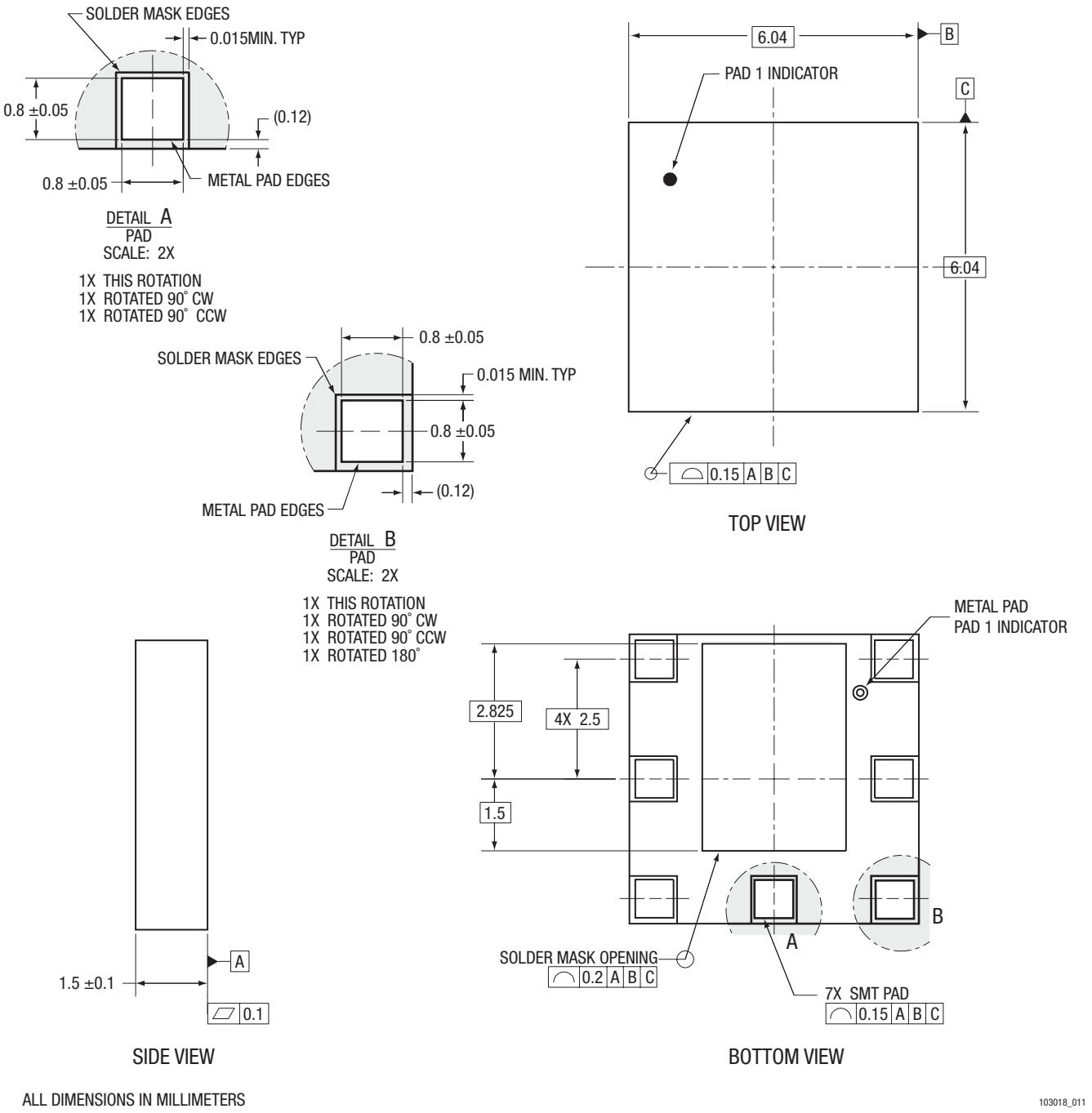
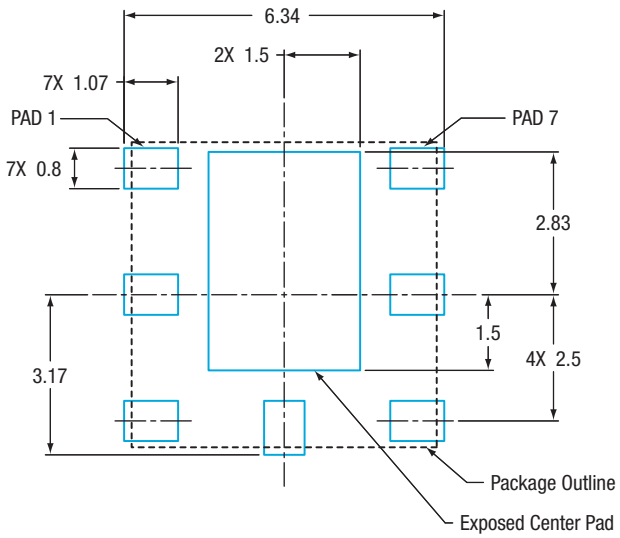
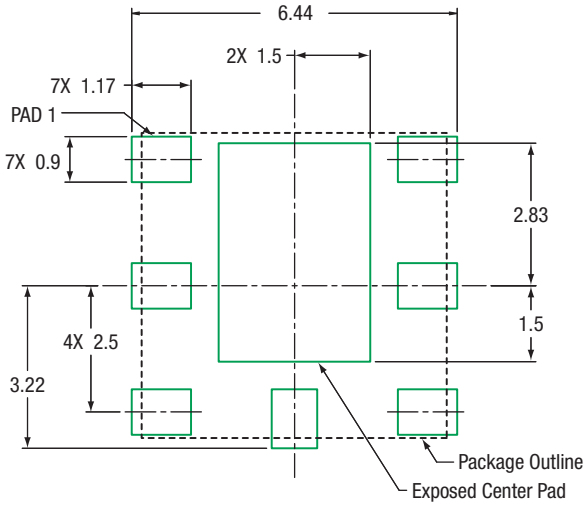


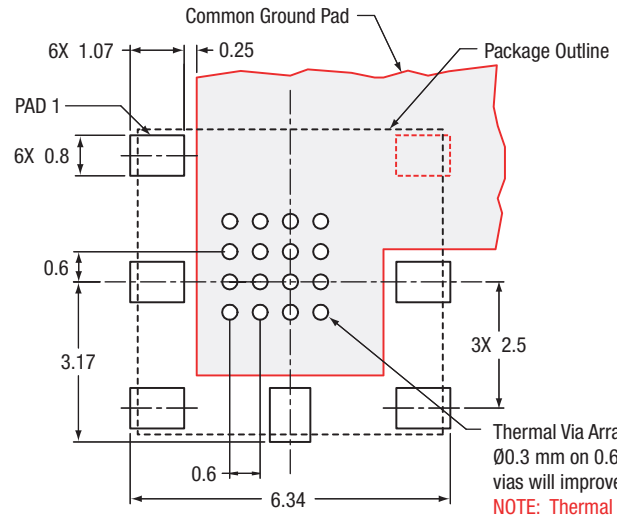
Figure 11. SKY77148 Package Dimensions



STENCIL APERTURE
TOP VIEW
STENCIL APERTURE SIZE FOR THE CENTER GROUND PAD SHOULD BE 80% TO 100% (BY AREA) OF THE SOLDER MASK OPENING.



SOLDER MASK OPENING
TOP VIEW



METALLIZATION
TOP VIEW
THE SHADED AREA REPRESENTS THE MERGER OF THE CENTER GROUND PAD AND 1 INDIVIDUAL I/O GROUND PAD. THEREFORE, THE NUMBER OF PLACES DIMENSIONED WILL BE REDUCED.

Thermal Via Array under PA areas. Ø0.3 mm on 0.6 pitch. Additional vias will improve thermal performance.
NOTE: Thermal vias should be tented and filled with solder mask, 30–35 µm Cu plating is recommended.

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Figure 12. Phone PCB Layout Footprint for 6 x 6, 7-Pad Package – SKY77148

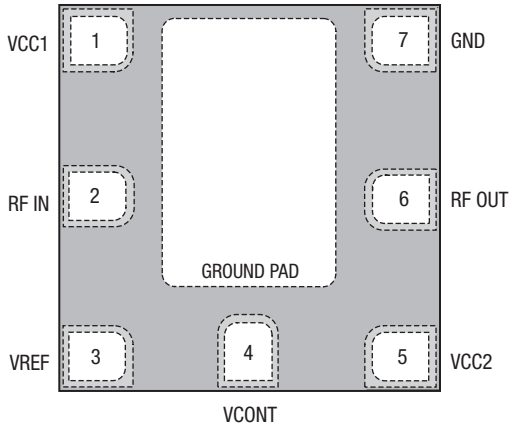

Figure 13. Pin Names and Configuration

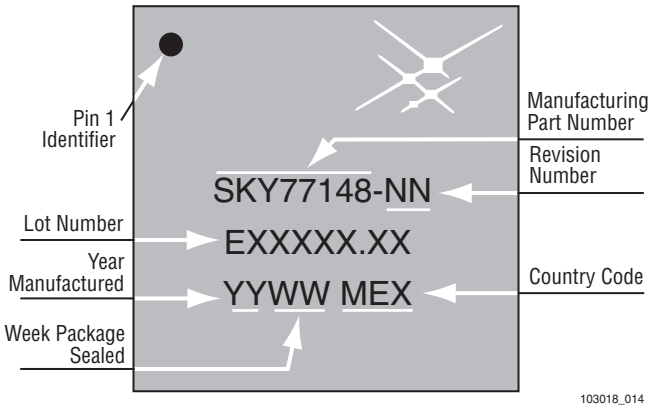

Figure 14. Typical Case Markings

Package and Handling Information

Because of its sensitivity to moisture absorption, this device package is baked and vacuum packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY77148 is capable of withstanding an MSL 3/235 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 3 °C per second; maximum temperature should not exceed 235 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 235 °C for more than 10 seconds. For details on attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to Skyworks Application Note: *PCB Design and SMT Assembly/Rework,* Document Number 101752. Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J-STD–020*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to Skyworks Application Note: *Tape and Reel,* Document Number 101568.

Electrostatic Discharge Sensitivity

The SKY77148 is a Class 1 device. Figure 15 lists the Electrostatic Discharge (ESD) immunity level for each pin of the SKY77148 product. The numbers in Figure 15 specify the ESD threshold level for each pin where the I-V curve between the pin and ground starts to show degradation. The ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model. If ESD damage threshold magnitude is found to consistently exceed 2000 volts on a given pin, this so is indicated. If ESD damage threshold below 2000 volts is measured for either polarity, numbers are indicated that represent worst case values observed in product characterization.

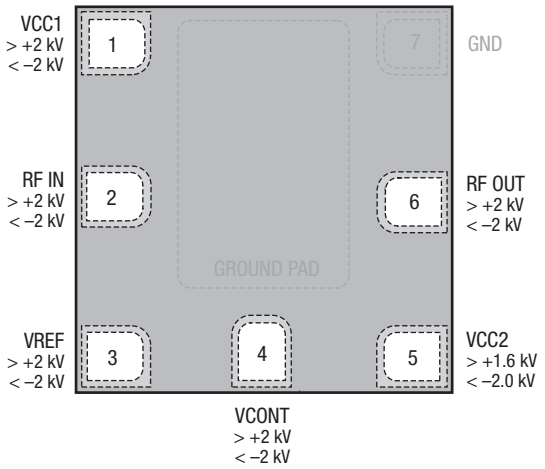

Figure 15. ESD Sensitivity Areas (Top View)

Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards, which fail devices only after “the pin fails the electrical specification limits” or “the pin becomes completely non-functional”. Skyworks employs most stringent criteria to fail devices as soon as the pin begins to show any degradation on a curve tracer. To avoid ESD damage, either latent or visible, it is very important that the product assembly and test areas follow the Class 1 ESD handling precautions listed in Table 6.

Table 6. Precautions for Handling GaAs IC-based Products to Avoid Induced Damage

Personnel Grounding	Wrist Straps Conductive Smocks, Gloves and Finger Cots Antistatic ID Badges
Facility	Relative Humidity Control and Air Ionizers Dissipative Floors (less than 10^9 Ω to GND)
Protective Workstation	Dissipative Table Tops Protective Test Equipment (Properly Grounded) Grounded Tip Soldering Irons Conductive Solder Suckers Static Sen sors
Protective Packaging and Transportation	Bags and Pouches (Faraday Shield) Protective Tote Boxes (Conductive Static Shielding) Protective Trays Grounded Carts Protective Work Order Holders

Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
SKY77148	SKY77148	–15	7-pin MCM L4 6 x 6 x 1.5 mm	–30 °C to +85 °C

Revision History

Revision	Level	Date	Description
A		October 19, 2005	Initial Release
B		May 12, 2006	Revise: Tables 2, 4

References

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752

Application Note: Tape and Reel Information – RF Modules, Document Number 101568

JEDEC Standard J–STD015–020