Ordering number : EN8767A

SANYO Semiconductors
DATA SHEET

LA6548ND — Monolithic Linear IC For CD Players and Recorders Four-Channel Driver IC

Overview

The LA6548ND is a four-channel driver IC for CD players and recorders (four BTL amplifier channels).

Functions

- Four BTL connection power amplifier channels
- I_O max 0.7A
- Built-in level shifters
- Muting circuit (on/off control of all outputs)
  (This circuit applies to the BTL amplifier circuits. It does not control operation of the regulator.)
- Built-in regulator (provides a 3.3V output using an external pnp transistor)
- Thermal protection circuit (thermal shutdown circuit)

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		14	V
Maximum output current	I_O max	For each of the channel 1 to 4 outputs	0.7	A
Maximum input voltage	V_{IN}		13	V
Muting pin application voltage	VMUTE		13	V
Allowable power dissipation	Pd max		1.5	W
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-55 to +150	°C

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Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	$V_{CC}1$		4.6 to 13	V
Supply voltage 2	$V_{CC}2$	Only used by the BTL amplifiers (Not used by the 3.3V regulator circuit)	3.9 to 13	V

Electrical Characteristics at Ta = 25°C, $V_{CC}1 = V_{CC}2 = 6V$, VREF = 1.65V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Overall Characteristics						
No-load current drain, on state	$I_{CC}ON$	All outputs on, MUTE : high		20	40	mA
No-load current drain, off state	$I_{CC}OFF$	All outputs off, MUTE : low		15	35	mA
Thermal shutdown circuit operating temperature	TSD	(Design guarantee value *1)	150	175	200	°C
Output Amplifier Block						
Output offset voltage	V_{OFF}	The voltage difference between each of the + or - outputs.	-50		50	mV
VREF input voltage range	$V_{IN}VREF$		1.3		V_{CC}-1.5	V
Output voltage	V_O	The voltage across the outputs when $R_L = 8\Omega$	2.6	3		V
Voltage gain, input to output	VG	The voltage gain from an input to the corresponding +/- outputs.*2		9		dB
Slew rate	SR	(Design guarantee value *1)		0.15		V/μs
Muting on voltage	VMUTE	The voltage at which the output on/off state changes		1.2		V
Power Supply Block (Using a 2SB632K)						
3.3V power supply voltage		$I_O = 200mA$	3.13	3.3	3.47	V
Line regulation	$\Delta V_O LIN$	$4.6V \le V_{CC} \le 12V$		40	100	mV
Load regulation	$\Delta V_O LOAD$	$5mA \le I_O \le 200mA$		50	150	mV
Reset Block						
RESET pin high-level voltage	$V_O RH$		3.08	3.25	3.42	V
RESET pin low-level voltage	$V_O RL$	ISRL = 2mA, Cd-GND		100	200	mV
RESET pin threshold voltage	V_{RT}	*4		2.8		V
RESET pin hysteresis	V_{HYS}	*5	40	80	160	mV
RESET pin output delay time	td	Cd = 0.1μF		10		ms

*1 : These parameters are not tested.

2 : The gain from input to output when only the V_{IN} pins are used.

*3 : The MUTE pin voltage when the output changes between the on and off states. When the MUTE pin is high, all the BTL amplifiers will be on, and the when MUTE is low, all the BTL amplifiers will be off.

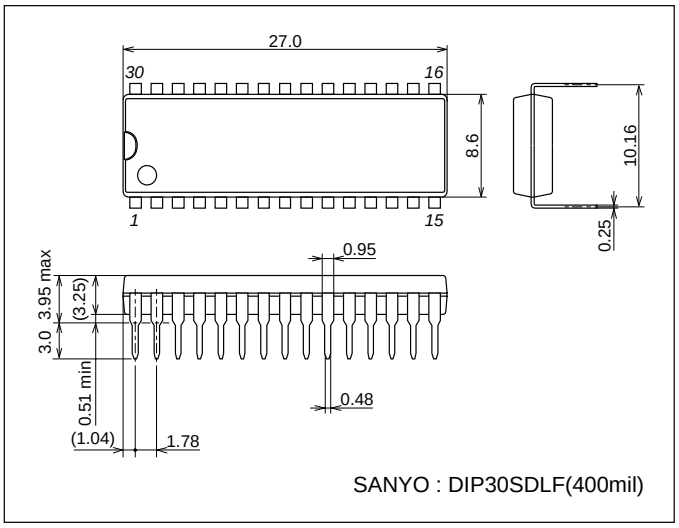
*4 : The 3.3V regulator voltage when the RESET pin goes from high to low.

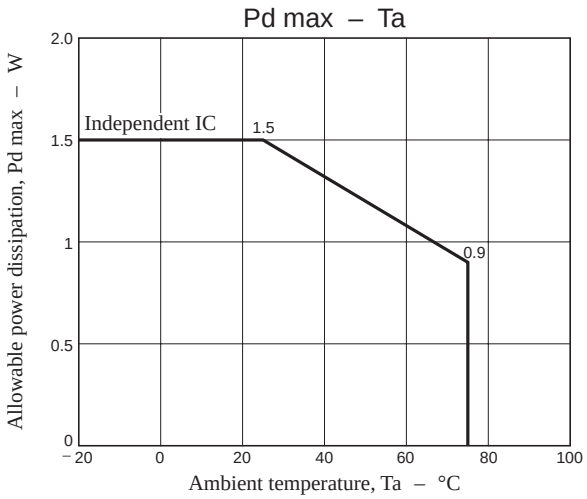
*5 : The 3.3V regulator voltage difference between the RESET pin going from high to low the RESET pin going from low to high. That is, the hysteresis.

Package Dimensions

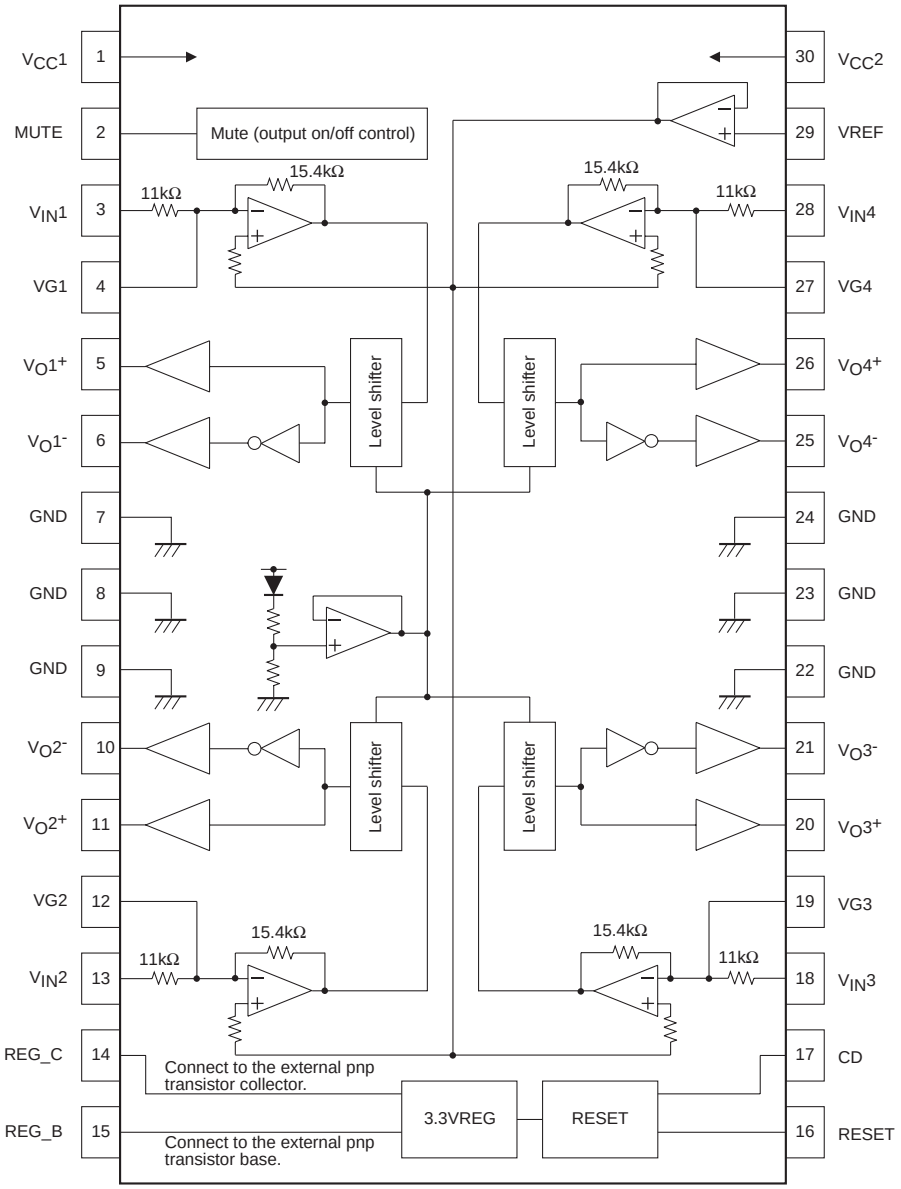
unit : mm (typ)

3307





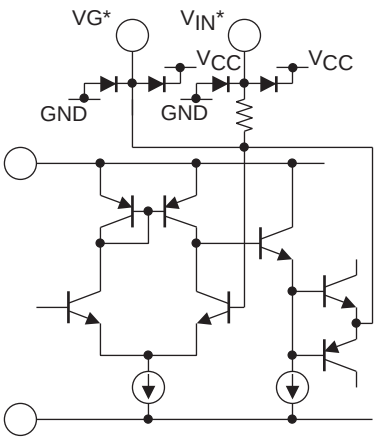
Block Diagram



Pin Functions

Pin No.	Pin	Description
1	$V_{CC}1$	Power supply (This pin is shorted to $V_{CC}2$ (pin 30)
2	MUTE	Output on/off control
3	$V_{IN}1$	Channel 1 input
4	VG1	Channel 1 input (Gain setting)
5	V_O1^+	Channel 1 output (+)
6	V_O1^-	Channel 1 output (-)
7	GND	GND pin
8	GND	GND pin
9	GND	GND pin
10	V_O2^-	Channel 2 output (-)
11	V_O2^+	Channel 2 output (+)
12	VG2	Channel 2 input (Gain setting)
13	$V_{IN}2$	Channel 2 input
14	REG_C	Connect this pin to the external pnp transistor collector. (This is the 3.3V regulator output)
15	REG_B	Connect this pin to the external pnp transistor base.
16	RESET	Reset output
17	CD	Connection for the reset delay time setting capacitor
18	$V_{IN}3$	Channel 3 input
19	VG3	Channel 3 input (Gain setting)
20	V_O3^+	Channel 3 output (+)
21	V_O3^-	Channel 3 output (-)
22	GND	GND pin
23	GND	GND pin
24	GND	GND pin
25	V_O4^-	Channel 4 output (-)
26	V_O4^+	Channel 4 output (+)
27	VG4	Channel 4 input (Gain setting)
28	$V_{IN}4$	Channel 4 input
29	VREF	Reference voltage input
30	$V_{CC}2$	Power supply (This pin is shorted to $V_{CC}1$ (pin 1)

Equivalent Circuits

Pin No.	Pin	Description	Equivalent circuit
3 4 13 12 18 19 28 27	$V_{IN}1$ VG1 $V_{IN}2$ VG2 $V_{IN}3$ VG3 $V_{IN}4$ VG4	Input pins.	

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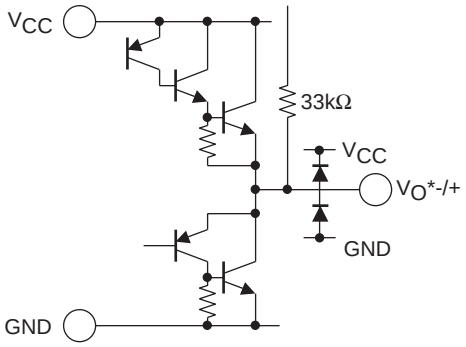
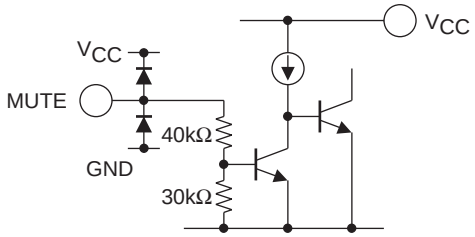
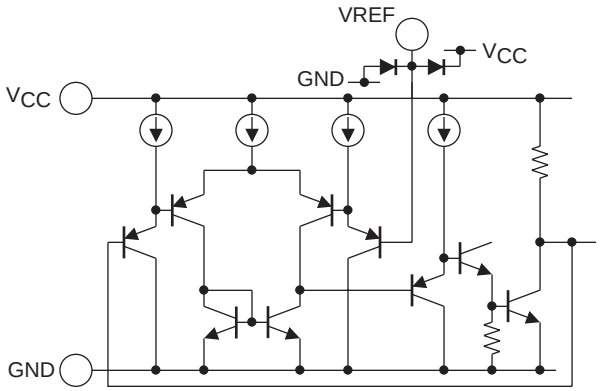
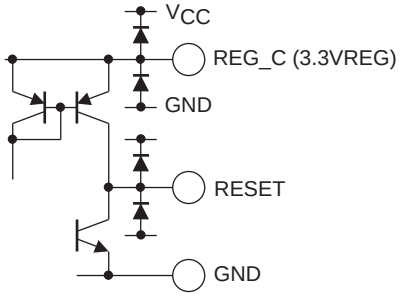
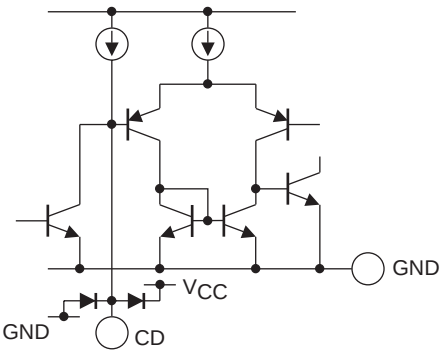
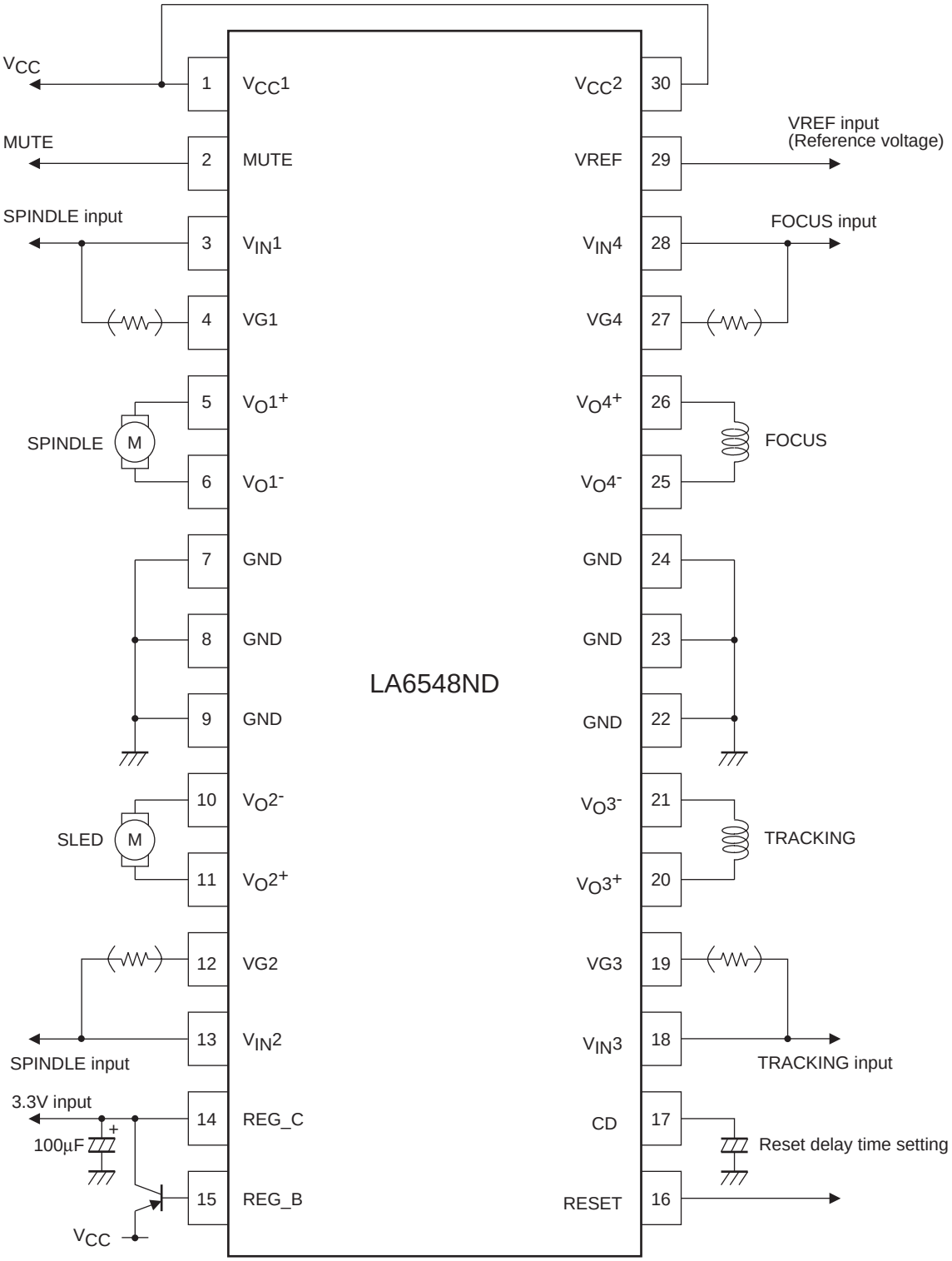
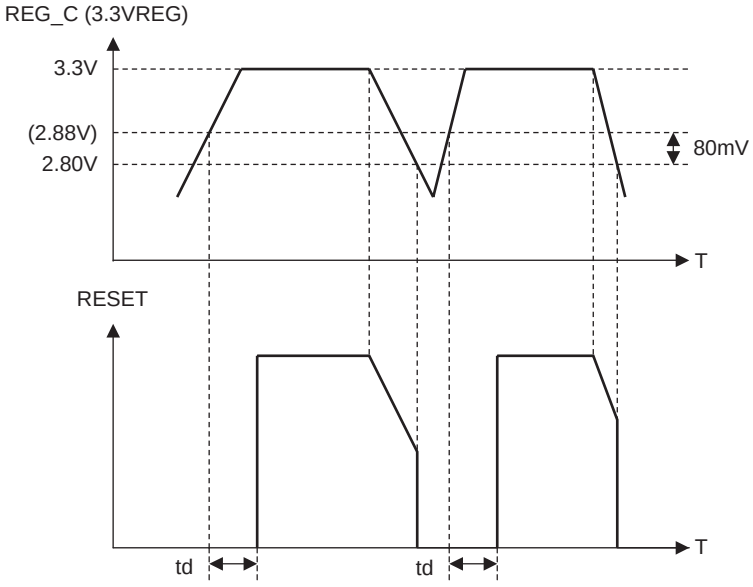
Pin No.	Pin	Description	Equivalent circuit
5 6 11 10 20 21 26 25	V_O1^+ V_O1^- V_O2^+ V_O2^- V_O3^+ V_O3^- V_O4^+ V_O4^-	Output pins.	
2	MUTE	Muting control input. The outputs will be on when the MUTE pin is at the high level. The outputs will be off when the MUTE pin is at the low level ; in particular, the outputs go to the high-impedance state at this time.	
29	VREF	Reference voltage input.	
16	RESET	Reset output. When REG C (3.3VREG) is high, RESET will be high. When REG C (3.3VREG) is low, RESET will be low. Details of Operating voltage see section Reset operation.	
17	CD	Reset output delay time setting. The delay time until the point the reset output switches from low to high is set by the capacitor connected between this pin and ground. Reference to Reset operation.	

Application Circuit Example



Reset Operation



*1 : td is the delay time. It is set by an external capacitor connected between the CD pin and ground).
*2 : The voltage at which RESET changes state is a typical value (voltage).