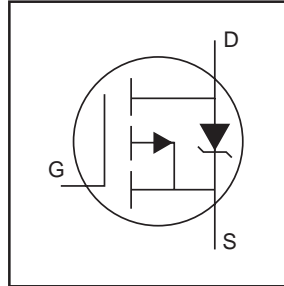


- Ultra Low On-Resistance
- Surface Mount (IRFR5305)
- Straight Lead (IRFU5305)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

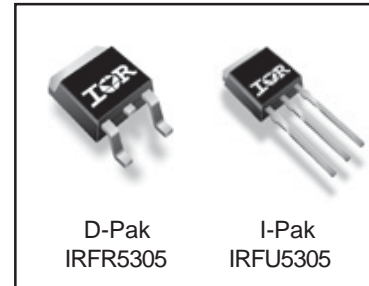


|                            |
|----------------------------|
| $V_{DSS} = -55V$           |
| $R_{DS(on)} = 0.065\Omega$ |
| $I_D = -31A$               |

## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET® Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



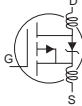
## Absolute Maximum Ratings

|                           | Parameter                                 | Max.               | Units |
|---------------------------|---|--------------------|-------|
| $I_D @ T_C = 25^\circ C$  | Continuous Drain Current, $V_{GS} @ -10V$ | -31                | A     |
| $I_D @ T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ -10V$ | -22                |       |
| $I_{DM}$                  | Pulsed Drain Current ①②                   | -110               |       |
| $P_D @ T_C = 25^\circ C$  | Power Dissipation                         | 110                | W     |
|                           | Linear Derating Factor                    | 0.71               | W/°C  |
| $V_{GS}$                  | Gate-to-Source Voltage                    | $\pm 20$           | V     |
| $E_{AS}$                  | Single Pulse Avalanche Energy ②③          | 280                | mJ    |
| $I_{AR}$                  | Avalanche Current ①③                      | -16                | A     |
| $E_{AR}$                  | Repetitive Avalanche Energy ①             | 11                 | mJ    |
| dv/dt                     | Peak Diode Recovery dv/dt ③④              | -5.0               | V/ns  |
| $T_J$                     | Operating Junction and                    | -55 to + 175       | °C    |
| $T_{STG}$                 | Storage Temperature Range                 |                    |       |
|                           | Soldering Temperature, for 10 seconds     |                    |       |
|                           | Mounting torque, 6-32 or M3 screw         | 10 lbf•in (1.1N•m) |       |

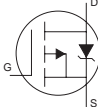
## Thermal Resistance

|                 | Parameter                        | Typ. | Max. | Units |
|-----------------|----------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case                 | —    | 1.4  | °C/W  |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB mount)* | —    | 50   |       |
| $R_{\theta JA}$ | Junction-to-Ambient**            | —    | 110  |       |

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

|  | Parameter                            | Min. | Typ.   | Max.  | Units | Conditions   |
|--|--------------------------------------|------|--------|-------|-------|--|
| V <sub>(BR)DSS</sub>                   | Drain-to-Source Breakdown Voltage    | -55  | —      | —     | V     | V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA  |
| ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub> | Breakdown Voltage Temp. Coefficient  | —    | -0.034 | —     | V/°C  | Reference to 25°C, I <sub>D</sub> = -1mA   |
| R <sub>DS(on)</sub>                    | Static Drain-to-Source On-Resistance | —    | —      | 0.065 | Ω     | V <sub>GS</sub> = -10V, I <sub>D</sub> = -16A ④                                      |
| V <sub>GS(th)</sub>                    | Gate Threshold Voltage               | -2.0 | —      | -4.0  | V     | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA                          |
| g <sub>fs</sub>                        | Forward Transconductance             | 8.0  | —      | —     | S     | V <sub>DS</sub> = -25V, I <sub>D</sub> = -16A⑥                                       |
| I <sub>DSS</sub>                       | Drain-to-Source Leakage Current      | —    | —      | -25   | μA    | V <sub>DS</sub> = -55V, V <sub>GS</sub> = 0V   |
|  |                                      | —    | —      | -250  |       | V <sub>DS</sub> = -44V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C                 |
| I <sub>GSS</sub>                       | Gate-to-Source Forward Leakage       | —    | —      | 100   | nA    | V <sub>GS</sub> = 20V  |
|  | Gate-to-Source Reverse Leakage       | —    | —      | -100  |       | V <sub>GS</sub> = -20V   |
| Q <sub>g</sub>                         | Total Gate Charge                    | —    | —      | 63    | nC    | I <sub>D</sub> = -16A  |
| Q <sub>gs</sub>                        | Gate-to-Source Charge                | —    | —      | 13    |       | V <sub>DS</sub> = -44V   |
| Q <sub>gd</sub>                        | Gate-to-Drain ("Miller") Charge      | —    | —      | 29    |       | V <sub>GS</sub> = -10V, See Fig. 6 and 13 ④⑥   |
| t <sub>d(on)</sub>                     | Turn-On Delay Time                   | —    | 14     | —     | ns    | V <sub>DD</sub> = -28V   |
| t <sub>r</sub>                         | Rise Time                            | —    | 66     | —     |       | I <sub>D</sub> = -16A  |
| t <sub>d(off)</sub>                    | Turn-Off Delay Time                  | —    | 39     | —     |       | R <sub>G</sub> = 6.8Ω  |
| t <sub>f</sub>                         | Fall Time                            | —    | 63     | —     |       | R <sub>D</sub> = 1.6Ω, See Fig. 10 ④⑥  |
| L <sub>D</sub>                         | Internal Drain Inductance            | —    | 4.5    | —     | nH    | Between lead,<br>6mm (0.25in.)<br>from package<br>and center of die contact ⑤        |
| L <sub>S</sub>                         | Internal Source Inductance           | —    | 7.5    | —     |       |  |
| C <sub>iss</sub>                       | Input Capacitance                    | —    | 1200   | —     | pF    | V <sub>GS</sub> = 0V   |
| C <sub>oss</sub>                       | Output Capacitance                   | —    | 520    | —     |       | V <sub>DS</sub> = -25V   |
| C <sub>rss</sub>                       | Reverse Transfer Capacitance         | —    | 250    | —     |       | f = 1.0MHz, See Fig. 5 ⑥   |

## Source-Drain Ratings and Characteristics

|                 | Parameter                                 | Min. | Typ. | Max. | Units | Conditions   |
|-----------------|---|------|------|------|-------|--|
| I <sub>S</sub>  | Continuous Source Current<br>(Body Diode) | —    | —    | -31  | A     | MOSFET symbol<br>showing the<br>integral reverse<br>p-n junction diode.<br> |
| I <sub>SM</sub> | Pulsed Source Current<br>(Body Diode) ①   | —    | —    | -110 |       |  |
| V <sub>SD</sub> | Diode Forward Voltage                     | —    | —    | -1.3 | V     | T <sub>J</sub> = 25°C, I <sub>S</sub> = -16A, V <sub>GS</sub> = 0V ④   |
| t <sub>rr</sub> | Reverse Recovery Time                     | —    | 71   | 110  | ns    | T <sub>J</sub> = 25°C, I <sub>F</sub> = -16A   |
| Q <sub>rr</sub> | Reverse Recovery Charge                   | —    | 170  | 250  | nC    | di/dt = -100A/μs ④⑥  |

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② V<sub>DD</sub> = -25V, starting T<sub>J</sub> = 25°C, L = 2.1mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = -16A. (See Figure 12)
- ③ I<sub>SD</sub> ≤ -16A, di/dt ≤ -280A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>,  
T<sub>J</sub> ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ This is applied for I-PAK, L<sub>S</sub> of D-PAK is measured between lead and center of die contact.
- ⑥ Uses IRF5305 data and test conditions.

\* When mounted on 1" square PCB (FR-4 or G-10 Material).  
For recommended footprint and soldering techniques refer to application note #AN-994.

\*\* Uses typical socket mount.

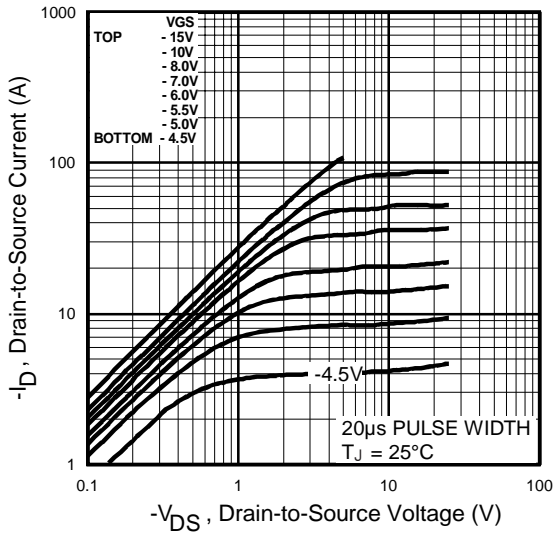


Fig 1. Typical Output Characteristics

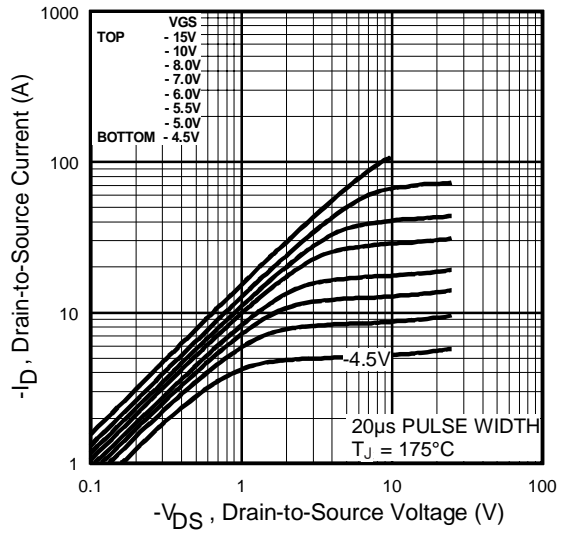


Fig 2. Typical Output Characteristics

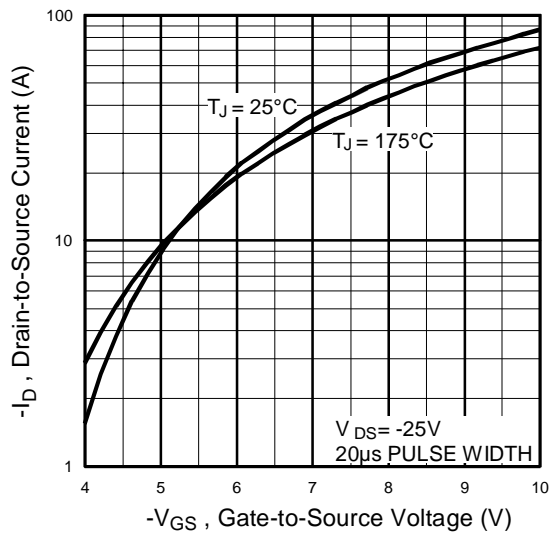


Fig 3. Typical Transfer Characteristics

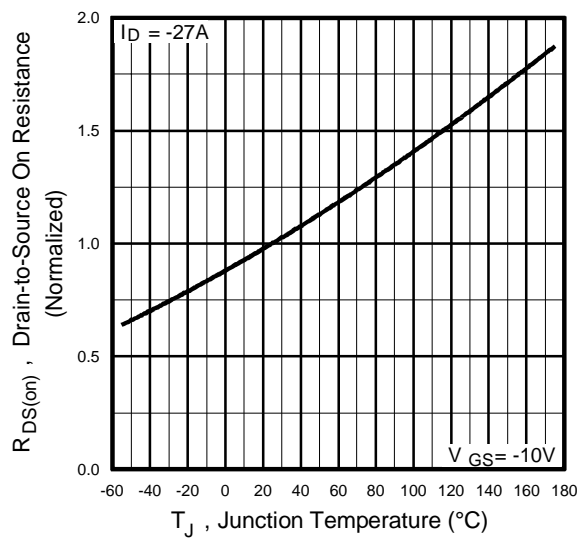
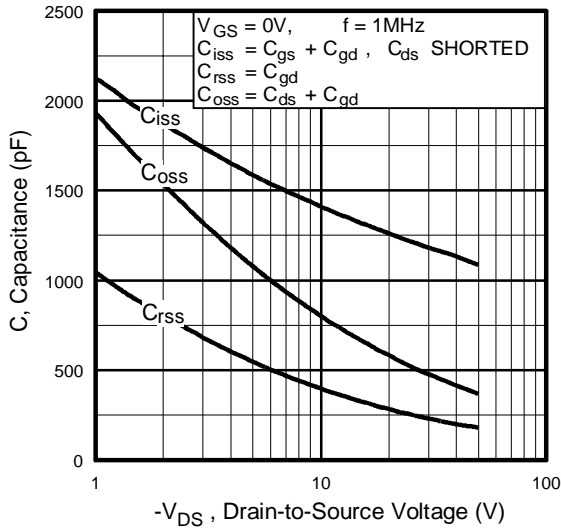
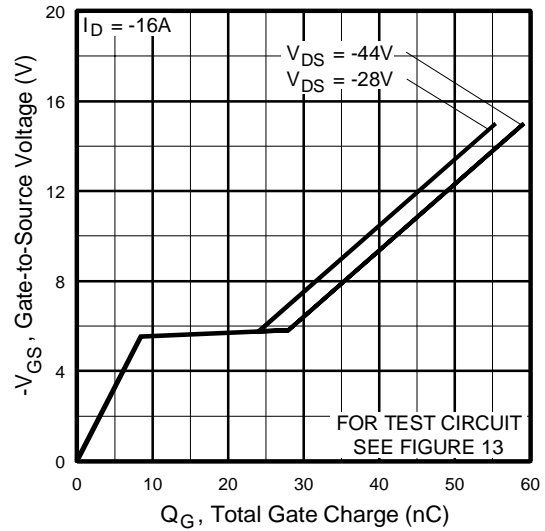


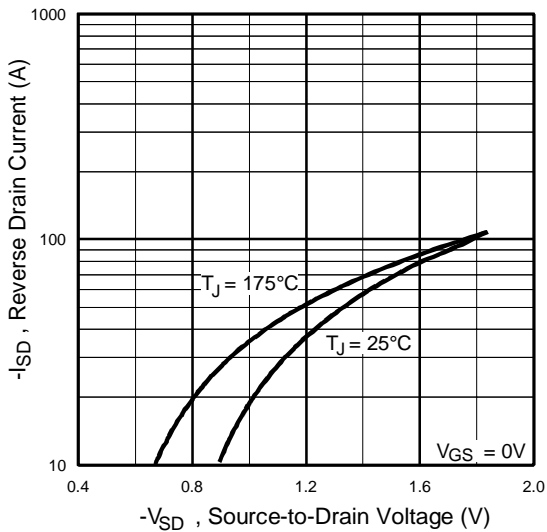
Fig 4. Normalized On-Resistance Vs. Temperature



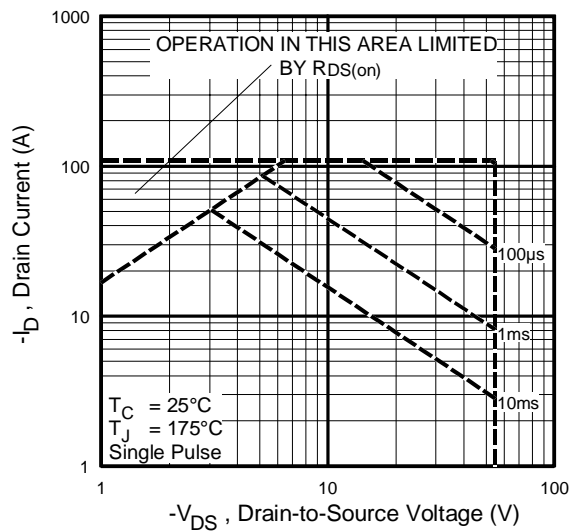
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

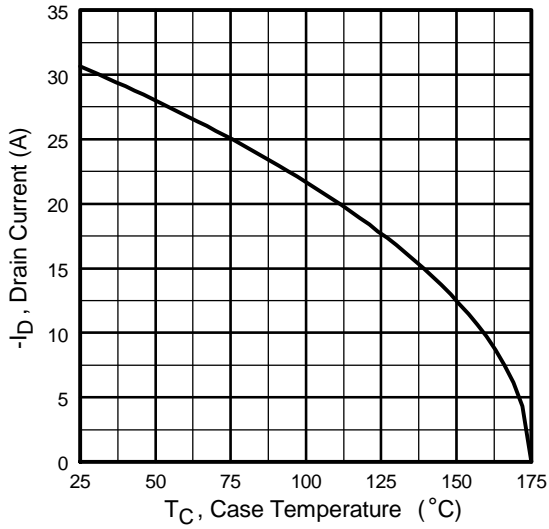


**Fig 7.** Typical Source-Drain Diode Forward Voltage

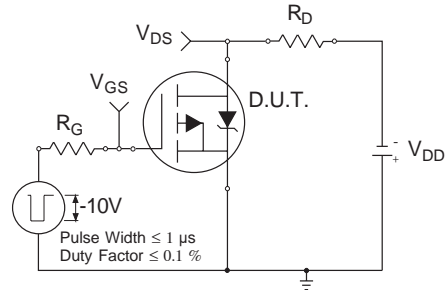


**Fig 8.** Maximum Safe Operating Area

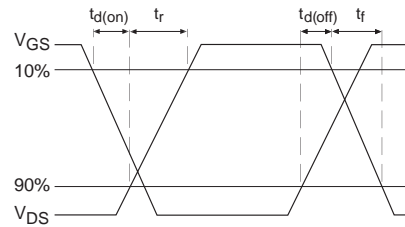
# IRFR/U5305PbF



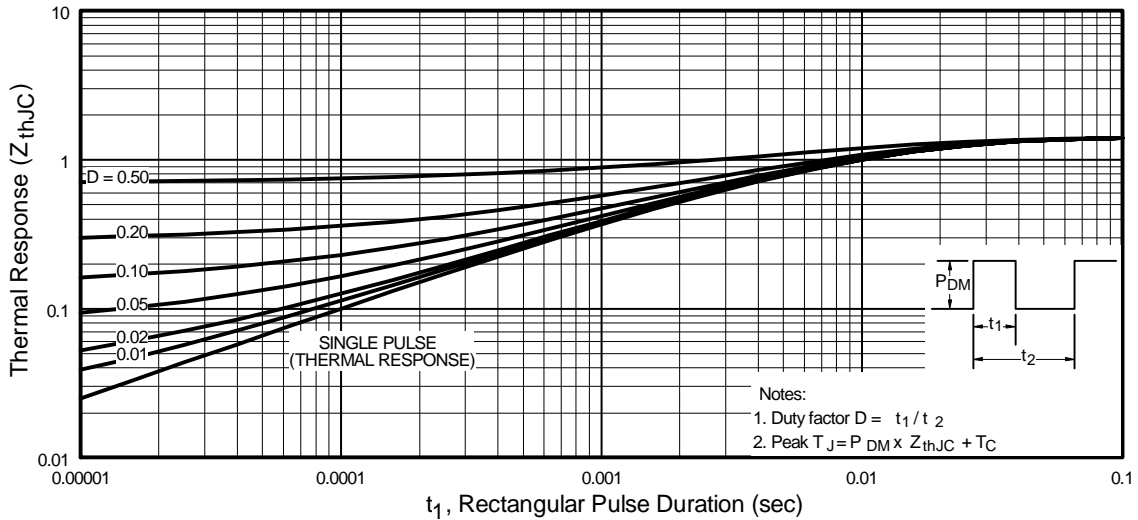
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

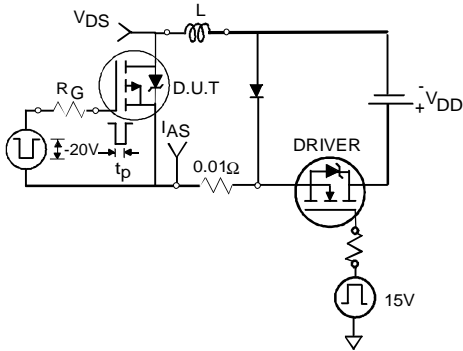


**Fig 10b.** Switching Time Waveforms

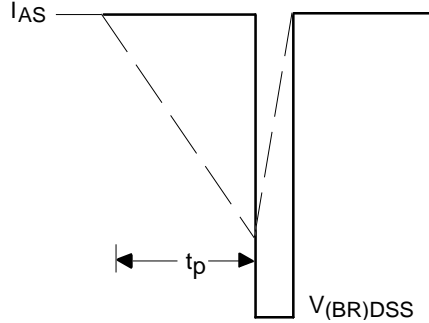


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

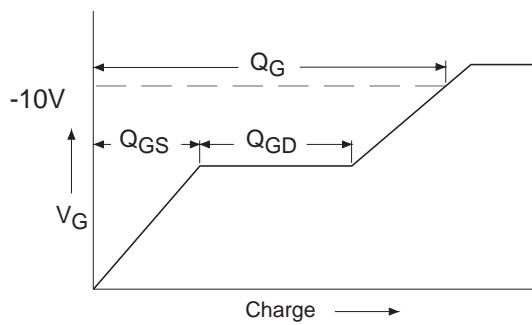
# IRFR/U5305PbF



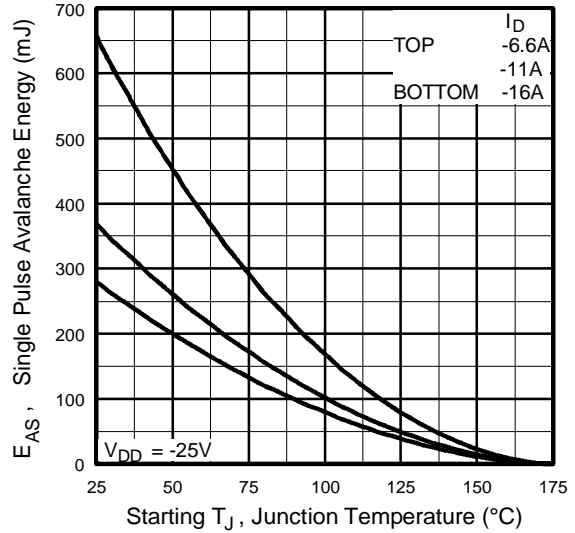
**Fig 12a.** Unclamped Inductive Test Circuit



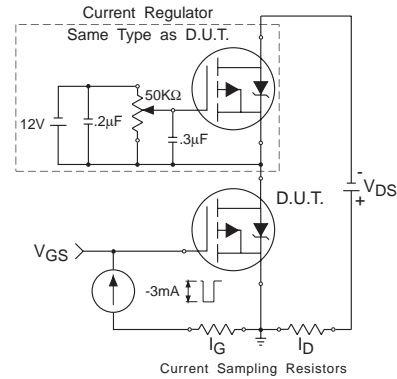
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

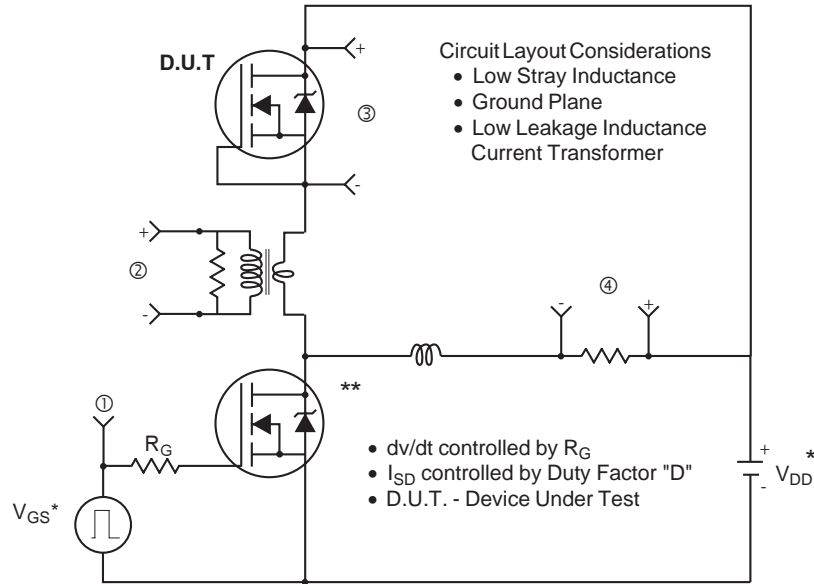


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



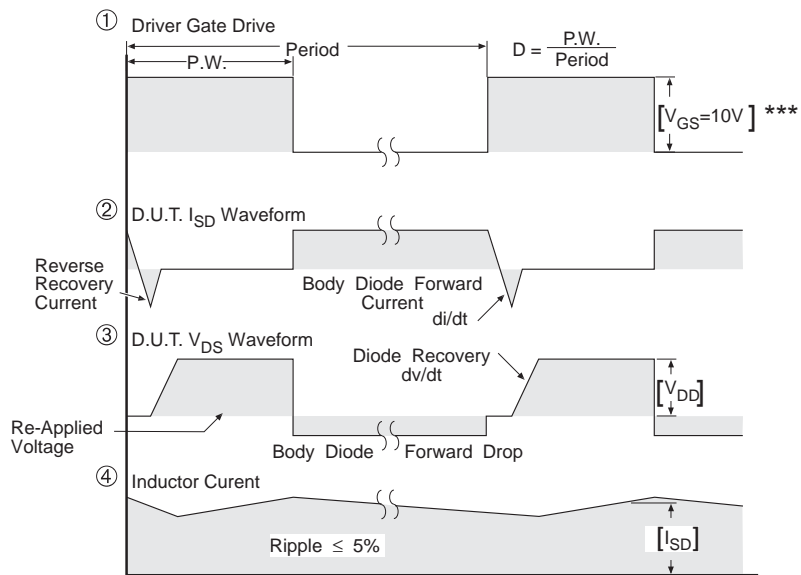
**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity for P-Channel

\*\* Use P-Channel Driver for P-Channel Measurements



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

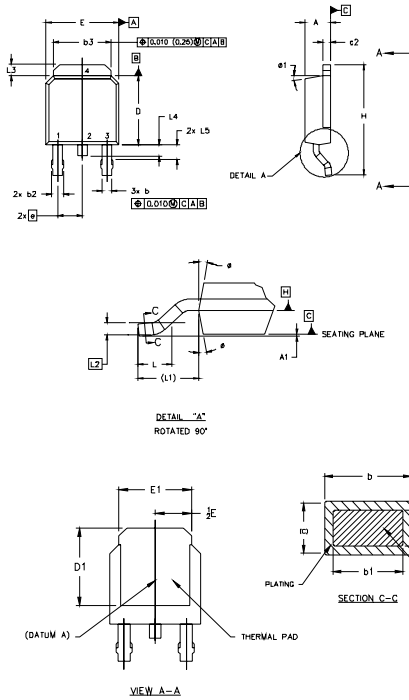
**Fig 14.** For P-Channel HEXFETS

# IRFR/U5305PbF



## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
- 3.0 LEAD DIMENSION UNCONTROLLED IN L5
- 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540] FROM THE LEAD TIP.
- 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

| SYMBOL | MILLIMETERS |       | INCHES    |       | NOTES |
|--------|-------------|-------|-----------|-------|-------|
|        | MIN.        | MAX.  | MIN.      | MAX.  |       |
| A      | 2.18        | 2.39  | .086      | .094  |       |
| A1     |             | 0.13  |           | .005  |       |
| b      | 0.64        | 0.89  | .025      | .035  | 5     |
| b1     | 0.64        | 0.79  | .025      | 0.031 | 5     |
| b2     | 0.76        | 1.14  | .030      | .045  |       |
| b3     | 4.95        | 5.46  | .195      | .215  |       |
| c      | 0.46        | 0.61  | .018      | .024  | 5     |
| c1     | 0.41        | 0.56  | .016      | .022  | 5     |
| c2     | .046        | 0.89  | .018      | .035  | 5     |
| D      | 5.97        | 6.22  | .235      | .245  | 6     |
| D1     | 5.21        | -     | .205      | -     | 4     |
| E      | 6.35        | 6.73  | .250      | .265  | 6     |
| E1     | 4.32        | -     | .170      | -     | 4     |
| e      | 2.29        | -     | .090 BSC  | -     |       |
| H      | 9.40        | 10.41 | .370      | .410  |       |
| L      | 1.40        | 1.78  | .055      | .070  |       |
| L1     | 2.74 REF.   | -     | .108 REF. | -     |       |
| L2     | 0.051 BSC   | -     | .020 BSC  | -     |       |
| L3     | 0.89        | 1.27  | .035      | .050  |       |
| L4     |             | 1.02  |           | .040  |       |
| L5     | 1.14        | 1.52  | .045      | .060  | 3     |
| a      | 0"          | 10"   | 0"        | 10"   |       |
| a1     | 0"          | 15"   | 0"        | 15"   |       |

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

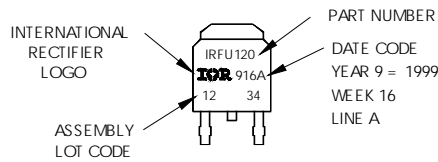
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

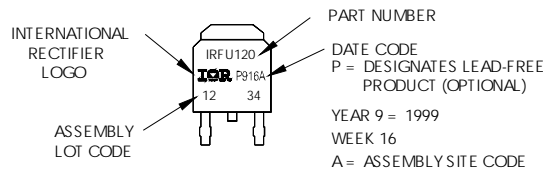
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 1999  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates "Lead-Free"



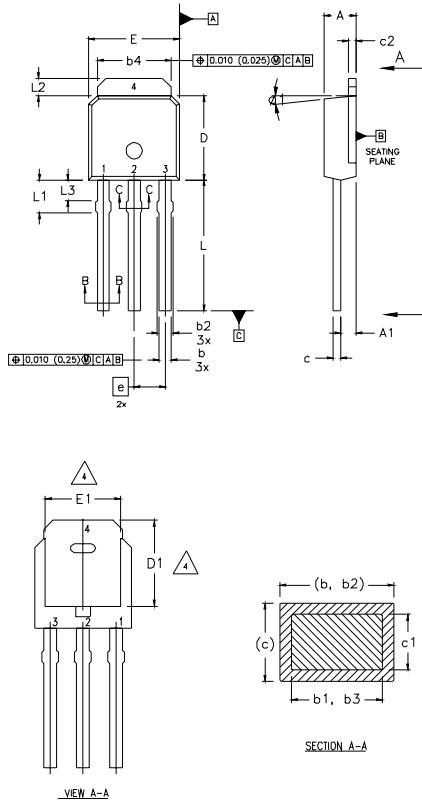
OR





## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

| SYMBOL | DIMENSIONS  |      |           |       | NOTES |
|--------|-------------|------|-----------|-------|-------|
|        | MILLIMETERS |      | INCHES    |       |       |
|        | MIN.        | MAX. | MIN.      | MAX.  |       |
| A      | 2.18        | 2.39 | 0.086     | .094  |       |
| A1     | 0.89        | 1.14 | 0.035     | 0.045 |       |
| b      | 0.64        | 0.89 | 0.025     | 0.035 |       |
| b1     | 0.64        | 0.79 | 0.025     | 0.031 | 4     |
| b2     | 0.76        | 1.14 | 0.030     | 0.045 |       |
| b3     | 0.76        | 1.04 | 0.030     | 0.041 |       |
| b4     | 5.00        | 5.46 | 0.195     | 0.215 | 4     |
| c      | 0.46        | 0.61 | 0.018     | 0.024 |       |
| c1     | 0.41        | 0.56 | 0.016     | 0.022 |       |
| c2     | .046        | 0.86 | 0.018     | 0.035 |       |
| D      | 5.97        | 6.22 | 0.235     | 0.245 | 3, 4  |
| D1     | 5.21        | -    | 0.205     | -     | 4     |
| E      | 6.35        | 6.73 | 0.250     | 0.265 | 3, 4  |
| E1     | 4.32        | -    | 0.170     | -     | 4     |
| e      | 2.29        |      | 0.090 BSC |       |       |
| L      | 8.89        | 9.60 | 0.350     | 0.380 |       |
| L1     | 1.91        | 2.29 | 0.075     | 0.090 |       |
| L2     | 0.89        | 1.27 | 0.035     | 0.050 | 4     |
| L3     | 1.14        | 1.52 | 0.045     | 0.060 | 5     |
| ø1     | Ø           | 15°  | Ø         | 15°   |       |

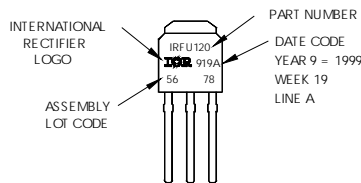
**LEAD ASSIGNMENTS**

**HEXFET**

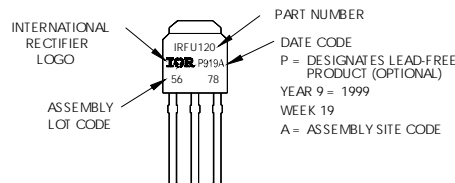
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 5678 ASSEMBLED ON WW 19, 1999 IN THE ASSEMBLY LINE "A"  
**Note:** "P" in assembly line position indicates "Lead-Free"



**OR**

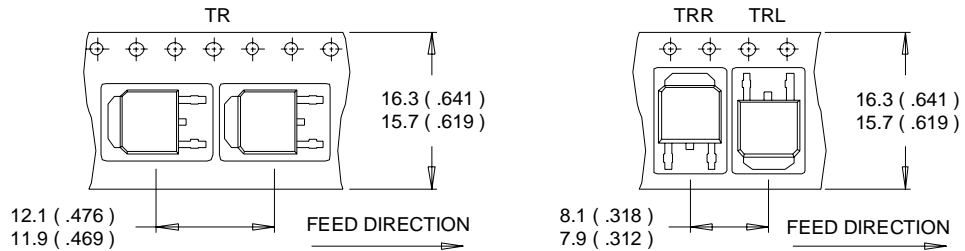


# IRFR/U5305PbF

International  
**IR** Rectifier

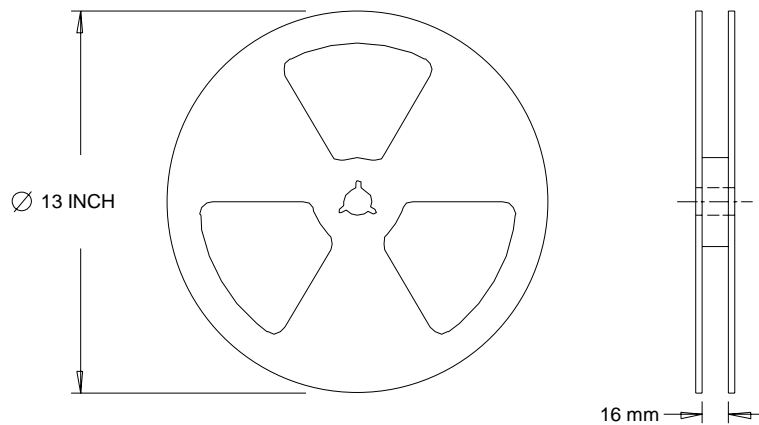
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

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[www.irf.com](http://www.irf.com)

Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>