FAIRCHILD SEMICONDUCTOR®

September 2005

FMS6410B
Dual Channel Video Drivers with Integrated Filters and Composite Video Summer

Features

- 7.1MHz 5th order Y,C filters with composite summer
- 50dB stopband attenuation at 27MHz on Y, C and CV outputs
- Better than 0.1dB flatness to 4.5MHz on Y,C and CV outputs
- No external frequency selection components or clocks
- < 5ns group delay on Y, C and CV outputs
- AC-Coupled Inputs
- AC or DC-Coupled Outputs
- Capable of PAL frequency selection components or clocks
- 0.3% differential gain with 0.2° differential phase on Y,C and CV channels
- Integrated DC restore circuitry with low tilt
- Lead (Pb) Free SOIC-8 Package

Applications

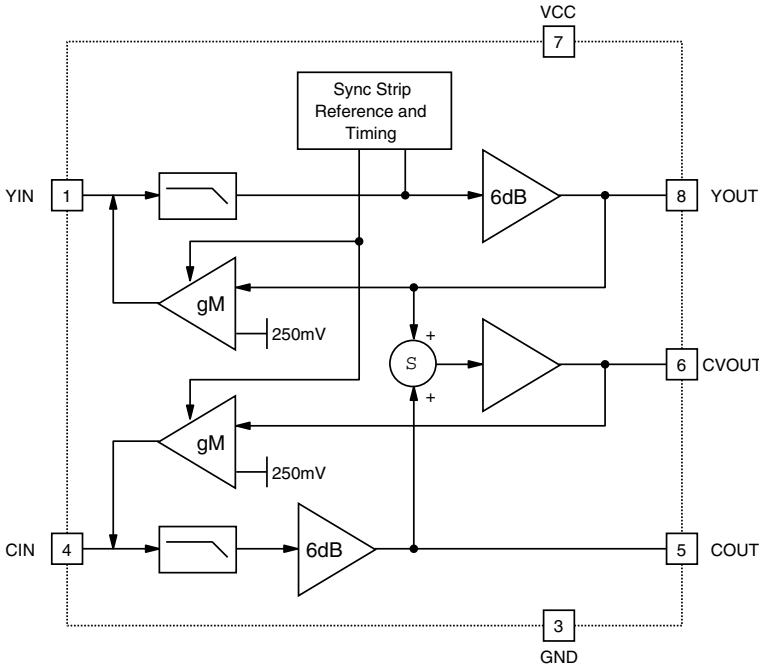
- Cable and Satellite set top boxes
- DVD players
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

Description

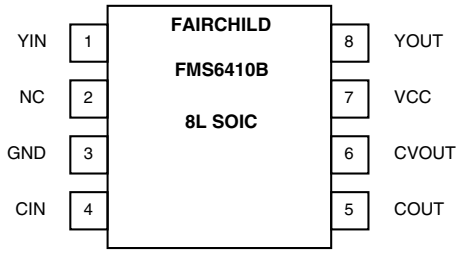
The FMS6410B is a dual Y/C 5th order Butterworth lowpass video filter optimized for minimum overshoot and flat group delay. The device also contains a summing circuit to generate filtered composite video. In a typical application, the Y and C input signals from DACs are AC coupled into the filters. Both channels have DC restore circuitry to clamp the DC input levels during video sync. The Y and C channels use separate feedback clamps. The clamp pulse is derived from the Y channel.

All outputs are capable of driving $2V_{pp}$, AC or DC coupled, into either a single or dual video load. A single video load consists of a series 75Ω impedance matching resistor connected to a terminated 75Ω line. This presents a total of 150Ω of loading to the part. A dual load would be two of these in parallel which would present a total of 75Ω to the part. The gain of the Y, C and CV signals is 6dB with $1V_{pp}$ input levels. All video channels are clamped during sync to establish the appropriate output voltage reference levels.

Block Diagrams



Pin Configuration



Pin Assignments

Pin#	Pin	Type	Description
1	Y_{IN}	Input	Luminance (Luma) Input: In a typical system, this pin is connected to the Luma or composite video output pin from the external video encoder.
2	NC	-	No Connect.
3	GND	Input	Must be tied to Ground
4	C_{IN}	Input	Chrominance (Chroma) Input: In a typical system, this pin is connected to the Chroma output pin from the external video encoder.
5	C_{OUT}	Output	Filtered Chrominance Video Output from the C_{IN} channel.
6	CV_{OUT}	Output	Composite Video Output: This pin is the sum of Y_{OUT} and C_{OUT} .
7	VCC	Input	+5V supply
8	Y_{OUT}	Output	Filtered Luminance Output from the Y_{IN} channel.

Typical Application Diagram

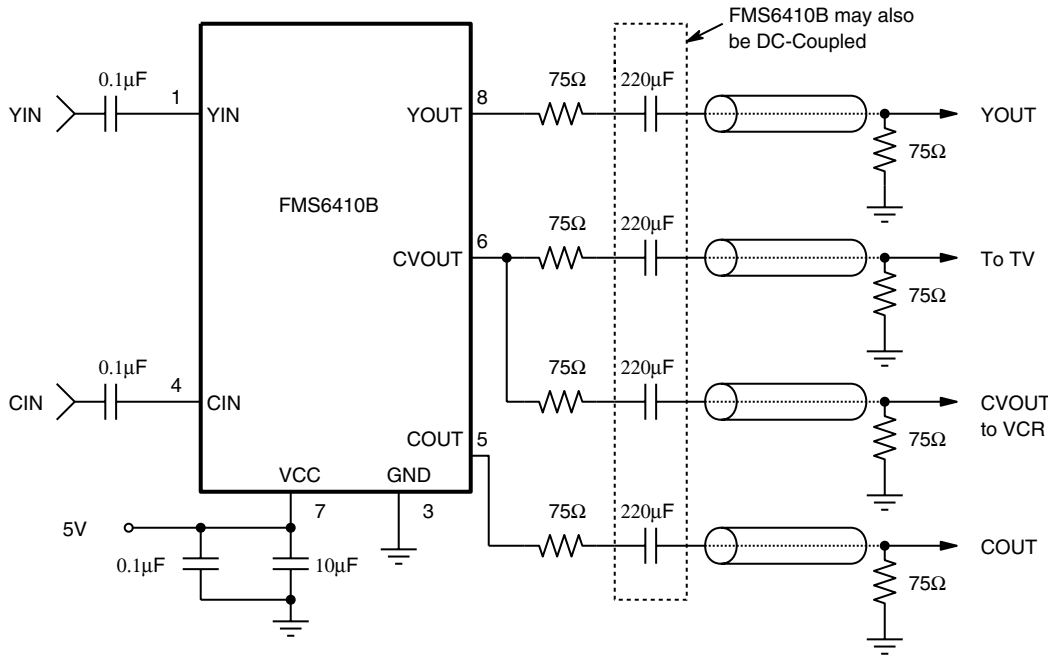


Figure 1. AC or DC-Coupled Application Diagram

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
DC Supply Voltage	-0.3	6	V
Analog and Digital I/O	-0.3	V_{cc} + 0.3	V
Output Current Any One Channel, Do Not Exceed		40	mA

Note:
Functional operation under any of these conditions in NOT implied. Performance and reliability are guaranteed only if operating conditions are not exceeded.

Reliability Information

Parameter	Min.	Typ.	Max.	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			300	°C
Thermal Resistance ($Theta_{JA}$), JEDEC Standard Multi-Layer Test Boards, Still Air		115		°C/W

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range	0		70	°C
Supply Voltage Range	4.75	5.0	5.25	V

DC Electrical Characteristics

T_c = 25°C, V_{cc} = 5V, V_{in} = 1V_{pp}, all inputs AC coupled with 0.1uF, all outputs AC coupled with 220uF into 150Ω loads, referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
I_{CC}	Supply Current[1]	No load		50	60	mA
V_i	Input Voltage Max			1.4		V_{pp}
PSRR	Power Supply Rejection Ratio	All channels, DC		60		dB

AC Electrical Characteristics

T_c = 25°C, V_{cc} = 5V, V_{in} = 1V_{pp}, all inputs AC coupled with 0.1uF, all outputs AC coupled with 220uF into 150Ω loads, referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
AV	Channel Gain[1]	All Channels	5.75	6.0	6.25	dB
C_{sync}	C_{OUT} Output Level (during sync)[1]	Sync present on Y_{IN} (after 6dB gain)		1.0	1.3	V
Y_{sync}	Y_{OUT} Output Level (during sync)[1]	Sync present on Y_{IN} (after 6dB gain)		0.35	0.5	V
CV_{sync}	CV_{OUT} Output Level (during sync)[1]	Sync present on Y_{IN} (after 6dB gain)		0.35	0.5	V
T_{CLAMP}	Clamp Response Time (Y channel)	Settled to within 10mV		10		ms
f_{FLAT}	Gain Flatness to 4.5MHz	All Channels		0		dB
f_C	-3dB Bandwidth[1]	All Channels	6.7	7.1		MHz
f_{SB}	Stopband Attenuation[1]	All Channels at 27MHz	42	50		dB
dG	Differential Gain	All Channels		0.3		%
dP	Differential Phase	All Channels		0.2		deg
THD	Output Distortion	V_{OUT} = 1.4V_{pp}, 3.58MHz		0.3		%
X_{TALK}	Crosstalk	at 3.58MHz		-50		dB
SNR	Signal-to-Noise Ratio All Channels	NTC-7 weighting, 4.2MHz LP, 100kHz HP		82		dB
t_{pd}	Propagation Delay	All Channels		115		ns
GD	Group Delay Deviation	All Channels at 3.58MHz		4		ns
t_{SKEW}	Skew Between Y_{OUT} and C_{OUT}	at 1MHz		0		ns
t_{CLGCV}	Chroma-Luma Gain CV_{OUT}[1]	f = 3.58MHz (ref to Y_{IN} at 400kHz)	96	100	104	%
t_{CLDCV}	Chroma-Luma Delay CV_{OUT}	f = 3.58MHz (ref to Y_{IN} at 400kHz)		4		ns

Notes:

1. 100% tested at 25°C

Applications Information

Functional Description

This product is a two channel monolithic continuous time video filter designed for reconstructing the luminance and chrominance signals from an S-Video D/A source. Composite video output is generated by summing the Y and C outputs. The chip is designed to have AC coupled inputs and will work equally well with either AC or DC coupled outputs.

The reconstruction filters provide a 5th order Butterworth response with group delay equalization. This provides a maximally flat response in terms of delay and amplitude. Each of the three outputs is capable of driving $2V_{pp}$ into a 75Ω load.

All channels are clamped during the sync interval to set the appropriate minimum output dc level. With this operation the effective input time constant is greatly reduced, which allows for the use of small low cost coupling capacitors. The net effect is that the input will settle to 10mV in 10ms for any DC shifts present in the input video signal.

In most applications the input coupling capacitors are 0.1µF. The Y and C inputs typically sink 1µA of current during active video, which normally tilts a horizontal line by 2mV at the Y output. During sync, the clamp restores this leakage current by sourcing an average of 20µA over the clamp interval. Any change in the coupling capacitor values will affect the amount of tilt per line. Any reduction in tilt will come with an increase in settling time.

Luminance (Y) I/O

The typical luma input is driven by either a low impedance source of $1V_{pp}$ or the output of a 75Ω terminated line driven by the output of a current DAC. In either case, the input must be capacitively coupled to allow the sync-detect and DC restore circuitry to operate properly.

All outputs are capable of driving 2Vpp, AC or DC coupled, into either a single or dual video load. A single video load consists of a series 75Ω impedance matching resistor connected to a terminated 75Ω line, this presents a total of 150Ω of loading to the part. A dual load would be two of these in parallel which would present a total of 75Ω to the part. The gain of the Y, C and CV signals is 6dB with $1V_{pp}$ input levels.

Chrominance (C) I/O

The chrominance input can be driven in the same manner as the luminance input but is typically only a $0.7V_{pp}$ signal.

Since the chrominance signal doesn't contain any DC content, the output signal can be AC coupled using as small as a 0.1µF capacitor if DC coupling is not desired.

Composite Video (CV) Output

The composite video output driver is same as the other outputs.

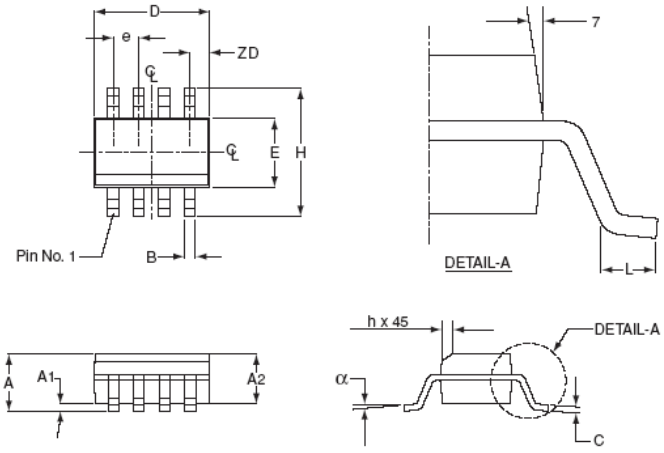
Layout Considerations

General layout and supply bypassing play major roles in high frequency performance and thermal characteristics. Fairchild offers a demonstration board, FMS6410BDEMO, to use as a guide for layout and to aid in device testing and characterization. The FMS6410BDEMO is a 4-layer board with a full power and ground plane. For optimum results, follow the steps below as a basis for high frequency layout:

- Include 10µF and 0.1µF ceramic bypass capacitors
- Place the 10µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- If using DC-coupled outputs, use a large ground plane to help dissipate heat
- Minimize all trace lengths to reduce series inductances

Mechanical Dimensions

SOIC-8



SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
	0°	8°
ZD	0.53 ref	
A2	1.37	1.57

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.10mm (.004") max.
3. Package surface finishing:
   (2.1) Top: matte (charmilles #18~30).
   (2.2) All sides: matte (charmilles #18~30).
   (2.3) Bottom: smooth or matte (charmilles #18~30).
4. All dimensions excluding mold flashes and end flash from the package body shall not exceed 0.152mm (.006) per side (D).

Ordering Information

Model	Part Number	Lead Free	Package	Container	Pack Qty
FMS6410B	FMS6410BCS	Yes	SOIC-8	Rail	95
FMS6410B	FMS6410BCSX	Yes	SOIC-8	Reel	2500

Temperature range for all parts: 0°C to 70°C.

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Bottomless™	FASTr™	MICROCOUPLER™	PowerTrench®	SuperSOT™-6
CoolFET™	FPS™	MicroFET™	QFET®	SuperSOT™-8
CROSSVOLT™	FRFET™	MicroPak™	QS™	SyncFET™
DOME™	GlobalOptoisolator™	MICROWIRE™	QT Optoelectronics™	TinyLogic®
EcoSPARK™	GTO™	MSX™	Quiet Series™	TINYOPTO™
E²CMOS™	HiSeC™	MSXPro™	RapidConfigure™	TruTranslation™
EnSigna™	I²C™	OCX™	RapidConnect™	UHC™
FACT™	ImpliedDisconnect™	OCXPro™	SILENT SWITCHER®	UltraFET®
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The Power Franchise™		OPTOPLANAR™	SPM™	
Programmable Active Droop™		PACMAN™	Stealth™	

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PRODUCT STATUS DEFINITIONS

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Rev. I7