ROHM

Structure : Silicon Monolithic Integrated Circuit
Product Name : Power Driver IC for CD changers

Device Name : **BD7962FM**

Features :
- 6-ch driver IC comprising of 3 channels for BTL drivers and 3 channels for loading drivers
- 2 channels of loading drivers providing MOS outputs with a high D-range (Ron=1.0Ω)
- Provided with a loading driver voltage setting terminal
- In BTL driver 3 channels, individually installed is a pre-stage OP-AMP which allows a differential input and an addition input.
- A built-in general operational amplifier 1 channel installed
- MUTE SW provided
- A built-in thermal shutdown circuit installed.
- HSOP-M36 package

O ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power Supply Voltage	Vcc	15	V
Power Dissipation	Pd	2.2 *1	W
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C

*1 When mounted on the glass/epoxy board with the size: 70 mm×70 mm, the thickness: 1.6 mm, and the rate of copper foil occupancy area: 3% or less.
Over Ta=25°C, derating at the rate of 17.6mW/°C.

O RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN	TYP	MAX	Unit
Power Supply Voltage 1 (CH1, CH2)	Vcc1	4.5	5.0	Vcc3	V
Power Supply Voltage2 (CH3, CH4)	Vcc2	4.5	8.0	14.0	V
Power Supply Voltage 3 (CH5, CH6)	Vcc3	4.5	8.0	14.0	V

This product has not been checked for the strategic materials (or service) defined in the Foreign Exchange and Foreign Trade Control Low of Japan so that a verification work is required before exporting it.
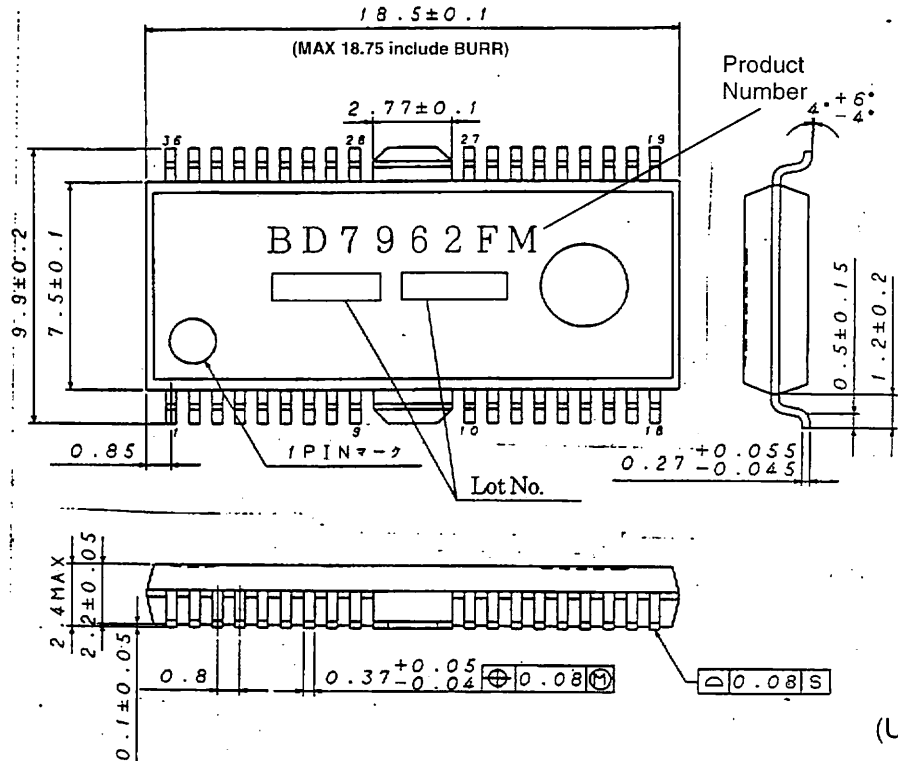Not designed for radiation resistance.
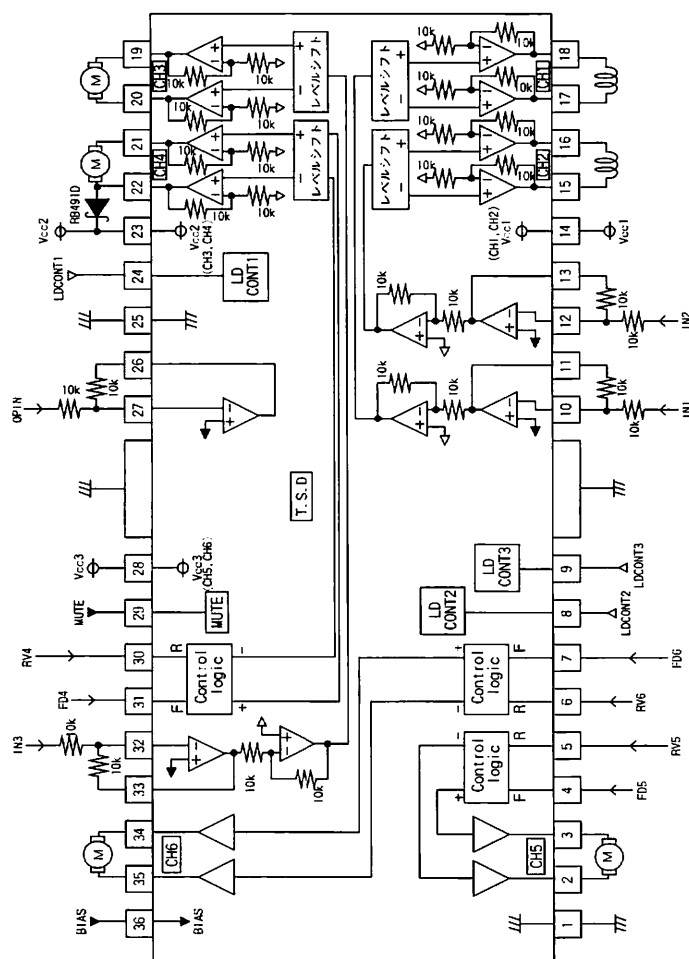
O ELECTRIC CHARACTERISTICS
(Ta=25°C, Vcc1=5V, Vcc2=Vcc3=8V, BIAS=1.65V, RL=8Ω, unless otherwise noted.)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Quiescent Circuit Current (Voc1)	ICC1	-	0.30	0.70	mA	No load applied
Quiescent Circuit Current (Voc2)	ICC2	11.5	23.0	32.0		No load applied
Quiescent Circuit Current (Voc3)	ICC3	1.9	3.8	5.7		No load applied
<BTL Driver CH1 - CH3>						
Output Offset Voltage	VOFS	-40	0	+70	mV	
Maximum Output Amplitude (CH1, CH2)	VOM1	3.7	4.0	-	V	
Maximum Output Amplitude (CH3)	VOM2	5.4	6.0	-	V	
Closed Circuit Voltage Gain (CH1 - CH3)	GVC	10	12	14	dB	VIN=BIAS±0.5V, when pre-stage OP buffered
Difference between positive and negative voltage gains (CH1 - CH3)	ΔGVC	-20	0	20	dB	
Mute ON Voltage	VMON	GND	-	0.5	V	
Mute Reset Voltage	VMOFF	2.0	-	Vcc	V	
Mute Terminal Input Current	IMUTE	-	80	125	μA	VMUTE=5VVBIAS=2.5V
Bias Terminal Inflow Current	IBIAS	-	75	120	μA	VBIAS=2.5V
<Loading Driver CH4 - CH6>						
Output Offset Voltage	VOFSL	-35	0	+35	mV	In brake mode
Input Terminal Threshold Voltage H	VH	2.0	-	Vcc	V	
Input Terminal Threshold Voltage L	VL	GND	-	0.5	V	
Maximum Output Amplitude (CH4)	VOML	5.4	6.0	-	V	RL=8Ω
Output Saturation Voltage H (CH5, CH6)	VOLH	-	0.38	0.70	V	Lo=500mA
Output Saturation Voltage L (CH5, CH6)	VOLL	-	0.12	0.25	V	Lo=500mA
Voltage Gain (Loading)	GVLD	4.0	6.0	8.0	dB	LDCONT=5V
Difference between positive and negative voltage gains (Loading)	ΔGVLD	-2.0	0	2.0	dB	
Input Terminal Inflow Current	INL	-	180	270	μA	LDIN=5V
LDCONT Terminal Outflow Current (LDCONT 1)	ILDC1	-	-	0.5	mA	LDCONT=5V
LDCONT Terminal Outflow Current (LDCONT 2,3)	ILDC2	-	-	300	nA	LDCONT=5V
<Pre-stage OP-amp / OP-amp>						
Input Offset Voltage	VOPOFS	-5	0	+5	mV	
Input Bias Current	IOPB	-	-	300	nA	
Common Mode Input Voltage Range	VOPICM	0.3	-	VCC-1.2	V	
Maximum Output Source Current	Isource	500	800	-	μA	
Maximum Output Sink Current	ISNK	2	-	-	mA	
Slew Rate	SR	-	2	-	V/μs	

O OUTLINE DIMENSIONS

(UNIT: mm)

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O APPLICATION CIRCUIT DIAGRAM

T.S.D: (Thermal shutdown)
Resistance unit : [Ω]

O PIN Description

No.	Pin name	Description	No.	Pin name	Description
1	GND2	GND (Loading driver unit)	19	OUT3+	BTL driver (CH3) output +
2	OUT5-	Loading driver (CH5) output -	20	OUT3-	BTL driver (CH3) output -
3	OUT5+	Loading driver (CH5) output +	21	OUT4+	Loading driver (CH4) output +
4	IN5FWD	Loading driver (CH5) FWD input	22	OUT4-	Loading driver (CH4) output -
5	IN5REV	Loading driver (CH5) REV input	23	Vcc2	Power Supply Voltage (CH3, CH4)
6	IN6REV	Loading driver (CH6) REV input	24	LDCONT 1	Loading driver (CH4) voltage setting terminal
7	IN6FWD	Loading driver (CH6) FWD input	25	GND1	GND (BTL driver part)
8	LDCONT 2	Loading driver (CH5) voltage setting terminal	26	OPOUT	OP-amp output
9	LDCONT 3	Loading driver (CH6) voltage setting terminal	27	OPIN-	OP-amp negative input
10	OPIN1-	CH1 pre-stage OP-amp negative input	28	Vcc3	Power Supply Voltage (CH5, CH6 parts)
11	OP1OUT	CH1 pre-stage OP-amp output	29	MUTE	BTL driver MUTE terminal
12	OPIN2-	CH2 pre-stage OP-amp negative input	30	IN4REV	loading driver (CH4) REV input
13	OP2OUT	CH2 pre-stage OP-amp output	31	IN4FWD	loading driver (CH4) FWD input
14	Vcc1	Power Supply Voltage (CH1, CH2)	32	OPIN3-	CH3 pre-stage OP-amp negative input
15	OUT2-	BTL driver (CH2) output -	33	OP3OUT	CH3 pre-stage OP-amp output
16	OUT2+	BTL driver (CH2) output +	34	OUT6+	Loading driver (CH6) output +
17	OUT1-	BTL driver (CH1) output -	35	OUT6-	loading driver (CH6) output -
18	OUT1+	BTL driver (CH1) output +	36	BIAS	BIAS terminal

* The positive or negative polarity of the BTL driver output corresponds to the output polarity of the pre-stage OP-amp.
When the pre-stage OP-amp output is H, the positive output will be H while the negative one L.

O CAUTIONS ON USE

(1) When the mute terminal (Pin 29) is set to open or its voltage drops to 0.5V (typ.) or less, the output current of the BTL driver part (CH1 to CH3) can be muted.
Under conditions of normal use, it should be pulled up to 2.0V or above.

(2) On the Bias terminal (Pin 36), the applied voltage of 0.7V (Typ.) or less will activate the mute function on the BTL driver part (CH1-CH3).
Under conditions of normal use, it should be kept 1.1V or above.

(3) Thermal shutdown (TSD) will activate the mute function on all drivers, while mute ON or bias terminal voltage drop will on the BTL drivers except loading drivers.
The pre-stage OP-amps cannot be muted in any cases described above.
While muting, the output terminals of CH1 and CH2 show the internal bias voltage: Vcc1/2V and the output terminal of CH3 show the internal bias voltage: (Vcc2-0.7)/2V.

(4) The loading driver functions following to the logic in the table below:

INPUT		OUTPUT		
FWD	REV	OUT+	OUT-	Function
L	L	Hi-Z	Hi-Z	High Impedance
L	H	L	H	Reverse mode
H	L	H	L	Forward mode
H	H	L	L	Brake mode

Although the output voltage can be changed by the input voltage through the LDCONT terminal (gain 6dB Typ.), it never exceeds the maximum output voltage restricted by the power supply voltage even if applying a voltage much larger than the normal value.
If the LDCONT terminals (Pin 8, Pin 9, Pin 24) are set to 0.7V or less, the outputs of the loading driver corresponding to the LDCONT terminal will be in the High-impedance mode.
CH4 with the impedance of 40kΩ, however, shows the internal bias voltage: (VCC2-0.7)/2V.

(5) On Vcc2 (Pin 23) must be applied the same voltage as that of Vcc3 (Pin 28) and Vcc1 (Pin 14) or above.

(6) The radiating FIN must be connected to the external GND.

(7) A Shot key diode must be inserted between OUT4- (Pin 22) and Vcc2 (Pin 23) (see the APPLICATION CIRCUIT DIAGRAM) to prevent the current induced by a counter electromotive force of the motor from flowing into the IC.

(8) Short-circuits between output pin-VCC, output pin-GND, or output terminals (load short) must be avoided.   It may damage ICs or produce smoke.

(9) About absolute maximum ratings
Exceeding the absolute maximum ratings, such as the applied voltage or the operating temperature range, may cause permanent device damage.   As these cases cannot be limited to the broken short mode or the open mode, if a special mode where the absolute maximum ratings may be exceeded is assumed, it is recommended to take mechanical safety measures such as attaching fuses.

(10) About power supply lines
As a measure against the back current regenerated by a counter electromotive force of the motor, a capacitor to be used as a regenerated-current path can be installed between the power supply and GND and its capacitance value should be determined after careful check that any problems, for example, a leak capacitance of the electrolytic capacitor at low temperature, are not found in various characteristics.

(11) About GND potential
The electric potential of the GND terminal must be kept lowest in the circuitry at any operation states.

(12) About thermal design
With consideration of the power dissipation (Pd) under conditions of actual use, a thermal design provided with an enough margin should be done.

(13) About operations in a strong electric field
When used in a strong electric field, note that a malfunction may occur.

(14) ASO
When using this IC, the output Tr. must be set not to exceed the values specified in the absolute

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maximum ratings and ASO.

(15) Thermal shutdown circuit

This IC incorporates a thermal shutdown circuit (TSD circuit).   When the chip temperature reaches the value shown below, the coil output to the motor will be set to open.

The thermal shutdown circuit is designed only to shut off the IC from a thermal runaway and not intended to protect or guarantee the entire IC functions.

Therefore, users cannot assume that the TSD circuit once activated can be used continuously in the subsequent operations.

TSD ON Temperature [°C] (typ.)	Hysteresis Temperature [°C] (typ.)
175	25

(16) About earth wiring patterns

When a small signal GND and a large current GND are provided, it is recommended that the large current GND pattern and the small signal GND pattern should be separated and grounded at a single point of the reference point of the set in order to prevent the voltage of the small signal GND from being affected by a voltage change caused by the resistance of the pattern wiring and the large current. Make sure that the GND wiring patterns of the external components will not change, too.

(17) This IC is a monolithic IC which has a P^+ isolations and P substrate to isolate elements each other.

This P layer and an N layer in each element form a PN junction to construct various parasitic elements. Due to the IC structure, the parasitic elements are inevitably created by the potential relationship. Activation of the parasitic elements can cause interference between circuits and may result in a malfunction or, consequently, a fatal damage.   Therefore, make sure that the IC must not be used under conditions that may activate the parasitic elements, for example, applying the lower voltage than the ground level (GND, P substrate) to the input terminals.

In addition, do not applying the voltage to input terminals without applying the power supply voltage to the IC.   Also while applying the power supply voltage, the voltage of each input terminal must not be over the power supply voltage, or within the guaranteed values in the electric characteristics.

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