THREE-DIMENSIONAL Y/C SEPARATION IC WITH ON-CHIP MEMORY

μPD64083

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The μPD64083 is a single-chip NTSC 3-D Y/C separation IC that achieves superior TV picture quality by incorporating the conventionally external 4 Mb frame memory on the chip.

Photo 1 NEC's 3-D Y/C Separation LSI with On-Chip Memory "μPD64083"

Introduction

The recent advent of flat-screen, LCD, and PDP panel televisions has brought significant increases in demand for larger screens with higher resolution, and a higher screen quality to match. A better picture quality than that provided by the conventional terrestrial TV broadcasts (NTSC signals) both in Japan and in North America is being especially looked for due to the arrival of high-picture-quality digital media, such as the increasingly popular DVD video and Japan's BS Digital satellite TV service, which started last year. Not limited to television, demands for high-quality terrestrial NTSC signals are also being felt in related fields, such as high-picture-quality digital image recording devices (DVD recorders, hard disk recorders) and PCs that include TV functions.

The key to improving the picture quality of NTSC signals is a high-precision Y/C separation function. Most televisions employ two-dimensional Y/C separation performed using inter-line processing, but this kind of separation invariably results in "cross color" (color noise such as fine diagonal lines occurring in the pattern) and "hanging dots" (network noise that occurs on the edge of the color).

In order to solve these problems, NEC has been developing and commercializing a range of motion-adaptive 3-D Y/C separation ICs that can be used to minimize cross color and hanging dot noise.

Development Background

Almost all wide TVs and most 29-inch or over 4:3 TVs in the Japanese television market incorporate a 3-D Y/C separation function, as do most 30-inch or over and 50-inch class projection TVs in the North American market. Realizing that 3-D Y/C separation ICs are the key device in these large-size televisions, NEC
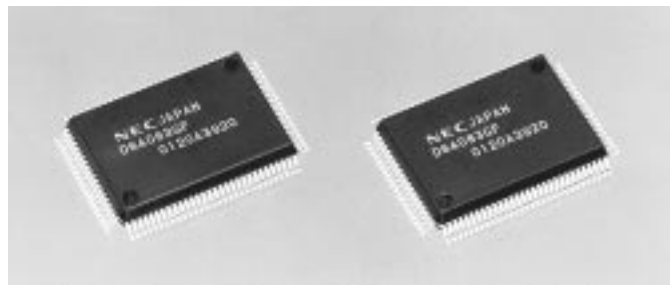
has focussed considerable development resources in this area and has gained a reputation from both television makers and end users for providing products that are superior in terms of functionality, performance and price: an effort that has been rewarded with the achievement of a 70% or more share in this market.

However, 3-D Y/C separation systems have tended to be complex and expensive, due in part to the necessity of providing memory to save picture data on a frame-by-frame basis. Moreover, the EDO DRAM that was conventionally attached externally for this purpose was a major source of noise, which then had to be countered by even more complex board design, resulting in even higher cost.

Against this background, NEC has now developed the μPD64083, a new single-chip 3-D Y/C separation IC that realizes high-precision separation by incorporating on the chip the 4 Mb memory that was conventionally attached externally (Photo 1). With this new IC, users can now create a high-picture-quality, noise-free 3-D Y/C separation system with little effort.

The development roadmap of NEC's 3-D Y/C separation ICs is shown in Figure 1.

Product Outline

This IC integrates on one chip all the functions required for Y/C separation of terrestrial broadcasts (NTSC signals) for high-picture-quality TV, including a 2-channel 10-bit A/D

converter, clock generator, 2-channel 10-bit D/A converter, I²C bus register, motion-adaptive 3-D Y/C separation, motion detection, nonstandard detection, and frame recursive noise reduction.

Figure 2 shows a block diagram of the μPD64083.

Either a composite signal or separate signals (S pin input) can be input as the input signal. If the former is input, the 3-D Y/C separation function can be used, and if the latter, the noise reduction function can be used. Furthermore, for a composite or luminance signal, not only is the 10-bit A/D converter used, but the signals are also processed internally in 10 bits, giving this IC the industry's highest grayscale reproduction performance as a consumer TV signal processor. The incorporation of a number of additional functions, including vertical border correction, horizontal peaking, coring, ID-1 signal detection, and noise detection, also makes this IC unrivaled in terms of versatility.

Features

1. Single-chip system

Whereas previous 3-D Y/C separation systems were made up of a number of different chips (memory, etc.), the μPD64083 integrates all these functions on a single chip. Now, all that needs to be provided externally are several discrete circuits such as a picture I/O circuit, 20 MHz crystal for clock generation,

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synchronization separator, and BPF circuit, all of which can be achieved using a few transistors.

This not only facilitates board design, but also significantly reduces the required mounting space.

2. On-chip memory

Four-megabit EDO DRAM is the frame memory used in conventional Y/C separation ICs (µPD64082, etc.) to store frame delay data, which is required in order to perform 3-D Y/C separation. However, the memory interface that connected this memory tended to be the source of extremely disruptive noise that had a very negative effect on the picture signals, leading to degraded picture quality. With the µPD64083, however, this noise source has been eliminated by incorporating the memory on the chip, leaving no picture quality degradation caused by memory access noise.

3. Low power consumption

By incorporating the memory on the µPD64083 IC chip using the latest fabrication technology to create a single-chip product, the power consumption of the chip during operation has been lowered to about half the level of the conventional IC. Moreover, the addition of a sleep mode that can be activated by a command sent over the I²C bus in cases when the set is operating but this IC is not has enabled a further 50% (or more) reduction in the power consumption.

4. Many added functions

The µPD64083 contains a function for performing noise reduction on Y/C separated signals, in addition to the 3-D Y/C separation function itself. This 3-D noise reduction function utilizes the frame memory and allows the efficient reduction of just the noise, without affecting the resolution of the picture.

A range of detection functions such as noise detection, wide clear vision ID detection, and ID-1 detection are also included, the results of which can be read out from the I²C bus.

Other functional additions include vertical border correction and horizontal peaking functions implemented for luminance signals to accentuate the edges of the picture, and a coring function to enable simple and effective noise reduction, thus providing broad picture quality control.
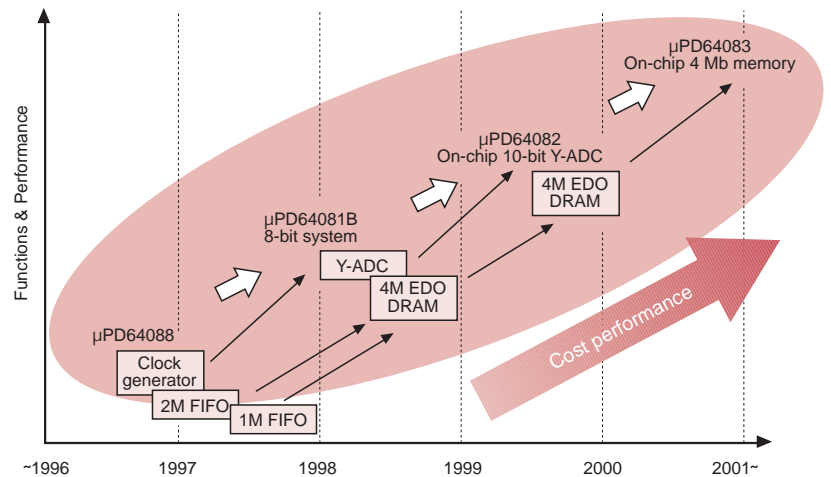

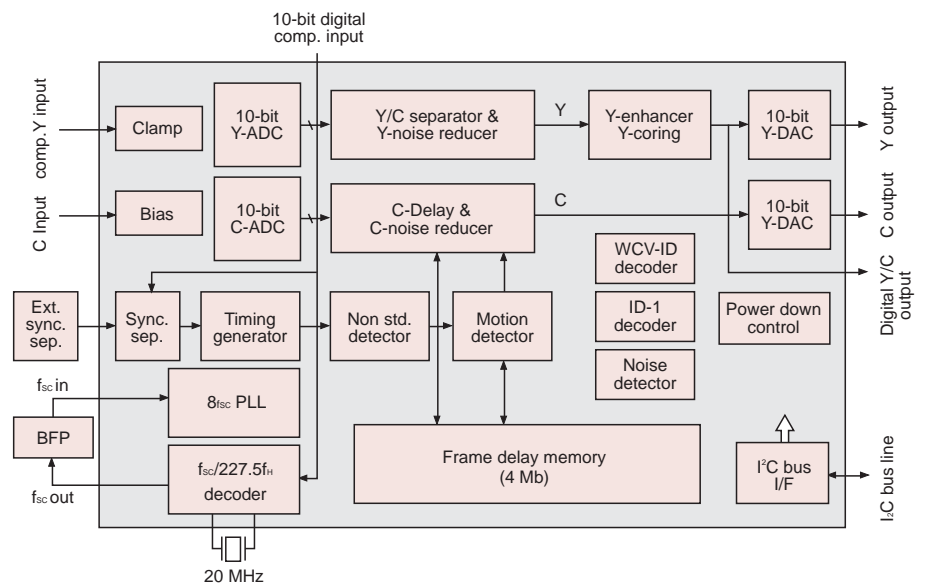**Fig. 1 Development Roadmap of NEC's 3-D Y/C Separation ICs**

Fig. 2 µPD64083 Block Diagram

Table 1 Basic Specifications of μPD64083

On-chip A/D resolution	For composite/luminance signals: 10 bits For chroma signals: 10 bits
On-chip D/A resolution	10 bits ($\times$ 2 channels)
Supported signal standard	NTSC
Picture input	Composite or Y/C separated signals
Picture output	Analog Y/C signals
Frame memory	4 Mb (on-chip)
Major functions	Motion-adaptive 3-D Y/C separation Logical comb filter type 2-D Y/C separation Frame recursive type Y/C noise reduction Frame comb type Y noise reduction Clock generator, ID-1 detection Power-down mode, various control functions via I²C bus
System clock	28.6 MHz (14.3 MHz for signal processing: either clock generated internally)
Power supply voltage	For analog/digital memory: 2.5 V, for peripheral circuits: 3.3 V
Package	100-pin plastic QFP (14 mm $\times$ 20 mm)

Conclusion

In spite of advances being made in the digitization of picture media, NTSC and other conventional analog picture signals are likely to be required for some time to come. In fact these signals are starting to perform a new role as the front-end block of digital video signals. NEC therefore plans to continue developing a range of analog video signal processor ICs based on its advanced 3-D Y/C separation technology to meet the varied needs of the AV equipment market.