3.3V, PRECISION, 33MHz to 500MHz PROGRAMMABLE LVPECL AND HSTL BUS CLOCK SYNTHESIZER

Precision Edge™
SY89536L

FEATURES

- **Integrated synthesizer plus fanout buffers, clock dividers, and translator in a single 64-pin package**
- **Accepts any reference input between 14MHz to 160MHz (single-ended or differential)**
- **33MHz to 500MHz output frequency range**
- **LVPECL and HSTL outputs**
- **3.3V ±10% power supply**
- **Low jitter: <50ps cycle-to-cycle**
- **Low pin-to-pin skew: <50ps**
- **TTL/CMOS compatible control logic**
- **3 independently programmable output frequency banks:**
  - **9 differential output pairs @BankB (HSTL)**
  - **2 differential output pairs @BankA (LVPECL)**
  - **2 differential output pairs @BankC (LVPECL)**
- **Available in 64-pin EPAD-TQFP**

Precision Edge™

DESCRIPTION

The SY89536L programmable clock synthesizer is part of a 3.3V, high-frequency, precision PLL-based clock synthesizer family optimized for multi-frequency, large clock-tree applications. This device integrates the following blocks into a single monolithic IC:

- PLL (Phase-Lock-Loop)-based synthesizer
- Fanout buffer
- Clock generator (divider)
- Logic translation (LVPECL, HSTL)

The SY89536L includes a flexible input design that accepts any reference input; single-ended LVTTL/CMOS, SSTL and differential LVPECL, LVDS, HSTL, and CML.

This level of integration minimizes the additive jitter and part-to-part skew associated with the discrete alternative, resulting in superior system-level timing as well as reduced board space and power. For applications that must interface to a crystal oscillator, see the SY89531L.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

APPLICATIONS

- **Servers**
- **Workstations**
- **Parallel processor-based systems**
- **Other high-performance computing**
- **Communications**

PRODUCT SELECTION GUIDE

	Input		Output		
Device	Crystal	Reference	BankA	BankB	BankC
SY89531L*	X		LVPECL	HSTL	LVPECL
SY89532L*	X		LVPECL	LVPECL	LVPECL
SY89533L*	X		LVPECL	LVDS	LVPECL
SY89534L*		X	LVPECL	LVPECL	LVPECL
SY89535L*		X	LVPECL	LVDS	LVPECL
SY89536L		X	LVPECL	HSTL	LVPECL

*Refer to individual data sheet for details.

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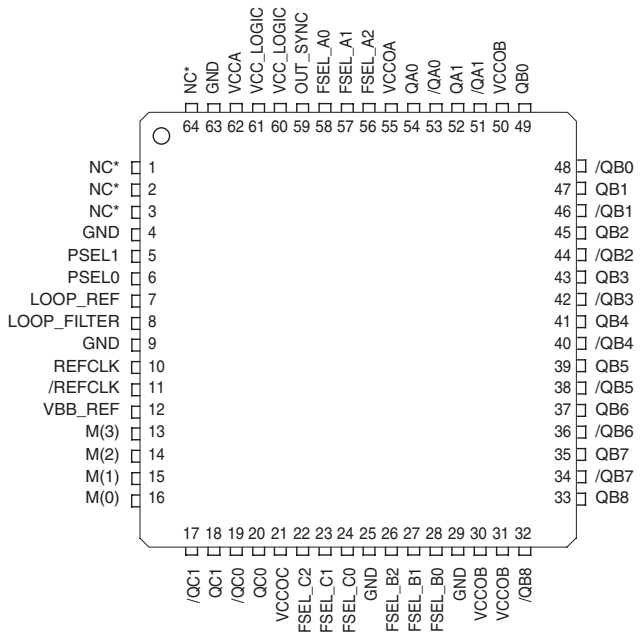
Issue Date: June 2003

PACKAGE/ORDERING INFORMATION



64-Pin EPAD-TQFP (H64-1)

*NC: Do not connect, leave floating.

Ordering Information

Part Number	Package Type	Operating Range	Package Marking
SY89536LHC	H64-1	Commercial	SY89536LHC

PIN DESCRIPTION

Power

Pin Number	Pin Name	Pin Function
60, 61	V_{CC_Logic}	Power for Core Logic: Connect to 3.3V supply. 3.3V power pins are not internally connected on the die, and must be connected together on the PCB.
62	V_{CCA}	Power for PLL: Connect to "quiet" 3.3V supply. 3.3V power pins are not internally connected on the die, and must be connected together on the PCB.
55 30, 31, 50 21	$V_{CCO}A$ $V_{CCO}B$ $V_{CCO}C$	Power for Output Drivers: Connect $V_{CCO}A$ and $V_{CCO}C$ pins to 3.3V supply and $V_{CCO}B$ pins to 1.8V supply.
4, 9, 25, 63, 29 (exposed pad)	GND	Ground: All GND pins must be tied together on the PCB. Exposed pad must be soldered to a ground plane.

Configuration

Pin Number	Pin Name	Pin Function
4	VCO_SEL	LVTTL/CMOS Compatible Input: Selects between internal or external VCO. When tied LOW (GND) internal VCO is selected. For external VCO, leave floating (default condition is logic HIGH). Internal 25kΩ pull-up.
5, 6	PSEL(1:0)	LVTTL/CMOS Compatible Input: Controls input frequency pre divider. Internal 25kΩ pull-up. Default is logic HIGH. See *"Pre-Divide Frequency Select"* table.
7	LOOP REF	Analog Input/Output: Provides the reference voltage for PLL loop filter.
8	LOOP FILTER	Analog Input/Output: Provides the loop filter for PLL. See *"External Loop Filter Considerations"* for loop filter values.
13,14,15,16	M (3:0)	LVTTL/CMOS Compatible Input: Used to change the PLL feedback divider. Internal 25kΩ pull-up. M0 = LSB. Default is logic HIGH. See *"Feedback Divide Select"* table.
22, 23, 24	FSEL_C (2:0)	LVTTL/CMOS Compatible Input: Bank C post-divide select. Internal 25kΩ pull-up. Default is logic HIGH. See *"Post-Divide Frequency Select"* table. FSEL_C0 = LSB.
26, 27, 28	FSEL_B (2:0)	LVTTL/CMOS Compatible Input: Bank B post-divide select. Internal 25kΩ pull-up. Default is logic HIGH. See *"Post-Divide Frequency Select"* table. FSEL_B0 = LSB.
56, 57, 58	FSEL_A (2:0)	LVTTL/CMOS Compatible Input: Bank A post-divide select. Internal 25kΩ pull-up. Default is logic HIGH. See *Post-Divide Frequency Select"* table. FSEL_A0 = LSB.
59	OUT_SYNC	Banks A, B, C Output Synchronous Control: (LVTTL/CMOS compatible). Internal 25kΩ pull-up. After any bank has been programmed, toggle with a HIGH-LOW-HIGH pulse to resynchronize all output banks.

Input/Output

Pin Number	Pin Name	Pin Function
1, 2, 3	NC	No Connect: Leave floating.
10, 11	REFCLK, /REFCLK	Reference Input: This flexible input accepts any input TTL/CMOS, LVPECL, LVDS, HSTL, SSTL logic levels. See *"Input Interface"* section.
12	VBB_REF	Reference Output Voltage. Used for single-ended input. Maximum sink/source current = 0.5mA.
51, 52, 53, 54	QA1 to QA0	Bank A 100k LVPECL Output Drivers: Output frequency is controlled by FSEL_A (0:2). Terminate outputs with 50Ω to V_{CC} –2V. See *"Output Termination Recommendations"* section.
32–49	QB8 to QB0	Bank B Output Drivers: Differential HSTL outputs. See *"Output Termination Recommendations"* section. Output frequency is controlled by FSEL_B (0:2).
17, 18, 19, 20	QC1 to QC0	Bank C 100k LVPECL Output Drivers: Output frequency is controlled by FSEL_C (0:2). Terminate outputs with 50Ω to V_{CC}–2V. See *"Output Termination Recommendations"* section.
64	NC	No Connect: Leave floating.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{IN}) ..... –0.5V to +4.0V
V_{CC} Pin Potential to Ground Pin (All V_{CC}) .. –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CCI}
DC Output Current (I_{OUT})
LVPECL, HSTL outputs ..... –50mA
Lead Temperature (soldering, 10 sec.) ..... 220°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings(Note 2)

Supply Voltage
V_{CCO}A and V_{CCO}C ..... 3.0V to +3.6V
V_{CCO}B ..... 1.6V to +2.0V
Ambient Temperature (T_A) ..... 0°C to +85°C
Package Thermal Resistance (Junction-to-Ambient)
With Die attach soldered to GND:
TQFP (θ_{JA}) Still-Air ..... 23°C/W
TQFP (θ_{JA}) 200lfpm ..... 18°C/W
TQFP (θ_{JA}) 500lfpm ..... 15°C/W
With Die attach NOT soldered to GND, **Note 3**:
TQFP (θ_{JA}) Still-Air ..... 44°C/W
TQFP (θ_{JA}) 200lfpm ..... 36°C/W
TQFP (θ_{JA}) 500lfpm ..... 30°C/W
Package Thermal Resistance (Junction-to-Case)
TQFP (θ_{JC}) ..... 4.0°C/W

DC ELECTRICAL CHARACTERISTICS

Power Supply

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CCA} V_{CC_LOGIC}	PLL and Logic Supply Voltage	**Note 4**	3.0	3.3	3.6	V
V_{CCO}A/C	Bank A and C V_{CC} Output		3.0	3.3	3.6	V
V_{CCO}B	Bank B V_{CC} Output LVPECL/HSTL		1.6	1.8	2.0	V
I_{CC}	Total Supply Current	**Note 5**	—	230	295	mA

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. It is recommended that the user always solder the exposed die pad to a ground plane for enhanced heat dissipation.

Note 4. V_{CCA}, V_{CC_LOGIC}, V_{CCO}A/C are *not* internally connected together inside the device. They must be connected together on the PCB. V_{CCO}B is a separate supply.

Note 5. No load. Outputs floating, Banks A, B, and C enabled.

DC ELECTRICAL CHARACTERISTICS

LVCMOS/LVTTL Input Control Logic (V_{CCA}, V_{CC_LOGIC}, V_{CCO}A/C pins = +3.3V ±10%)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0	—	—	V
V_{IL}	Input LOW Voltage		—	—	0.8	V
I_{IH}	Input HIGH Current		—	—	150	µA
I_{IL}	Input LOW Current		—	—	–300	µA

REFCLK (Pins 10, 11) INPUT (All V_{CC} pins except V_{CCO}B = +3.3V ±10%, V_{CCO}B = +1.8V ±10%)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{ID}	Differential Input Voltage		100	—	—	mV
V_{IH}	Input HIGH Voltage		—	—	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage		–0.3	—	—	V

100k LVPECL Outputs (All V_{CC} pins except V_{CCO}B = +3.3V ±10%, V_{CCO}B = +1.8V ±10%)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	**Note 6**	V_{CC}–1.145	V_{CC}–1.020	V_{CC}–0.895	V
V_{OL}	Output LOW Voltage	**Note 6**	V_{CC}–1.945	V_{CC}–1.820	V_{CC} –1.695	V
V_{ID}	Differential Input Voltage	**Note 7**	100 200	— —	— —	mV mV
V_{IH}	Input HIGH Voltage	**Note 7**	—	—	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage	**Note 7**	–0.3	—	—	V
I_{IH}	Input HIGH Current		–600	—	–300	µA
I_{IL}	Input LOW Current		–1200	—	–700	µA
V_{BB}	Output Reference Voltage		V_{CC}–1.325	V_{CC}–1.425	V_{CC}–1.525	V

HSTL Outputs (Bank B QB0:8) (All V_{CC} pins except V_{CCO}B = +3.3V ±10%, V_{CCO}B = +1.8V ±10%)**(Note 8)**

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing		—	800	—	mV
V_{OH}	Output HIGH Voltage		1.0	—	1.2	V
V_{OL}	Output LOW Voltage		0.2	—	0.4	V

Note 6. 50Ω to V_{CC} –2V. Banks A, B, and C enabled.

Note 7. V_{CC} = 3.0V to 3.6V.

AC ELECTRICAL CHARACTERISTICS

V_{CC_LOGIC} = V_{CC}A/C = +3.3V ±10%, V_{CCO}B = +1.8V ±10%

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{IN}	Reference Input Frequency		14	—	160	MHz
f_{OUT}	Output Frequency Range		33.33	—	500	MHz
t_{VCO}	Internal VCO Frequency Range		600	—	1000	MHz
t_{skew}	Within Device Skew Within Bank PECL	**Note 9**	—	—	50	ps
	Within Bank HSTL	**Note 9**	—	—	75	ps
	Bank-to-Bank	**Note 9**	—	60	150	ps
	Part-to-Part Skew	**Note 10**	—	—	200	ps
t_{LOCK}	Maximum PLL Lock Time		—	—	10	ms
t_{JITTER}	Cycle-to-Cycle Jitter (Pk-to-Pk)	**Note 11**	—	—	50	ps
	Period Jitter (rms)	**Note 12**	—	50	—	ps
t_{pw} (min)	Minimum Pulse Width		50	—	—	ps
	Target PLL Loop Bandwidth Feedback Divider Ratio: 66 Feedback Divider Ratio: 30	 **Note 13** **Note 13**	 — —	 1.0 2.0	 — —	 MHz MHz
t_{DC}	f_{OUT} Duty Cycle		45	50	55	%
t_r, t_f	Output Rise/Fall Time (20% to 80%) LVPECL_Out HSTL_Out		 — 100	 250 —	 400 400	 ps ps
t_{OUTPUT_RESET}		**Note 14**	—	—	10	ns
t_{HOLD_FSEL}		**Note 14**	5	—	—	ns
t_{SETUP_FSEL}		**Note 14**	5	—	—	ns
t_{OUTPUT_SYNC}		**Note 14**	1	—	—	VCO clock cycle
FSEL-to-Valid Output Transition Time			—	50	—	ns
$t_{SETUP\_OUT\_SYNC}$			500	—	—	ps

Note 8. All HSTL outputs loaded with 50Ω to GND.

Note 9. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device operating at the same voltage and temperature.

Note 10. The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature.

Note 11. Cycle-to-cycle jitter definition: The variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{JITTER\_CC} = T_n - T_{n+1}$ where T is the time between rising edges of the output signal.

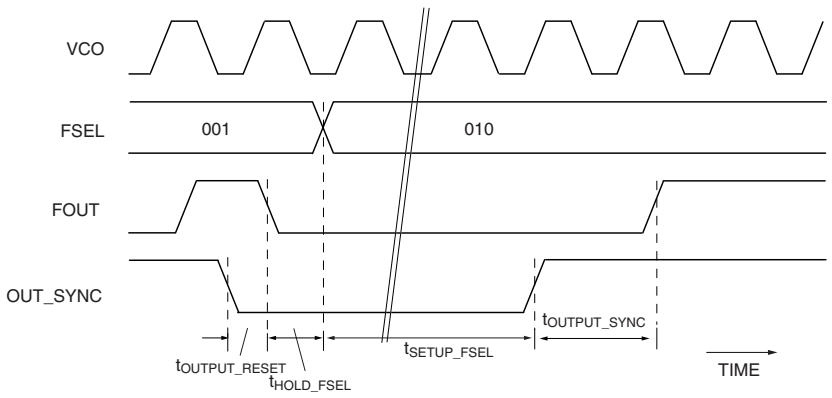
Note 12. Period Jitter definition: For a specified amount of time (i.e., 1ms), there are N periods of a signal, and T_n is defined as the average period of that signal. Period jitter is defined as the variation in the period of the output signal for corresponding edges relative to T_n.

Note 13. Using recommended loop filter components.

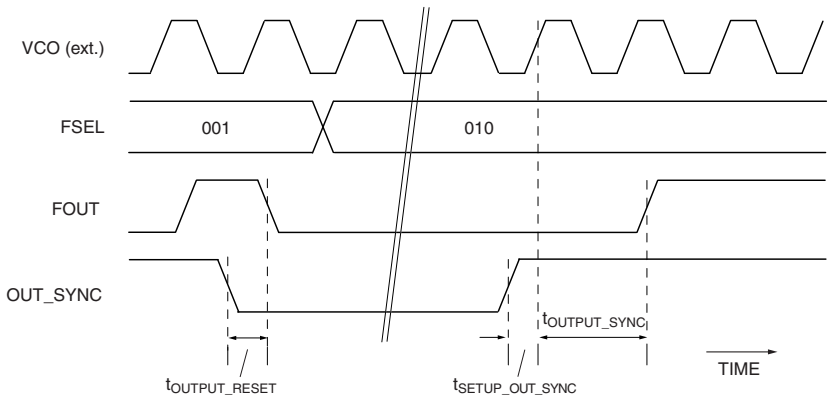
Note 14. See *"Timing Diagrams."*

TIMING DIAGRAMS

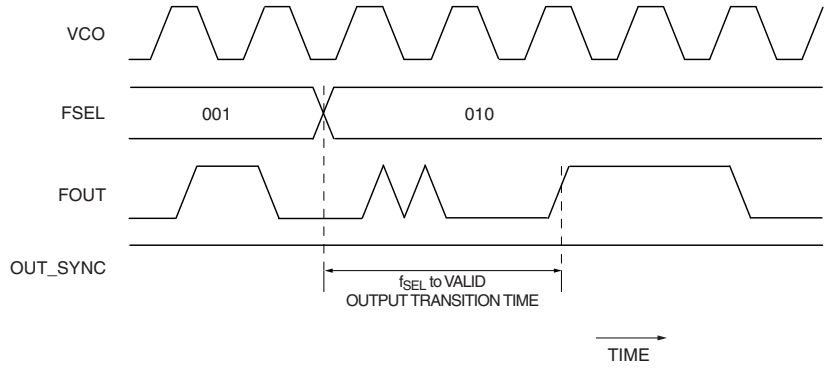
Conditions: Internal VCO, unless otherwise stated.



Frequency Programming

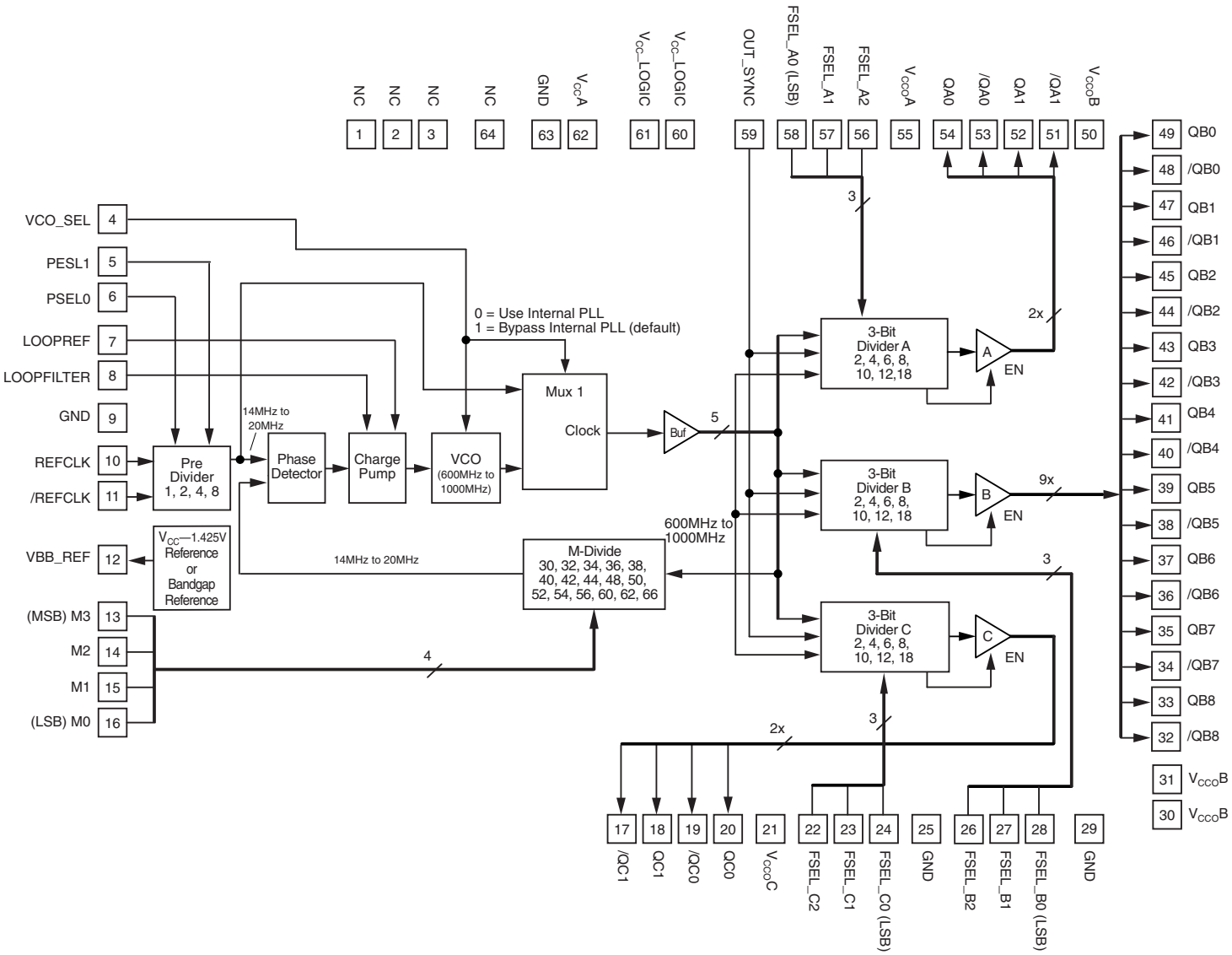


Frequency Programming (External VCO Clock)



Output Frequency Updates to Valid Output

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

At the core of the SY89536L clock synthesizer is a precision PLL driven by a differential or single-ended reference input. For users who wish to supply a crystal input, please use the SY89531L. The PLL output is sent to three banks of outputs. Each bank has its own programmable frequency divider, and the design is optimized to provide very low skew between banks, and very low jitter.

PLL Programming and Operation

IMPORTANT: If the internal VCO will be used, VCO_SEL **must** be tied LOW, and ExtVCO pins can be left unconnected. The internal VCO range is 600MHz to 1000MHz, and the feedback ratio is selectable via the MSEL divider control (M3:0 pins). The feedback ratio can be changed without powering the chip down. The PLL output is fed to three banks of outputs: Bank A, Bank B, and Bank C. Banks A and C each have two differential LVPECL output pairs. Bank B has nine differential HSTL output pairs.

Each bank has a separate frequency divider circuit that can be reprogrammed on the fly. The FSEL_x0:2 (where x is A, B, or C) pins control the divider value. The FSEL divider can be programmed in ratios from 2 to 18, and the outputs of Banks A, B, and C can be synchronized after programming by pulsing the OUT_SYNC pin HIGH-LOW-HIGH. Setting a value of 000 for FSEL is an output disable forcing the Q outputs to be LOW and the /Q outputs to be HIGH. Doing so will decrease power consumption by approximately 5mA per bank.

To determine the correct settings for SY89536L follow these steps:

1. Refer to the *"Suggested Selections for Specific Customer Applications"* section for common applications, as well as the formula used to compute the output frequency.

2. Determine the desired output frequency, such as 66MHz.

3. Choose a reference input frequency between 14MHz and 20MHz. The user can also choose a higher input frequency, and use the PSEL pre-divider to divide it down to the 14MHz to 20MHz range. In this example, we choose 18MHz for the reference input frequency. This results in an input/output ratio of 66/18.

4. Refer to the *"Feedback Divide Select"* table and the *"Post-Divide Frequency Select"* table to find values for MSEL and FSEL such that MSEL/FSEL equals the same 66/18 ratio. In this example, values of MSEL=44 and FSEL=12 work.

5. Make sure that REFCLK ÷ PSEL × MSEL is between 600MHz and 1000MHz.

The user may need to experiment with different REFCLK input frequencies to satisfy these requirements.

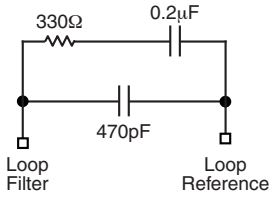


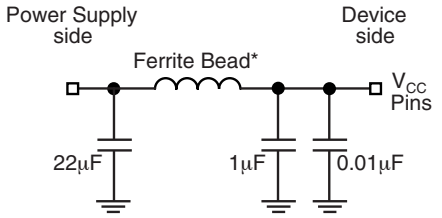
Figure 1. External Loop Filter Connection

External Loop Filter Considerations

The SY89536L features an external PLL loop filter that allows the user to tailor the PLL's behavior to their application and operating environment. We recommend using ceramic capacitors with NPO or X7R dielectric, as they have very low effective series resistance. For applications that require ultra-low cycle-to-cycle jitter, use the components shown in Figure 1. The PLL loop bandwidth is a function of feedback divider ratio, and the external loop filter allows the user to compensate. For instance, the PLL's loop bandwidth can be decreased by using a smaller resistor in the loop filter. This results in less noise from the PLL input, but potentially more noise from the VCO. Refer to *"AC Electrical Characteristics"* for target PLL loop bandwidth. The designer should take care to keep the loop filter components on the same side of the board and as close as possible to the SY89536L's LOOP_REF and LOOP_FILTER pins. To insure minimal noise pick-up on the loop filter, it is desirable to cut away the ground plane directly underneath the loop filter component pads and traces. However, the benefit may not be significant in all applications and one must be careful to not alter the characteristic impedance of nearby traces.

Power Supply Filtering Techniques

As with any high-speed integrated circuit, power supply filtering is very important. At a minimum, V_{CC}A, V_{CC}_Logic, and all V_{CCO} pins should be individually connected using a via to the power supply plane, and separate bypass capacitors should be used for each pin. To achieve optimal jitter performance, each power supply pin should use separate instances of the circuit shown in Figure 2.



*For V_{CC}_Analog, V_{CC_TTL}, V_{CC1}, use ferrite bead = 200mA, 0.45Ω DC, Murata P/N BLM21A1025

*For V_{CCO}A,B,C use ferrite bead = 3A, 0.025Ω DC, Murata, P/N BLM31P005

*Component size: 0805

Figure 2. Power Supply Filtering

Output Logic Characteristics

See *"Output Termination Recommendations"* for illustrations. In cases where single-ended output is desired, the designer should terminate the unused complimentary output in the same manner as the normal output that is being used. Unused output pairs can be left floating.

LVPECL operation:

- Typical voltage swing is 700mV$_{PP}$ to 800mV$_{PP}$ into 50Ω.
- Common mode voltage is V_{CC}–1.3V, typical.
- 100Ω termination across the output pair is NOT recommended for LVPECL. See *"Output Termination"* section, Figures 5 to 7.

HSTL operation (Bank B):

- Typical voltage swing is 250mV$_{PP}$ to 450mV$_{PP}$ into effective 50Ω.

Thermal Considerations

This part has an exposed die pad for enhanced heat dissipation. We strongly recommend soldering the exposed die pad to a ground plane. Where this is not possible, we recommend maintaining at least 500lfpm air flow around the part.

For additional information on exposed-pad characteristics and implementation details, see Amkor Technology's web site, www.amkor.com.

REFCLK Input Interface

The flexible REFCLK inputs are designed to accept any differential or single-ended input signal within 300mV above V_{CC} and 300mV below ground.

Do not leave unused REFCLK inputs floating. Tie either the true or complement inputs to ground, but not both. A logic zero is achieved by connecting the complement input to ground with the true input floating. For a TTL input, tie a resistor between the complement input and ground. See *"Input Interface"* section, Figures 4a through 4h.

Input Levels

LVDS, CML and HSTL differential signals may be connected directly to the REFCLK inputs. Depending on the actual worst case voltage seen, the minimum input voltage swing varies.

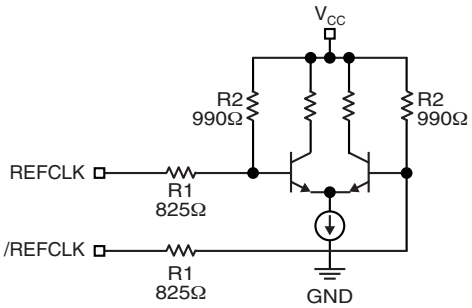


Figure 3. Simplified Input Structure

PRE-DIVIDE FREQUENCY SELECT TABLE (PSEL)

PSEL1 (MSB)	PSEL0	Reference Input Frequency
0	0	REFCLK ÷ 8
0	1	REFCLK ÷ 4
1	0	REFCLK ÷ 2
1	1	REFCLK ÷ 1

POST-DIVIDE FREQUENCY SELECT TABLE (FSEL)

FSEL_A2[1] (MSB)	FSEL_A1[1]	FSEL_A0[1] (LSB)	Output Divider
0	0	0	Output Disable Function, all outputs: Q = LOW, /Q = HIGH
0	0	1	VCO ÷ 2
0	1	0	VCO ÷ 4
0	1	1	VCO ÷ 6
1	0	0	VCO ÷ 8
1	0	1	VCO ÷ 10
1	1	0	VCO ÷ 12
1	1	1	VCO ÷ 18

Note 1. Same dividers apply to FSEL_B (0:2) and FSEL_C (0:2).

FEEDBACK DIVIDE SELECT TABLE (MSEL)

M3	M2	M1	M0	VCO Frequency[1]
0	0	0	0	REFCLK ÷ PSEL × 34
0	0	0	1	REFCLK ÷ PSEL × 36
0	0	1	0	REFCLK ÷ PSEL × 38
0	0	1	1	REFCLK ÷ PSEL × 40
0	1	0	0	REFCLK ÷ PSEL × 42
0	1	0	1	REFCLK ÷ PSEL × 44
0	1	1	0	REFCLK ÷ PSEL × 48
0	1	1	1	REFCLK ÷ PSEL × 50
1	0	0	0	REFCLK ÷ PSEL × 52
1	0	0	1	REFCLK ÷ PSEL × 54
1	0	1	0	REFCLK ÷ PSEL × 56
1	0	1	1	REFCLK ÷ PSEL × 60
1	1	0	0	REFCLK ÷ PSEL × 62
1	1	0	1	REFCLK ÷ PSEL × 66
1	1	1	0	REFCLK ÷ PSEL × 30
1	1	1	1	REFCLK ÷ PSEL × 32

SUGGESTED SELECTIONS FOR SPECIFIC CUSTOMER APPLICATIONS[Notes 1, 2, 3]

Protocol	Rate (MHz)	FSEL (Post Divider)	MSEL (Feedback Div.)	REFCLK (MHz)	PSEL	FOUT
PCI	33	18	36	16.67	1	33
Fast Ethernet	100	6	40	15	1	100
1/8 FC	133	6	52	15.36	1	133
ESCON	200	4	50	16	1	200

$$FOUT = \frac{(REFCLK \div PSEL \times MSEL)}{FSEL}$$

Note 1. 600MHz < (REFCLK ÷ PSEL × MSEL) < 1000MHz.

Note 2. 14MHz ≤ (REFCLK ÷ PSEL) ≤ 20MHz.

Note 3. Where two settings provide the user with the identical desired frequency, the setting with the higher PLL input reference frequency (and lower feedback divider) will usually have lower output jitter. However, the reference input frequency, as well as the VCO frequency, must be kept within their respective ranges.

INPUT INTERFACE

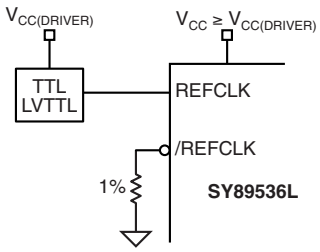


Figure 4a. 3.3V "TTL"

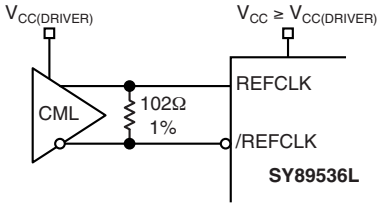


Figure 4b. CML DC-Coupled

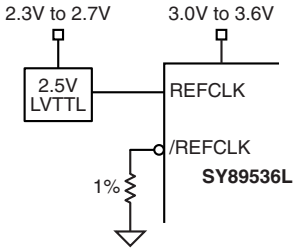


Figure 4c. 2.5V "LVTTL"

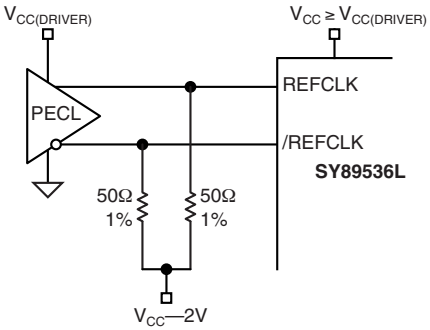


Figure 4d. 3.3V LVPECL DC-Coupled

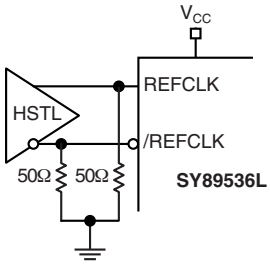


Figure 4e. HSTL

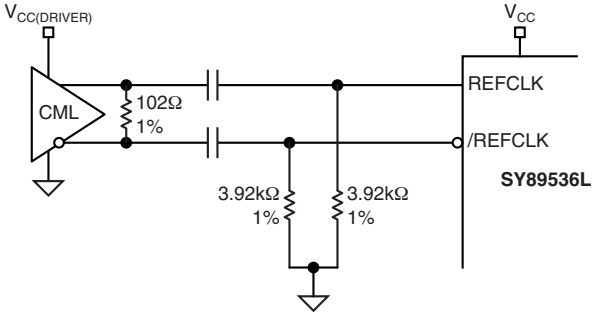


Figure 4f. CML AC-Coupled (Short Trace Lengths)

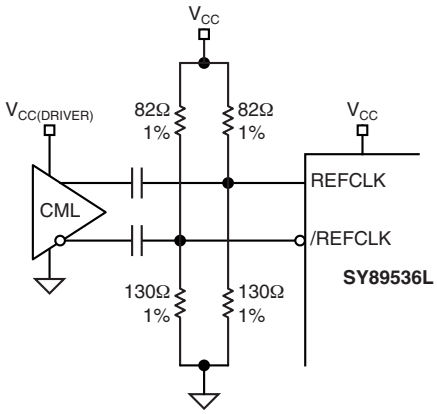


Figure 4g. CML AC-Coupled (Long Trace Lengths)

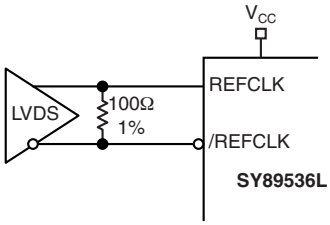


Figure 4h. LVDS

OUTPUT TERMINATION RECOMMENDATIONS

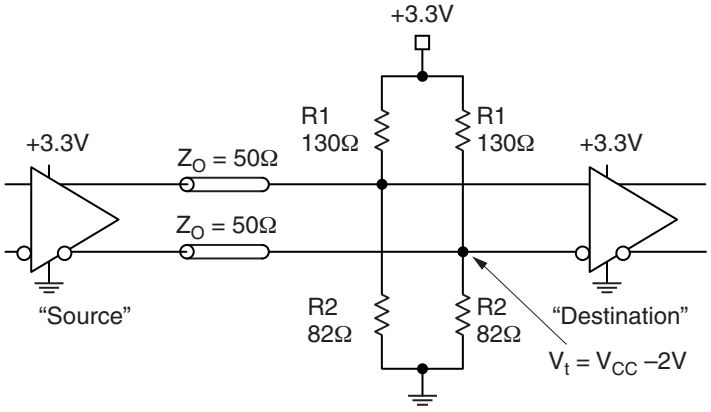


Figure 5. PECL Parallel Termination Thevenin Equivalent (Note 1)

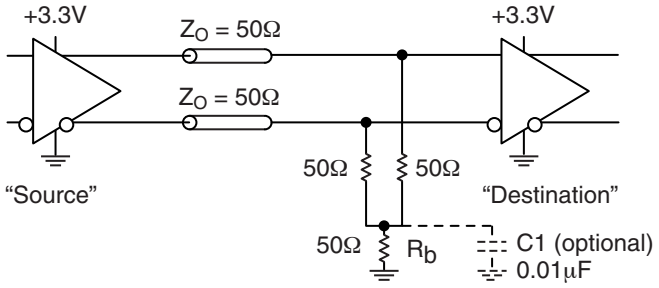


Figure 6. PECL Three-Resistor "Y-Termination" (Notes 1, 2, 3)

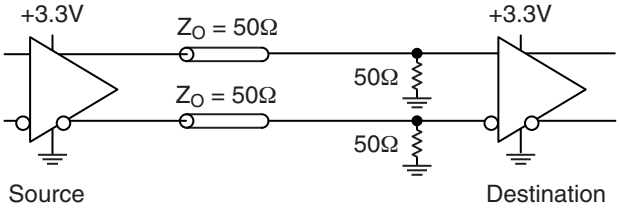


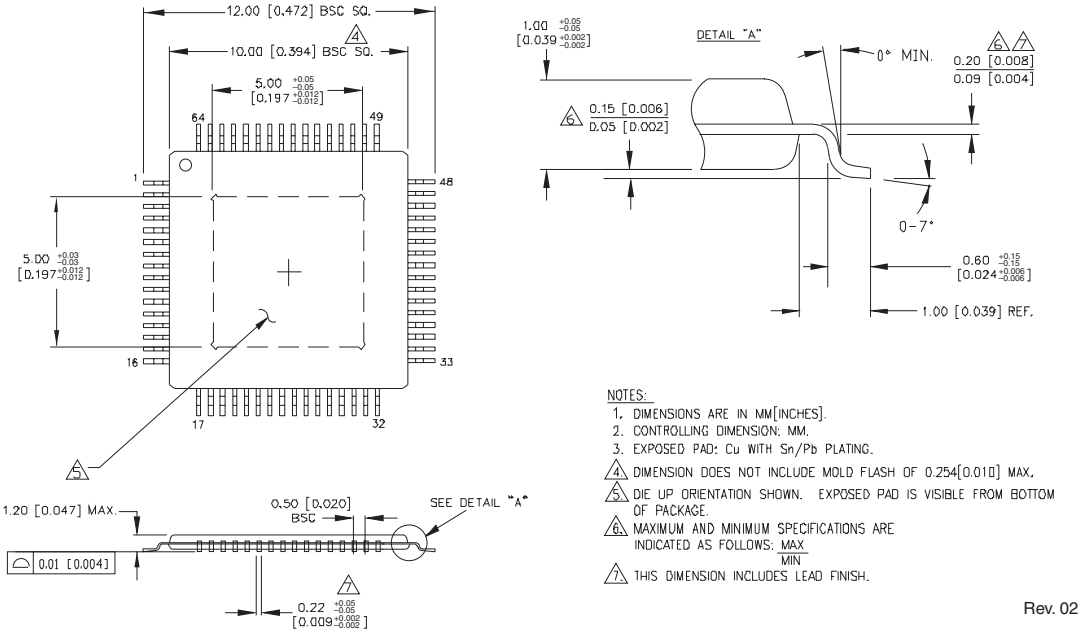
Figure 7. HSTL Differential Termination (Note 1)

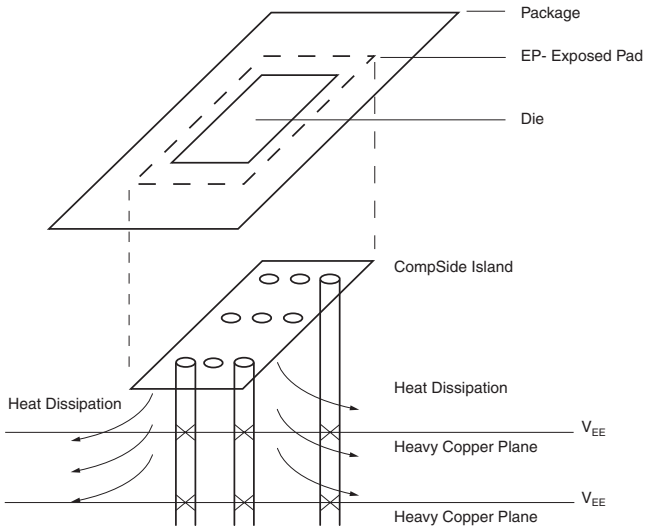
Note 1. Place termination resistors as close to destination inputs as possible.

Note 2. PECL Y-termination is a power-saving alternative to Thevenin termination.

Note 3. R_b resistor sets the DC bias voltage, equal to V_t. For +3.3V systems R_b = 46Ω to 50Ω.

64 LEAD EPAD-TQFP (DIE UP) (H64-1)





PCB Thermal Consideration for 64-Pin EPAD-TQFP Package

Package Notes:

Note 1. Package meets Level 2 moisture sensitivity classification, and is shipped in dry-pack form.

Note 2. Exposed pads must be soldered to a ground for proper thermal management.

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