Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

The PT2310 is an electronic volume controller IC designed for audio equipment. Utilize CMOS Technology; it has 2 individual channels attenuator built inside and ideal for both mono and stereo applications. The PT2310 provides wide frequency response range, very low total harmonic distortion and low noise. It also has a built-in loudness compensation function for the sound effect improvement.

FEATURES

- CMOS Technology
- Low Power Consumption
- Two channel independent volume attenuator
- Simplified External Components
- Wide Supply Voltage 4.5V~12V, controlled by MCU interface
- Attenuation Range 0dB~-78dB (2dB/Step)
- Built-in Loudness Compensation Function
- Wide Frequency Response, Low Total Harmonic Distortion and Low Noise
- Available in 16 Pins DIP and 16 Pins SOP

APPLICATIONS

- Audio Equipments
- TV
- Multi-media Sound Device

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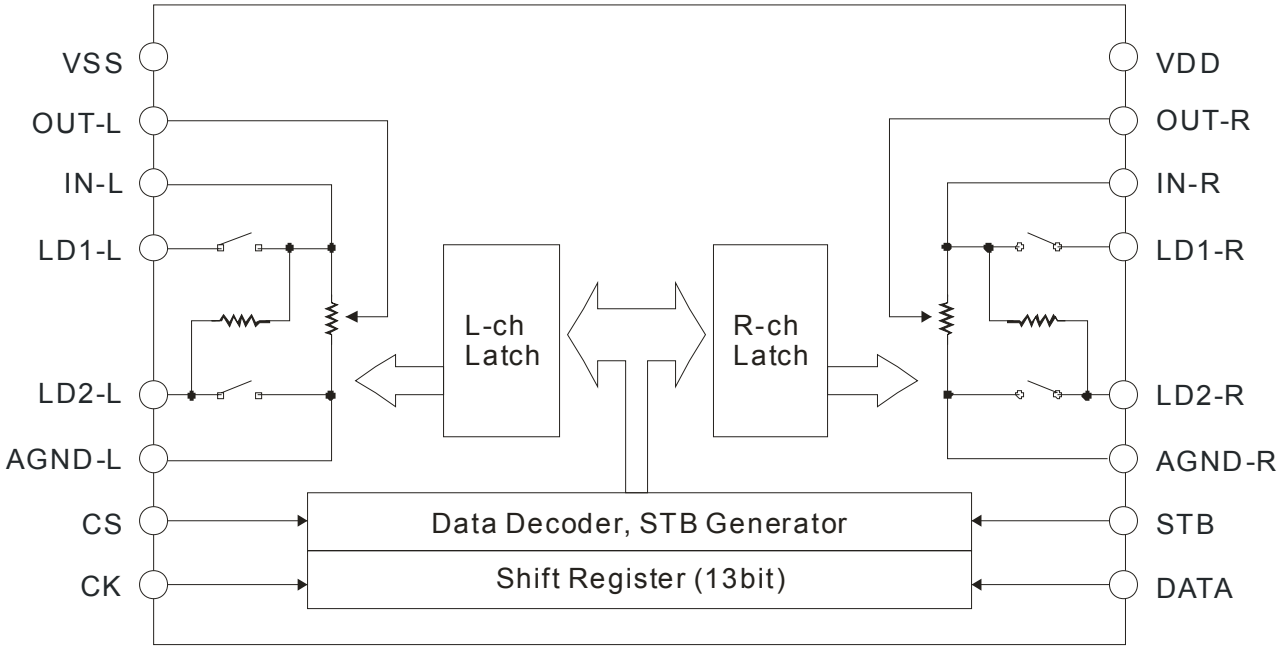
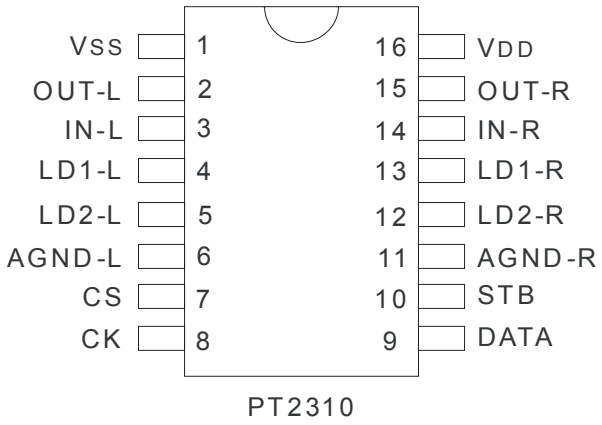
BLOCK DIAGRAM



PIN CONFIGURATION



PT2310

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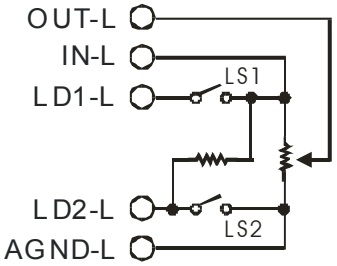
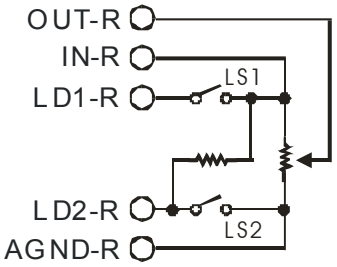
PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description	Function
1	V_{SS}	-	Supply voltage input (-)	-
2	OUT-L	O	Left channel output	Volume control circuit:  (Loudness On: LS1=On, LS2=Off)
3	IN-L	I	Left channel input	
4	LD1-L	O	Left channel volume loudness tap (1)	
5	LD2-L	O	Left channel volume loudness tap (2)	
6	AGND-L	-	Analog ground	
7	CS	-	Chip select pin	C2、C3、C4 Fixed codes are 0, 1, 1 When CS=1, C1=1 When CS=0, C1=0 (see P.5 description)
8	CK	I	Clock input	-
9	DATA	I	Data code input	Attenuation value is defined by the data code; the data code is consisting of 13bits.
10	STB	I	Strobe	After the DATA & CK codes were sent, a high strobe pulse in STB pin to confirm the data is validity.
11	AGND-R	-	Analog ground	Volume control circuit:  (Loudness On: LS1=On, LS2=Off)
12	LD2-R	O	Right channel volume loudness tap (2)	
13	LD1-R	O	Right channel volume loudness tap (1)	
14	IN-R	I	Right channel input	
15	OUT-R	O	Right channel output	
16	V_{DD}	-	Supply voltage input (+)	-

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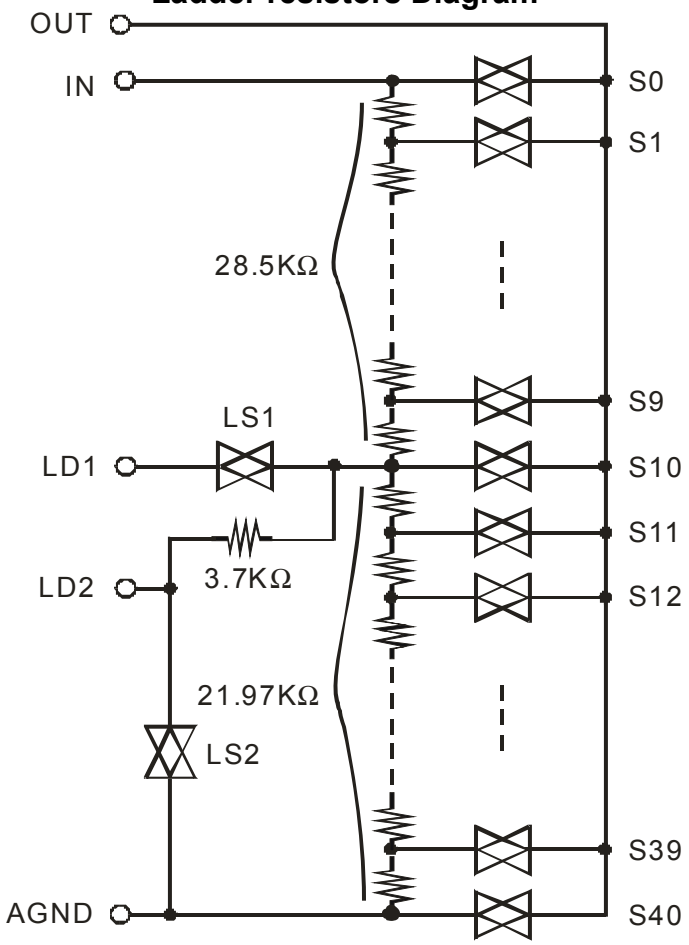
FUNCTION DESCRIPTION

ATTENUATION

The PT2310 volume attenuator is consists of resistor ladder and analog switch. The Tap for loudness function is connected to the Step 10 (-20 dB). The relations of step and attenuation is given in table below

Step	dB	Step	dB
0	0	21	-42
1	-2	22	-44
2	-4	23	-46
3	-6	24	-48
4	-8	25	-50
5	-10	26	-52
6	-12	27	-54
7	-14	28	-56
8	-16	29	-58
9	-18	30	-60
10	-20	31	-62
11	-22	32	-64
12	-24	33	-66
13	-26	34	-68
14	-28	35	-70
15	-30	36	-72
16	-32	37	-74
17	-34	38	-76
18	-36	39	-78
19	-38	40	-∞
20	-40		

Ladder resistors Diagram



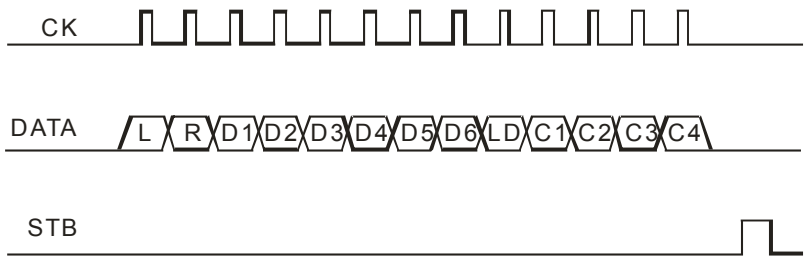
Note:
1. Loudness On: LS1=On, LS2=Off
2. Loudness Off: LS1=Off, LS2=On

SERIAL BUS INTERFACE

The DATA, CK and STB pins consist of bus line; the bus line is for communication with the MCU and the PT2310.

SERIAL DATA CODE

The data code is consists by L, R, D1~D4, LD, C1~C4 (totally 13 bits), at the end of the code there needs a high strobe pulse to confirm the data code is validity.



CHIP SELECTION (C1~C4)

The Chip Selection code C1 is depending on the states of the CS pin, the CS pin in low state means the C1 bit=0; and the CS pin in high state means the C1 bit=1. Ignore what states of the CS pin the C2, C3 and C4 bit is presets to the state 0, 1, 1.

CS	C1	C2	C3	C4
“1”	1	0	1	1
“0”	0	0	1	1

LEFT AND RIGHT CHANNEL CONTROL CODE

In the DATA code, the “L” bit is for left channel and the “R” is for right channel is selected. If the “L” bit is 1 means the attenuation value (D1 to D6) is for left channel exclusively; and if “L” and “R” all are “1” means attenuation value is for the both channel.

LOUDNESS SETUP CODE

The “LD” bit In the DATA code is for the Loudness function. When the “LD” bit is 0, the Loudness function is turned off (LS1=Off, LS2=ON) and the “LD” bit is 1 means the Loudness is turned ON (LS1=On, LS2=Off).

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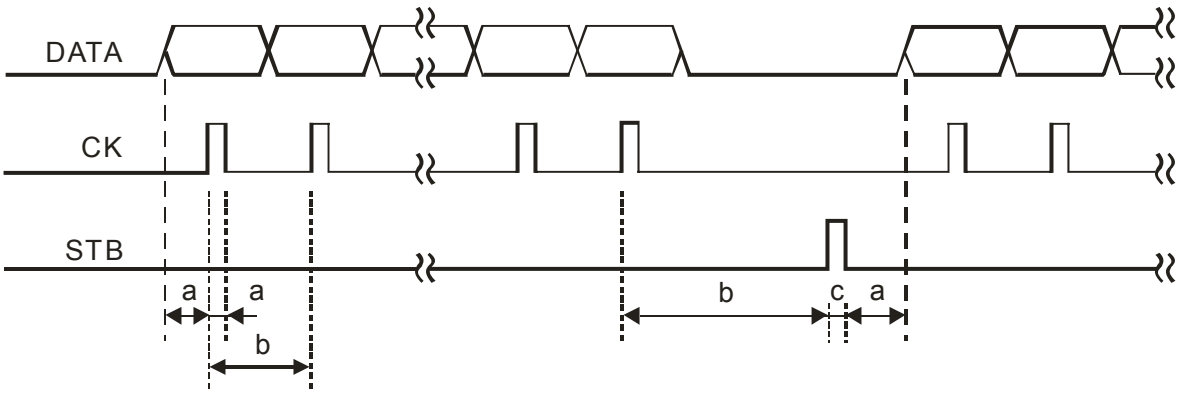
VOLUME SETUP CODE (D1~D6)

In the DATA code, “D1~D6” is defined to the volume attenuation value. Please refer the table is shown on below for the relation of volume setup code of each step.

Volume Value (dB)	D1	D2	D3	D4	D5	D6	Volume Value (dB)	D1	D2	D3	D4	D5	D6
0	0	0	0	0	0	0	40	0	0	1	0	1	0
2	1	0	0	0	0	0	42	1	0	1	0	1	0
4	0	1	0	0	0	0	44	0	1	1	0	1	0
6	1	1	0	0	0	0	46	1	1	1	0	1	0
8	0	0	1	0	0	0	48	0	0	0	1	1	0
10	1	0	1	0	0	0	50	1	0	0	1	1	0
12	0	1	1	0	0	0	52	0	1	0	1	1	0
14	1	1	1	0	0	0	54	1	1	0	1	1	0
16	0	0	0	1	0	0	56	0	0	1	1	1	0
18	1	0	0	1	0	0	58	1	0	1	1	1	0
20	0	1	0	1	0	0	60	0	1	1	1	1	0
22	1	1	0	1	0	0	62	1	1	1	1	1	0
24	0	0	1	1	0	0	64	0	0	0	0	0	1
26	1	0	1	1	0	0	66	1	0	0	0	0	1
28	0	1	1	1	0	0	68	0	1	0	0	0	1
30	1	1	1	1	0	0	70	1	1	0	0	0	1
32	0	0	0	0	1	0	72	0	0	1	0	0	1
34	1	0	0	0	1	0	74	1	0	1	0	0	1
36	0	1	0	0	1	0	76	0	1	1	0	0	1
38	1	1	0	0	1	0	78	1	1	1	0	0	1
							∞	0	0	0	1	0	1

SERIAL BUS TIMING



Note: a>1μs, b>2μs, c>2μs

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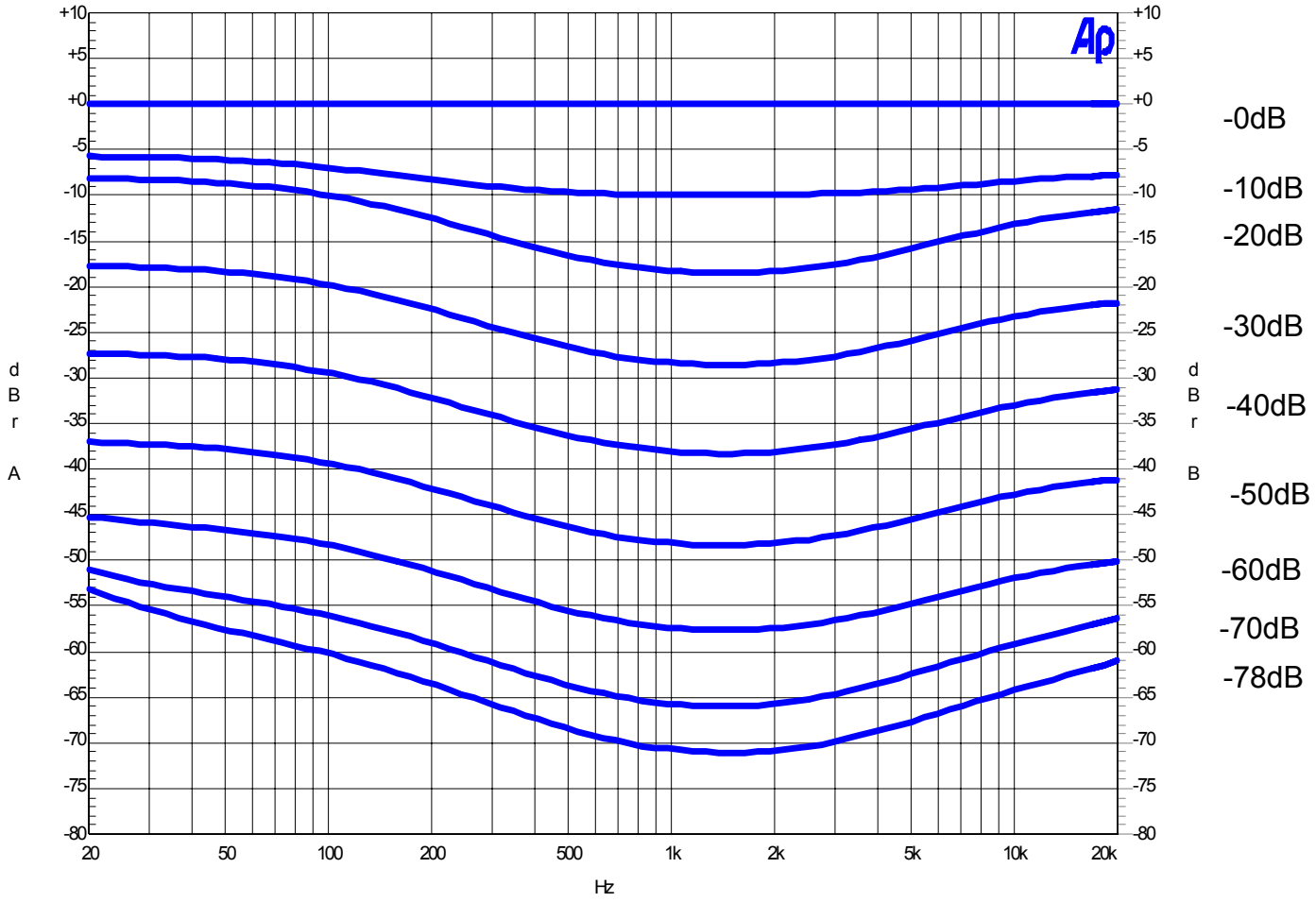
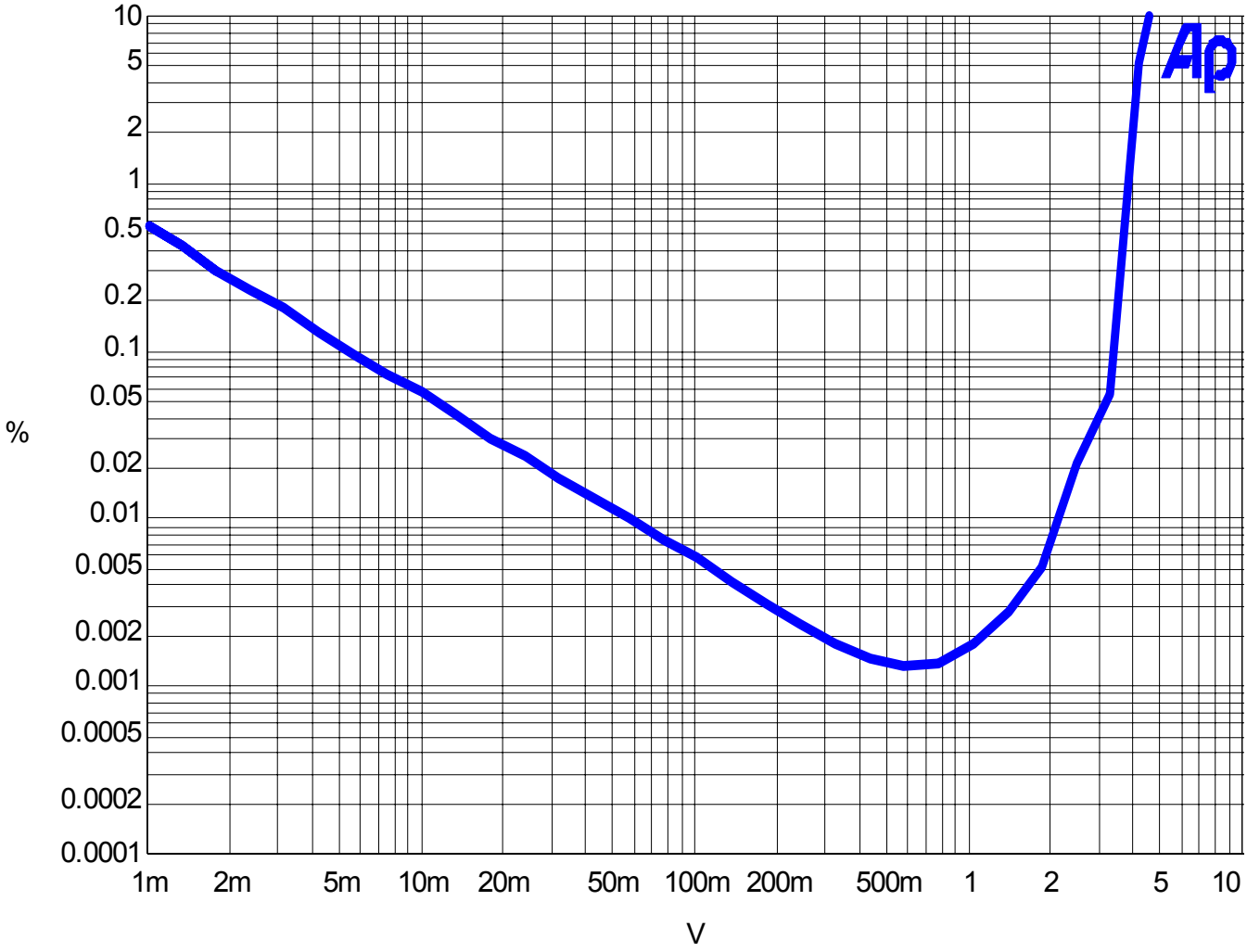
LOUDNESS FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION VS. INPUT LEVEL



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ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

Parameter	Symbol	Rating	Unit
Maximum supply voltage	V_{DD}	-0.3 ~ 15	V
Input voltage	V_{IN}	-0.3 ~ VDD+0.3	V
Power dissipation	P_D	300	mW
Operating temperature	Topr	-40 ~ +85	℃
Storage temperature	Tstg	-65 ~ +150	℃

ELECTRONICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25℃, V_{DD}=9V)

Parameter	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}			4.5	9.0	12	V
Operating current	I_{DD}	No load, F=20Hz		-	0.3	1.0	mA
Quiescent current	Iq	IN, OUT, CK, CS, SATA, STB connect to VSS		-	0.1	10	μA
Input high level voltage	V_{IH}	CK, DATA, STB, V_{DD}=5V		4	-	V_{DD}	V
		CS, V_{DD}=10V		$0.7V_{DD}$	-	V_{DD}	V
Input low level voltage	V_{IL}	CK, DATA, STB, V_{DD}=5V		0	-	1	V
		CS, V_{DD}=10V		0	-	$0.3V_{DD}$	V
Input high level current	I_{IH}	V_{IL}=V_{DD}		-1	-	1	μA
Input low level current	I_{IL}	V_{IL}=0V		-1	-	1	μA
Resistance of Attenuator	R_{VR}			20	28	37	KΩ
Resistance of analog switch	R_{ON}	When 0dB, the resistance between IN1~OUT1 and IN2~OUT2		-	250	600	Ω
Two Channel Attenuation error	ΔATT			-	0	±2	dB
Channel Balance	ΔR_{VR}	Vin=1Vrms		-	0	±3	%
Total harmonic distortion	THD	1.Input Frequency: 1KHz 2. Input voltage: 1Vrms 3. Test equipment input resistance=100KΩ 4. Test equipment output resistance=600Ω	0dB	-	0.01	-	%
Max. attenuation	ATTmax		∞dB	-	100	-	dB
Crosstalk	CT		0dB	-	100	-	dB
Residual noise	V_N		0dB	-	2	-	μVrms
Maximum Bus. Operation Frequency	Fop	-		10	-	500K	Hz
Minimum pulse duty	T_{CK}	CK input		-	0.5	1	μs
	T_{STB}	STB input		-	1	2	

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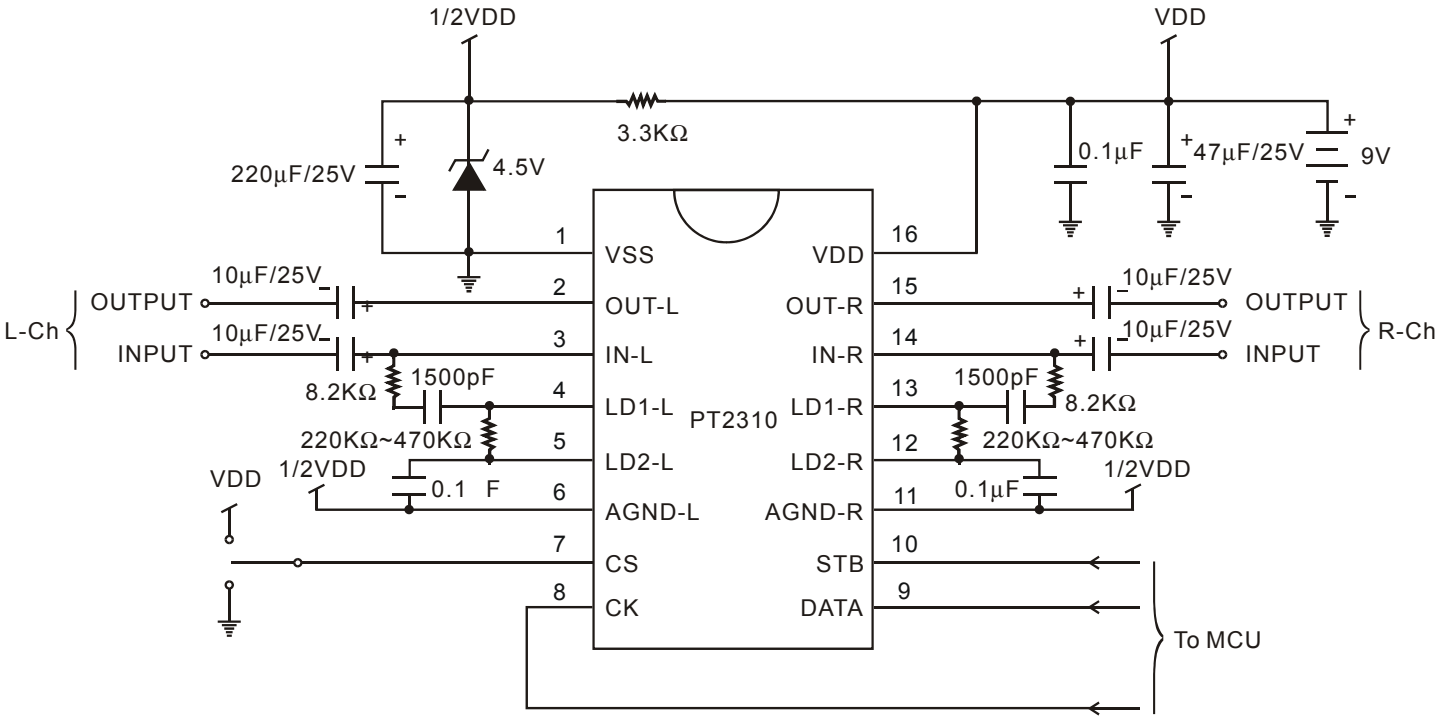
APPLICATION CIRCUIT 1



Note: With Loudness function

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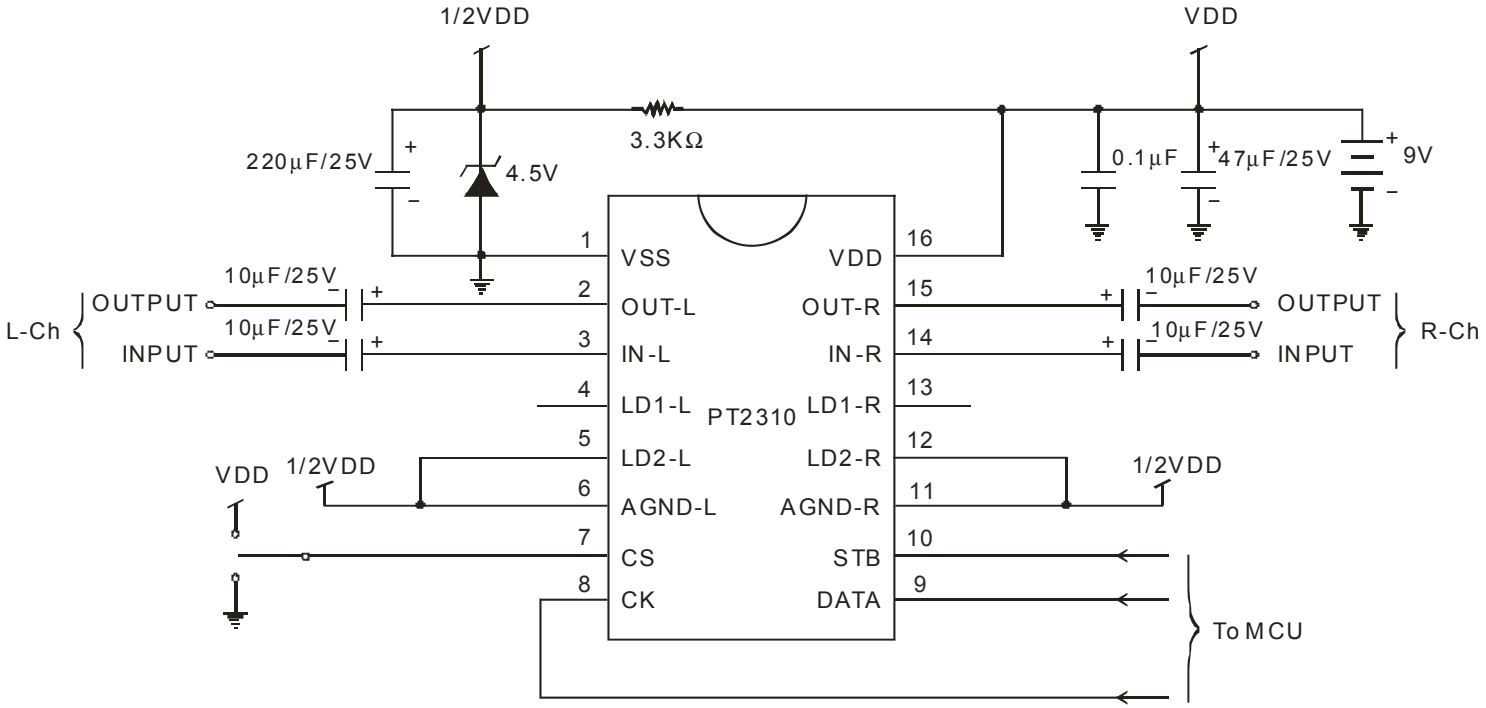
APPLICATION CIRCUIT 2



Note: Without Loudness function

ORDER INFORMATION

Order Part Number	Package Type	Top Code
PT2310	16 Pins, DIP, 300mil	PT2310
PT2310-S	16 Pins, SOP, 300mil	PT2310-S
PT2310 (L)	16 Pins, DIP, 300mil	PT2310
PT2310-S (L)	16 Pins, SOP, 300mil	PT2310-S

Note:
1. (L), (C) or (S) = Lead Free
2. The Lead Free mark is put in front of the data code.

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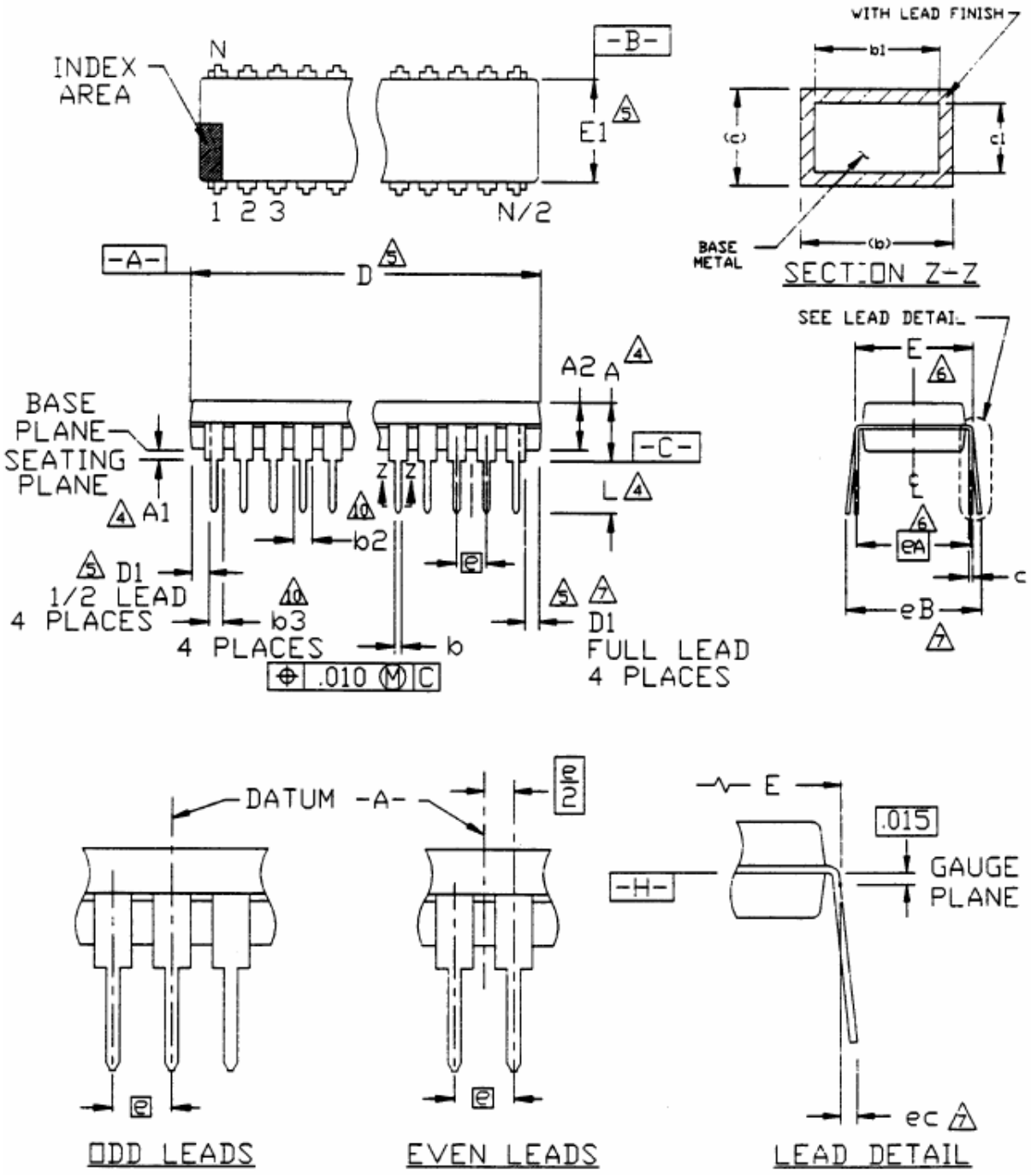
PACKAGE INFORMATION

16 PINS, DIP, 300MIL



Symbol	Min.	Nom.	Max.
A			0.210
A1	0.015		
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.780	0.790	0.800
D1	0.005		
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	0.100 bsc.		
eA	0.300 bsc.		
eB			0.430
eC	0.000		0.060
L	0.115	0.130	0.150

Notes：
1. All dimensions are in INCHS.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimensions “A”, “A1” and “L” are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. “D”, “D1” and “E1” dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. “E” and “eA” measured with the leads constrained to be perpendicular to datum -c-.
6. “eB” and “eC” are measured at the lead tips with the loads unconstrained.
7. “N” is the number of terminal positions. (N=16)
8. Pointed or rounded lead tips are preferred to ease insertion.
9. “b2” and “b3” maximum dimensions are not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25 mm).
10. Distance between leads including Dambar protrusions to be 0.005 inch minimum.
11. Datum plane -H- coincident with the bottom of lead, where lead exits body.
12. Refer to JEDEC MS-001 Variation AB.

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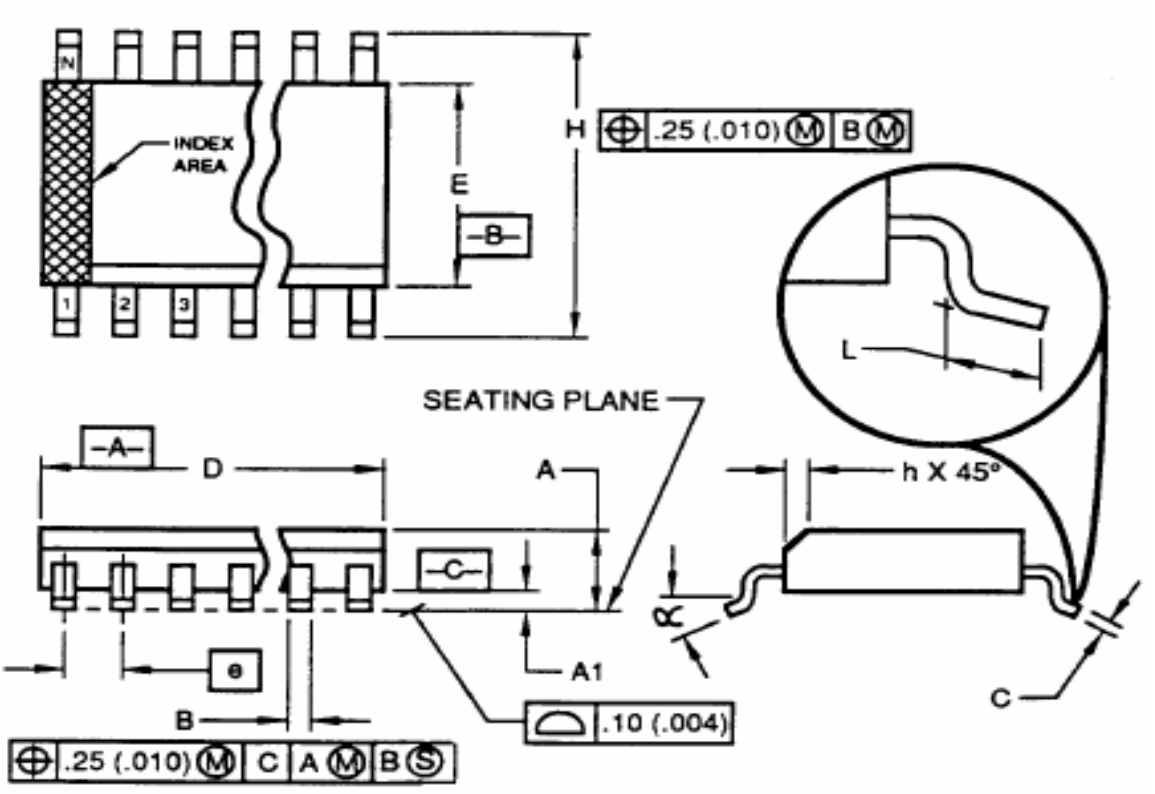
16 PINS, SOP, 300MIL



Symbol	Min.	Nom.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	10.10		10.50
E	7.40		7.60
e		1.27 bsc.	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
α	0°		8°

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5-1982.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold Flash protrusion or gate burrs shall not exceed 0.15mm (0.006 in) per side.
3. Dimension “E” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. “L” is the length of the terminal for soldering to a substrate.
6. “N” is the number of terminal positions. (N=16)
7. The lead width “B” as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in).
8. Controlling dimension: MILLIMETER.
9. Refer to JEDEC MS-013 Variation AA

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