Single-PLL General Purpose EPROM Programmable Clock Generator

Features

- Single phase locked loop (PLL) architecture
- EPROM programmability
- Factory-programmable (CY2907, CY2907I) or field-programmable (CY2907F, CY2907FI) device options
- Up to two configurable outputs
- Low skew, low jitter, high accuracy outputs
- Power management (power down, OE)
- Frequency select option
- Configurable 5V or 3.3V operation
- 8-pin or 14-pin SOIC packages

Benefits

- Generates a custom frequency from an external source
- Easy customization and fast turnaround
- Programming support available for all opportunities
- Provides clocking requirements from a single device
- Meets critical industry-standard timing requirements
- Supports low-power applications
- Up to 16 user-selectable frequencies
- Supports industry-standard design platforms
- Industry-standard packaging saves on board space

Selector Guide

Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY2907	2	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–130 MHz (5V) 500 kHz–100 MHz (3.3V)	Factory Programmable Commercial Temperature
CY2907I	2	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–100 MHz (5V) 500 kHz–80 MHz (3.3V)	Factory Programmable Industrial Temperature
CY2907F8 CY2907F14	2	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–100 MHz (5V) 500 kHz–80 MHz (3.3V)	*Field Programmable* Commercial Temperature
CY2907F8I CY2907F14I	2	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–90 MHz (5V) 500 kHz–66.66 MHz (3.3V)	*Field Programmable* Industrial Temperature

Logic Block Diagram

Pin Configurations

Top View

14-Pin SOIC

8-Pin SOIC

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[+] Feedback
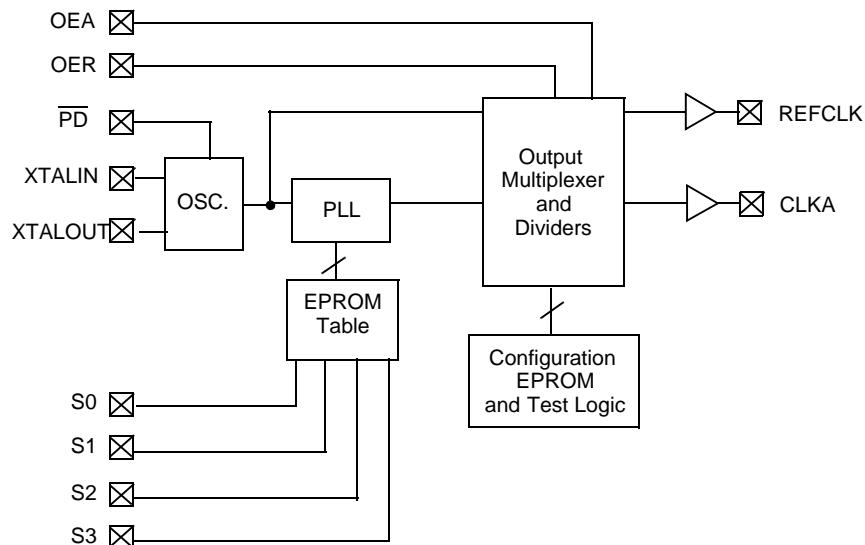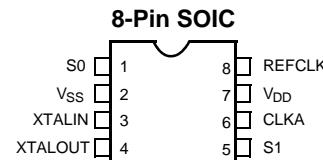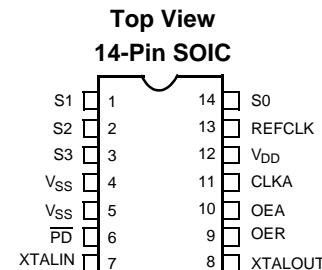
Pin Summary

Name	Pin Number		Description
	14-Pin SOIC	8-Pin SOIC	
S1	1	5	Frequency Select (CLKA) (Internal pull up resistor to V_{DD})
S2	2	NA	Frequency Select (CLKA) (Internal pull up resistor to V_{DD})
S3	3	NA	Frequency Select (CLKA) (Internal pull up resistor to V_{DD})
V_{SS}	4	2	Ground
V_{SS}	5	NA	Ground
PD	6	NA	Power Down (Active LOW) (Internal pull up resistor to V_{DD})
XTALIN[1]	7	3	Reference Crystal Input
XTALOUT[1, 2]	8	4	Reference Crystal Feedback
OER	9	NA	REFCLK Output Enable (Active HIGH) (Internal pull up resistor to V_{DD})
OEA	10	NA	CLKA Output Enable (Active HIGH) (Internal pull up resistor to V_{DD})
CLKA	11	6	Clock Output
V_{DD}	12	7	Voltage Supply
REFCLK	13	8	Reference Clock Output (Default, can be driven by PLL if desired)
S0	14	1	Frequency Select (CLKA) (Internal pull up resistor to V_{DD})

Functional Description

The CY2907 is a general purpose clock generator designed for use in a wide variety of applications—from graphics to PC peripherals to disk drives. It generates selectable system clock frequencies from a single reference input (crystal or reference clock). The CY2907 is configured with an EPROM array, similar to the other devices in the Cypress EPROM Programmable Clock family, making it easy to customize for any application. Furthermore, the CY2907 is compatible with all industry-standard 9107 and 9108 clock synthesizers.

Device Programming

Two versions of the CY2907 are available - Field Programmable and Factory Programmable. Field programmable devices must be programmed before being installed in an application. They are one-time-programmable (OTP). Customers can program small quantities in-house using the Cypress CY3670 programmer. Production quantities are available through Cypress's value-added distribution partners, or by using third party programmers from BP Microsystems, Hi-Lo Systems, and others.

For high-volume orders, devices can be factory programmed by Cypress. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. Once the request has been processed, you will receive a new part number, samples, and a data sheet with the programmed values. This part number will be used for additional sample requests and production orders.

CyberClocks™ Software

CyberClocks is an easy-to-use software application that allows the user to configure any one of the EPROM Programmable Clocks offered by Cypress. You may specify the input frequency, PLL and output frequencies, and different functional options. Note the output frequency ranges in this data sheet when specifying them in CyberClocks to make sure that you stay within the limits. Once a configuration is established, you can print the configuration and save programming files in ENT and JED formats.

CyberClocks runs on PCs running the Windows™ operating system, and is available for free download on the Cypress Semiconductor website at www.cypress.com.

Within the CyberClocks application, the CY2907 is found in the CyClocks™ section. Note that the stand-alone CyberClocks software should not be confused with the CyberClocks Online software, which is a web-based application that is used to configure other programmable clock devices.

Cypress CY3670 Programming Kit

Cypress's CY3670 is a portable programmer that connects to a PC serial port and allow users of CyClocks software to quickly and easily program any of the CY2291F, CY2292F, CY2071AF, and CY2907F devices. An adapter is also required and is ordered separately. The CY3097 is the adapter for the CY2907F8. For the CY2907F14, order adapter CY3098.

Notes
1. For best accuracy, use a parallel resonant crystal, $C_{LOAD} \approx 17$ pF.
2. Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to crystal).

Maximum Ratings

Exceeding maximum ratings may shorten the battery life of the device. User guidelines are not tested.

Supply Voltage ....–0.5 to +7.0V

Input Voltage ....–0.5V to V_{DD}+0.5V

Storage Temperature (Non-Condensing).... –65°C to +150°C

Max. Soldering Temperature (10 sec) .... +260°C

Junction Temperature .... +150°C

Static Discharge Voltage... >2000V
(per MIL-STD-883, Method 3015)

Operating Conditions[3]

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage, 5V Operation	4.5	5.5	V
	Supply Voltage, 3.3V Operation	3.0	3.6	V
T_A	Commercial Operating Temperature, Ambient	0	70	°C
	Industrial Operating Temperature, Ambient	–40	85	°C
C_L	Max. Capacitive Load		15	pF
f_{REF}	External Reference Crystal	10.0	25.0	MHz
	External Reference Clock[4, 5]	1.0	30.0	MHz

Electrical Characteristics at 5.0V Commercial V_{DD} = 4.5V to 5.5V, T_A = 0°C to +70°C

Parameter	Description	Test Conditions			Min	Max	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}[4]	High-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OH} = –30 mA	CLKA	2.4		V
V_{OL}[4]	Low-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OL} = 10 mA	CLKA		0.4	V
I_{OH}[4]	Output High Current	V_{OH} = 2.0V				–35	mA
I_{OL}[4]	Output Low Current	V_{OL} = 0.8V			22		mA
I_{IH}	Input High Current	V_{IH} = V_{DD}			–2	2	μA
I_{IL}	Input Low Current	V_{IL} = 0V				20	μA
I_{DD}[5]	Power Supply Current	$\overline{PD}$ HIGH, CLKA = 50 MHz				42	mA
I_{DD}	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs LOW				100	μA
I_{DD}	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs HIGH				40	μA
R_{PU}[4]	Pull Up Resistor	V_{IN} = V_{DD} – 1.0 V				700	kΩ

Notes
3. Electrical parameters are guaranteed with these operating conditions.
4. Guaranteed by design, not 100% tested in production.
5. Load = max. typical configuration, f_{REF} = 14.318 MHz. Specific configurations may vary. A close approximation of I_{DD} can be derived by the following formula:
I_{DD} (mA) = V_{DD} * (6.25 + (0.055*F_{REF}) + (0.0017*C_{LOAD}*(F_{CLKA} + $\overline{REFCLK}$))). C_{LOAD} is specified in pF and F is specified in MHz.

[+] Feedback

Electrical Characteristics at 3.3V Commercial V_{DD} = 3.0V to 3.6V, T_A = 0°C to +70°C

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs	$0.7*V_{DD}$		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs		$0.2*V_{DD}$	V
V_{OH}[4]	High-level Output Voltage	CLKA, I_{OH} = –5 mA	$0.85*V_{DD}$		V
V_{OL}[4]	Low-level Output Voltage	CLKA, I_{OL} = 6 mA		$0.1*V_{DD}$	V
I_{OH}[4]	Output High Current	V_{OH} = $0.7*V_{DD}$		–10	mA
I_{OL}[4]	Output Low Current	V_{OL} = $0.2*V_{DD}$	15		mA
I_{IH}	Input High Current	V_{IH} = V_{DD}	–2	2	μA
I_{IL}	Input Low Current	V_{IL} = 0V		10	μA
I_{DD}[5]	Power Supply Current	$\overline{PD}$ HIGH, CLKA = 50 MHz		40	mA
I_{DD}	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs LOW		40	μA
I_{DD}	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs HIGH		12	μA
R_{PU}[4]	Pull Up Resistor	V_{IN} = V_{DD} – 0.5V		900	kΩ

6.

Electrical Characteristics at 5.0V Industrial V_{DD} = 4.5V to 5.5V, T_A = –40°C to +85°C

Parameter	Description	Test Conditions			Min	Max	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}[4]	High-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OH} = –30 mA	CLKA	2.4		V
V_{OL}[4]	Low-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OL} = 10 mA	CLKA		0.4	V
I_{OH}[4]	Output High Current	V_{OH} = 2.0V				–45	mA
I_{OL}[4]	Output Low Current	V_{OL} = 0.8V			20		mA
I_{IH}	Input High Current	V_{IH} = V_{DD}			–2	2	μA
I_{IL}	Input Low Current	V_{IL} = 0V				20	μA
I_{DD}[5]	Power Supply Current	$\overline{PD}$ HIGH, CLKA = 50 MHz				54	mA
I_{DD}	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs LOW				110	μA
I_{DD}	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs HIGH				45	μA
R_{PU}[4]	Pull Up Resistor	V_{IN} = V_{DD} – 1.0 V				700	kΩ

Electrical Characteristics at 3.3V Industrial V_{DD} = 3.0V to 3.6V, T_A = −40°C to +85°C

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs	$0.7*V_{DD}$		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs		$0.2*V_{DD}$	V
V_{OH}[4]	High-level Output Voltage	CLKA, I_{OH} = −5 mA	$0.85*V_{DD}$		V
V_{OL}[4]	Low-level Output Voltage	CLKA, I_{OL} = 6 mA		$0.1*V_{DD}$	V
I_{OH}[4]	Output High Current	V_{OH} = $0.7*V_{DD}$		−12	mA
I_{OL}[4]	Output Low Current	V_{OL} = $0.2*V_{DD}$	14		mA
I_{IH}	Input High Current	V_{IH} = V_{DD}	−2	2	μA
I_{IL}	Input Low Current	V_{IL} = 0V		10	μA
I_{DD}[5]	Power Supply Current	$\overline{PD}$ HIGH, CLKA = 50 MHz		50	mA
I_{DD}	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs LOW		50	μA
I_{DD}	Power Supply Current	$\overline{PD}$ LOW, Logic Inputs HIGH		15	μA
R_{PU}[4]	Pull Up resistor	V_{IN} = V_{DD} − 0.5V		900	kΩ

Switching Characteristics at 5.0V Commercial[4]

Parameter	Output[7]	Description	Test Conditions	Min	Max	Unit
t_R	CLKA	Output Rise Time 0.8V to 2.0V	15-pF Load		1.40	ns
t_F	CLKA	Output Fall Time 2.0V to 0.8V	15-pF Load		1.00	ns
t_R	CLKA	Output Rise Time 20% to 80%	15-pF Load		3.5	ns
t_F	CLKA	Output Fall Time 80% to 20%	15-pF Load		2.5	ns
t_D	CLKA	Duty Cycle	15-pF Load at 1.4V	45.0	55.0	%
F_I	XTALIN	Input Frequency	Crystal Oscillator	10	25	MHz
F_I	XTALIN	Input Frequency	External Input Clock[8]	1	30	MHz
F_O	CLKA	Output Frequency	CY2907, 15-pF Load	0.5	130.0	MHz
			CY2907F, 15-pF Load	0.5	100.0	MHz
t_{JIS}	CLKA	Jitter (One Sigma)	20 MHz to 130 MHz		150	ps
t_{JIS}	CLKA	Jitter (One Sigma)	14 MHz to 20 MHz		200	ps
t_{JIS}	CLKA	Jitter (One Sigma)	Less than 14 MHz		1	%
t_{JAB}	CLKA	Jitter (Absolute)	20 MHz to 130 MHz	−250	+ 250	ps
t_{JAB}	CLKA	Jitter (Absolute)	14 MHz to 20 MHz	−500	+ 500	ps
t_{JAB}	CLKA	Jitter (Absolute)	Less than 14 MHz		3	%
t_{PU}		Power Up Time			18	ms
t_{FT}	CLKA	Transition Time	8 MHz to 66.6 MHz		13	ms

Switching Characteristics at 3.3V Commercial[4]

Parameter	Output[7]	Description	Test Conditions	Min	Max	Unit
t_R	CLKA	Output Rise Time 20% to 80%	15-pF Load		3.5	ns
t_F	CLKA	Output Fall Time 80% to 20%	15-pF Load		2.5	ns
t_D	CLKA	Duty Cycle	15-pF Load at 1.4V	40.0	53.0	%
F_I	XTALIN	Input Frequency	Crystal Oscillator	10	25	MHz
F_I	XTALIN	Input Frequency	External Input Clock[8]	1	30	MHz
F_O	CLKA	Output Frequency	CY2907, 15-pF Load	0.5	100.0	MHz
			CY2907F, 15-pF Load	0.5	80.0	MHz
t_{JIS}	CLKA	Jitter (One Sigma)	25 MHz to 100 MHz		150	ps
t_{JIS}	CLKA	Jitter (One Sigma)	14 MHz to 25 MHz		200	ps
t_{JIS}	CLKA	Jitter (One Sigma)	Less than 14 MHz		1	%
t_{JAB}	CLKA	Jitter (Absolute)	25 MHz to 120 MHz	−250	+250	ps
t_{JAB}	CLKA	Jitter (Absolute)	14 MHz to 25 MHz	−500	+500	ps
t_{JAB}	CLKA	Jitter (Absolute)	Less than 14 MHz		3	%
t_{PU}		Power Up Time			18	ms
t_{FT}	CLKA	Transition Time	8 MHz to 66.6 MHz		13	ms

Switching Characteristics at 5.0V Industrial

Parameter	Output[7]	Description	Test Conditions	Min	Max	Unit
t_R	CLKA	Output Rise Time 0.8V to 2.0V	15-pF Load		1.40	ns
t_F	CLKA	Output Fall Time 2.0V to 0.8V	15-pF Load		1.00	ns
t_R	CLKA	Output Rise Time 20% to 80%	15-pF Load		3.5	ns
t_F	CLKA	Output Fall Time 80% to 20%	15-pF Load		2.5	ns
t_D	CLKA	Duty Cycle	15-pF Load at 1.4V	45.0	55.0	%
F_I	XTALIN	Input Frequency	Crystal Oscillator	10	25	MHz
F_I	XTALIN	Input Frequency	External Input Clock[8]	1	30	MHz
F_O	CLKA	Output Frequency	CY2907, 15-pF Load	0.5	100.0	MHz
			CY2907F, 15-pF Load	0.5	90	MHz
t_{JIS}	CLKA	Jitter (One Sigma)	20 MHz to 130 MHz		150	ps
t_{JIS}	CLKA	Jitter (One Sigma)	14 MHz to 20 MHz		200	ps
t_{JIS}	CLKA	Jitter (One Sigma)	Less than 14 MHz		1	%
t_{JAB}	CLKA	Jitter (Absolute)	20 MHz to 130 MHz	−250	+ 250	ps
t_{JAB}	CLKA	Jitter (Absolute)	14 MHz to 20 MHz	−500	+ 500	ps
t_{JAB}	CLKA	Jitter (Absolute)	Less than 14 MHz		3	%
t_{PU}		Power Up Time			18	ms
t_{FT}	CLKA	Transition Time	8 MHz to 66.6 MHz		13	ms

Notes
7. REFCLK output can also be configured to be driven by the PLL. In that case these characteristics are also valid.
8. Refer to the application note *Crystal Oscillator Topics* when using an external reference clock as an input frequency source.

Switching Characteristics at 3.3V Industrial

Parameter	Output[7]	Description	Test Conditions	Min	Max	Unit
t_R	CLKA	Output Rise Time 20% to 80%	15-pF Load		3.5	ns
t_F	CLKA	Output Fall Time 80% to 20%	15-pF Load		2.5	ns
t_D	CLKA	Duty Cycle	15-pF Load at 1.4V	40.0	53.0	%
F_I	XTALIN	Input Frequency	Crystal Oscillator	10	25	MHz
F_I	XTALIN	Input Frequency	External Input Clock[8]	1	30	MHz
F_O	CLKA	Output Frequency	CY2907I, 15-pF Load	0.5	80.0	MHz
			CY2907FI, 15-pF Load	0.5	66.6	MHz
t_{JIS}	CLKA	Jitter (One Sigma)	25 MHz to 100 MHz		150	ps
t_{JIS}	CLKA	Jitter (One Sigma)	14 MHz to 25 MHz		200	ps
t_{JIS}	CLKA	Jitter (One Sigma)	Less than 14 MHz		1	%
t_{JAB}	CLKA	Jitter (Absolute)	25 MHz to 120 MHz	−250	+250	ps
t_{JAB}	CLKA	Jitter (Absolute)	14 MHz to 25 MHz	−500	+500	ps
t_{JAB}	CLKA	Jitter (Absolute)	Less than 14 MHz		3	%
t_{PU}		Power Up Time			18	ms
t_{FT}	CLKA	Transition Time	8 MHz to 66.6 MHz		13	ms

Switching Waveforms

Figure 1. Frequency Select Change (Transition Time)
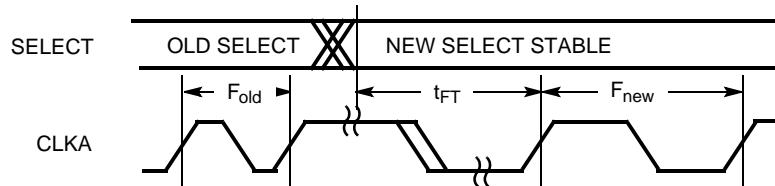
Figure 2. Duty Cycle Timing

$t_D = t_2 \div t_1$
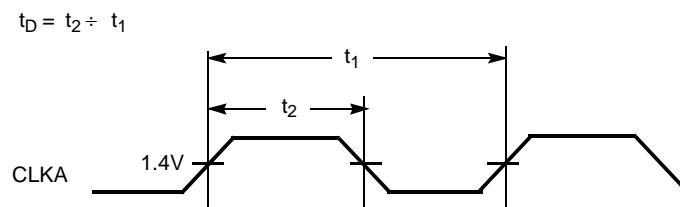
Figure 3. All Outputs Rise/Fall Time
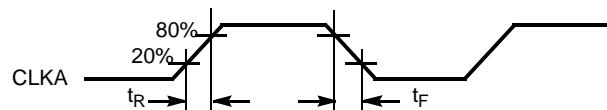
Test Circuit

Figure 4. Test Circuit
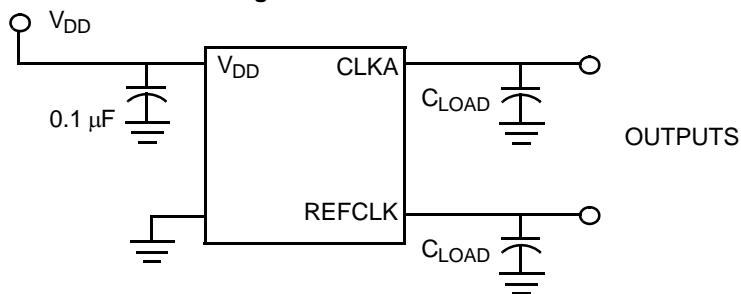
Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Type	Operating Range
CY2907SC-xxx	8-pin or 14-pin SOIC	5.0V, Commercial, Factory Programmable
CY2907SC-xxxT	8-pin or 14-pin SOIC -Tape and Reel	5.0V, Commercial, Factory Programmable
CY2907SL-xxx	8-pin or 14-pin SOIC	3.3V, Commercial, Factory Programmable
CY2907SL-xxxT	8-pin or 14-pin SOIC - Tape and Reel	3.3V, Commercial, Factory Programmable
CY2907SI-xxx	8-pin or 14-pin SOIC	5.0V/3.3V, Industrial, Factory Programmable
CY2907SI-xxxT	8-pin or 14-pin SOIC - Tape and Reel	5.0V/3.3V, Industrial, Factory Programmable
CY2907F8	8-pin SOIC	5.0V/3.3V, Commercial, Field Programmable
CY2907F8T	8-pin SOIC - Tape and Reel	5.0V/3.3V, Commercial, Field Programmable
CY2907F8I	8-pin SOIC	5.0V/3.3V, Industrial, Field Programmable
CY2907F8IT	8-pin SOIC - Tape and Reel	5.0V/3.3V, Industrial, Field Programmable
CY2907F14	14-pin SOIC	5.0V/3.3V, Commercial, Field Programmable
CY2907F14T	14-pin SOIC - Tape and Reel	5.0V/3.3V, Commercial, Field Programmable
CY2907F14I	14-pin SOIC	5.0V/3.3V, Industrial, Field Programmable
CY2907F14IT	14-pin SOIC - Tape and Reel	5.0V/3.3V, Industrial, Field Programmable
CY3670	Cypress FTG Programmer	Custom Programming for Field Programmable Clocks
Pb-free		
CY2907FX8	8-pin SOIC	5.0V/3.3V, Commercial, Field Programmable
CY2907FX8T	8-pin SOIC - Tape and Reel	5.0V/3.3V, Commercial, Field Programmable
CY2907FX14	14-pin SOIC	5.0V/3.3V, Commercial, Field Programmable
CY2907FX14T	14-pin SOIC - Tape and Reel	5.0V/3.3V, Commercial, Field Programmable

Package Characteristics

Package	θ_{JA} (C/W)	θ_{JC} (C/W)	Transistor Count
8-pin SOIC	170	35	5436
14-pin SOIC	140	31	5436

Package Diagrams

Figure 5. 8-Lead (150-Mil) SOIC S8

1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.

2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME

3. REFERENCE JEDEC MS-012

4. PACKAGE WEIGHT 0.07gms

PART #
S08.15 STANDARD PKG.
SZ08.15 LEAD FREE PKG.

51-85066-*C

[+] Feedback
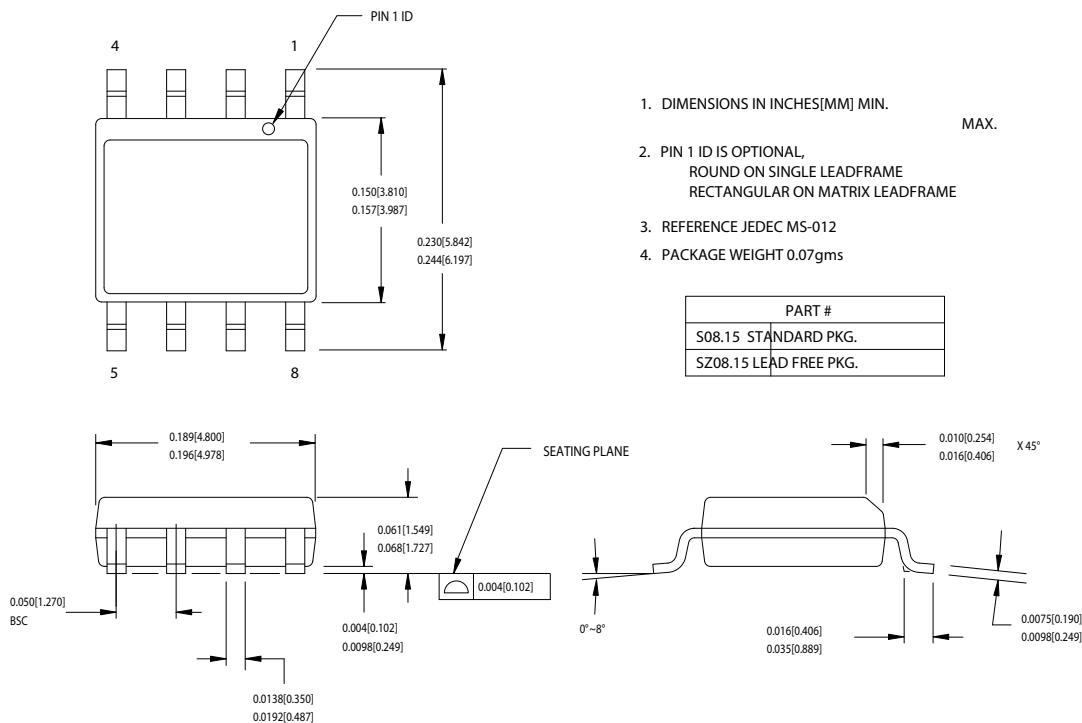
Package Diagrams (continued)

Figure 6. 14-Lead (150-Mil) SOIC S14

PIN 1 ID

7 1

0.150[3.810]
0.157[3.987]

0.230[5.842]
0.244[6.197]

8 14

DIMENSIONS IN INCHES[MM] MIN.

MAX.

REFERENCE JEDEC MS-012

PART #
S14.15 STANDARD PKG.
SZ14.15 LEAD FREE PKG.

0.337[8.559]
0.344[8.7376]

SEATING PLANE

0.010[0.254]
0.016[0.406]

X 45°

0.061[1.549]
0.068[1.727]

0.050[1.270]
BSC

0.004[0.102]

0.0075[0.190]
0.0098[0.249]

0.0138[0.350]
0.0192[0.487]

0.004[0.102]
0.0098[0.249]

0°~8°

0.016[0.406]
0.035[0.889]

51-85067-*B

Document #: 38-07137 Rev. *A

[+] Feedback

Document History Page

				Document Title: CY2907 Single-PLL General Purpose EPROM Programmable Clock Generator Document Number: 38-07137
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110246	12/18/01	SZV	Change from Spec number: 38-00505 to 38-07137
*A	1088524	See ECN	KVM/ KKVTMP	Added Pb-free for CY2907F8 and CY2907F14 field programmable devices Updated and added to text on page 2 Applied new template

[+] Feedback