NEC

MOS INTEGRATED CIRCUIT

μPD168103

5-CHANNEL OPERATIONAL AMPLIFIER, IRIS DRIVER, AND 4-CHANNEL H-BRIDGE DRIVER

DESCRIPTION

The μPD168103 is the motor driver IC with IRIS control circuit, operational amplifier and 4-ch H-bridge output. Smooth operation is possible for IRIS control with linear method.

The package is 48-pin thin type QFN and then it helps reduce the mounting area and height.

The μPD168103 is suitable for the lens drive of a camcorder, DSC, etc.

FEATURES

- 5-ch H-bridge circuits employing power MOS FET
- Low-voltage driving
  LV_{DD} = 2.7 to 3.6 V, AV_{DD} = 4.5 to 5.5 V, V_{M12} = V_{M34} = $V_{SHUTTER}$ = V_{IRIS} = 2.7 to 5.5 V
- Output on-state resistance: 2.0 Ω TYP., 3.0 Ω MAX. (4-ch H-bridge block, sum of top and bottom stage, V_M = 5 V)
- PWM output (ch1 to ch4)
- Output current
  DC current: ±0.3 A/ch (when each channel is used independently)
  Peak current: ±0.7 A/ch (when each channel is used independently)
- 3-ch general-purpose operational amplifier
  Input offset voltage: ±5 mV
  Input voltage range: 0 to AV_{DD} – 1.5 V
  Output voltage range: 0.2 to AV_{DD} – 0.2 V
- 1-ch current sink amplifier
  Output current: 5 mA
- 1-ch 1/2V_{DD} output amplifier
- IRIS driver block supporting linear driving
- Pre-driver amplifier of the IRIS driver block
- Undervoltage lockout circuit
  Output circuit and amplifier stop at LV_{DD} = 1.7 V TYP. or less.
- Overheat protection circuit
  Operates at 150°C or more and shuts down the output circuit.
- Mounted on 48-pin plastic WQFN (7 x 7)

APPLICATIONS

Lens motor driving for DVC and DSC, etc.

ORDERING INFORMATION

Part Number	Package	Marking	Packing Type
μPD168103K9-5B4-A [Note]	48-pin plastic WQFN (7 x 7)	D168103	• Tray stuffing • Dry pack

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

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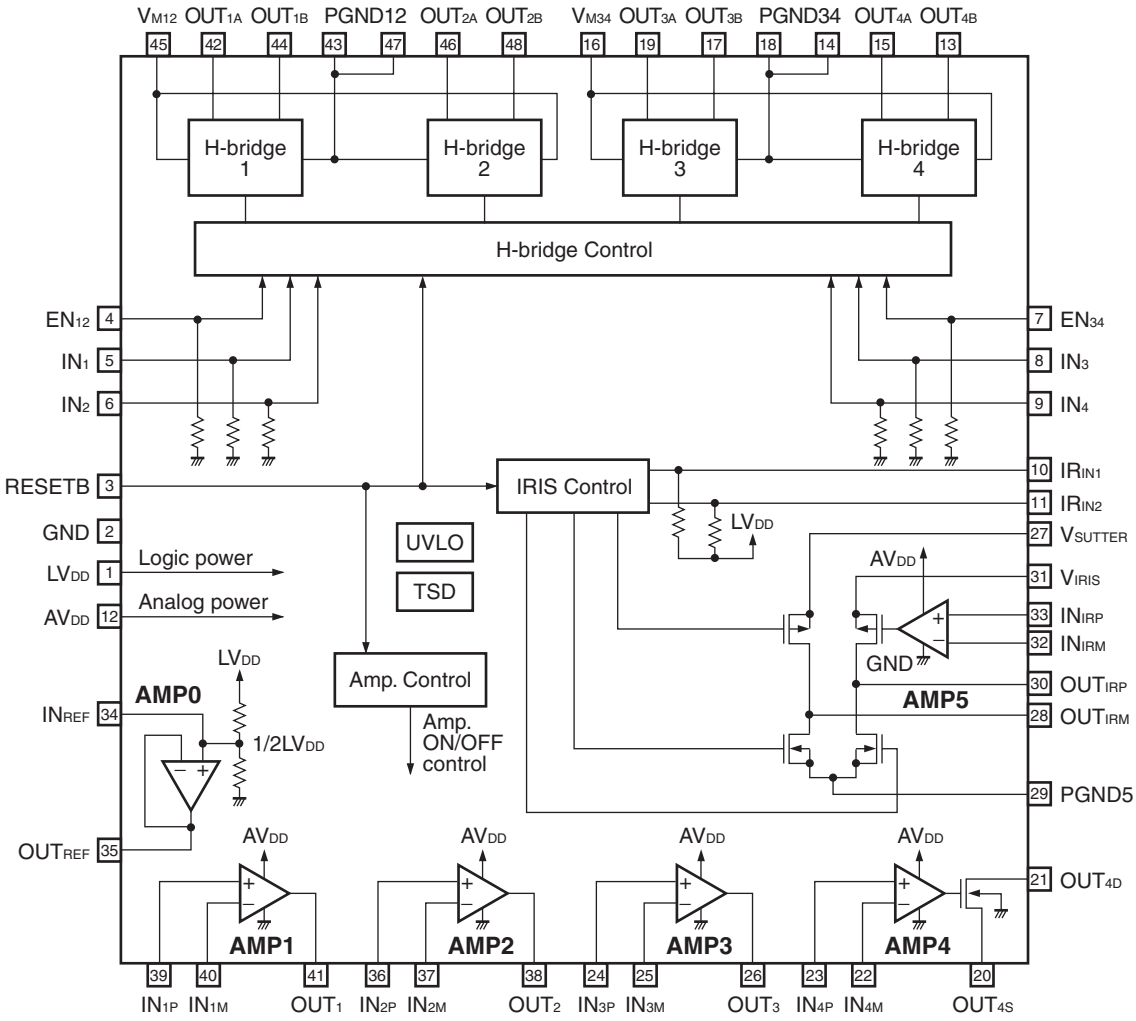
1. BLOCK DIAGRAM



Cautions 1. P in pin name means plus, and M in pin name means minus.

2. A pull-down resistor (50 to 200 kΩ) is connected to the logic input pins (EN_{12}, EN_{34}, IN_1, IN_2, IN_3, and IN_4). A pull-up resistor (50 to 200 kΩ) is connected to the IR_{IN1} and IR_{IN2} pins.

2. PIN FUNCTIONS

(1/2)

Pin No.	Pin Name	I/O	Function
1	LV_{DD}	–	Logic power supply voltage pin
2	GND	–	Logic and analog GND pin
3	RESETB	Input	Reset input pin
4	EN_{12}	Input	ch1 and ch2 output control input pin
5	IN_1	Input	ch1 input pin
6	IN_2	Input	ch2 input pin
7	EN_{34}	Input	ch3 and ch4 output control input pin
8	IN_3	Input	ch3 input pin
9	IN_4	Input	ch4 input pin
10	IR_{IN1}	Input	IRIS control logic input pin 1
11	IR_{IN2}	Input	IRIS control logic input pin 2
12	AV_{DD}	–	Analog power supply voltage pin
13	OUT_{4B}	Output	ch4 output pin B
14	PGND34	–	ch3 and ch4 GND pin
15	OUT_{4A}	Output	ch4 output pin A
16	VM_{34}	–	ch3 and ch4 power supply voltage pin
17	OUT_{3B}	Output	ch3 output pin B
18	PGND34	–	ch3 and ch4 GND pin
19	OUT_{3A}	Output	ch3 output pin A
20	OUT_{4S}	Output	Amplifier 4 (AMP4) source output pin (source)
21	OUT_{4D}	Output	Amplifier 4 (AMP4) drain output pin (sink)
22	IN_{4M}	Input	Amplifier 4 (AMP4) minus input pin
23	IN_{4P}	Input	Amplifier 4 (AMP4) plus input pin
24	IN_{3P}	Input	Amplifier 3 (AMP3) plus input pin
25	IN_{3M}	Input	Amplifier 3 (AMP3) minus input pin
26	OUT_3	Output	Amplifier 3 (AMP3) output pin
27	$V_{SHUTTER}$	–	Shutter (ON/OFF) power supply voltage pin
28	OUT_{IRM}	Output	IRIS minus output pin
29	PGND5	–	IRIS and shutter GND pin
30	OUT_{IRP}	Output	IRIS plus output pin
31	V_{IRIS}	–	IRIS (linear) power supply voltage pin
32	IN_{IRM}	Input	IRIS linear control (AMP5) minus input pin
33	IN_{IRP}	Input	IRIS linear control (AMP5) plus input pin
34	IN_{REF}	Input	$1/2AV_{DD}$ amplifier (AMP0) input pin (for capacitor connection)

(2/2)

Pin No.	Pin Name	I/O	Function
35	OUT_{REF}	Output	1/2AV_{DD} amplifier (AMP0) output pin
36	IN_{2P}	Input	Amplifier 2 (AMP2) plus input pin
37	IN_{2M}	Input	Amplifier 2 (AMP2) minus input pin
38	OUT_2	Output	Amplifier 2 (AMP2) output pin
39	IN_{1P}	Input	Amplifier 1 (AMP1) plus input pin
40	IN_{1M}	Input	Amplifier 1 (AMP1) minus input pin
41	OUT_1	Output	Amplifier 1 (AMP1) output pin
42	OUT_{1A}	Output	ch1 output pin A
43	PGND12	–	ch1 and ch2 GND pin
44	OUT_{1B}	Output	ch1 output pin B
45	V_{M12}	–	ch1 and ch2 power supply voltage pin
46	OUT_{2A}	Output	ch2 output pin A
47	PGND12	–	ch1 and ch2 GND pin
48	OUT_{2B}	Output	ch2 output pin B

3. FUNCTION OPERATION TABLE

3.1 Reset Function

The internal circuit is shut off and the circuit current is kept to 1 μA MAX. when the RESETB pin is made L (reset status). In this status, the output pin goes into a Hi-Z (High impedance) state. Set the RESETB pin H for normal usage.

Remark H: High level, L: Low level

3.2 Stepping Motor Driving Block

Table 3–1. I/O Truth Table of the Stepping Motor Driving Block

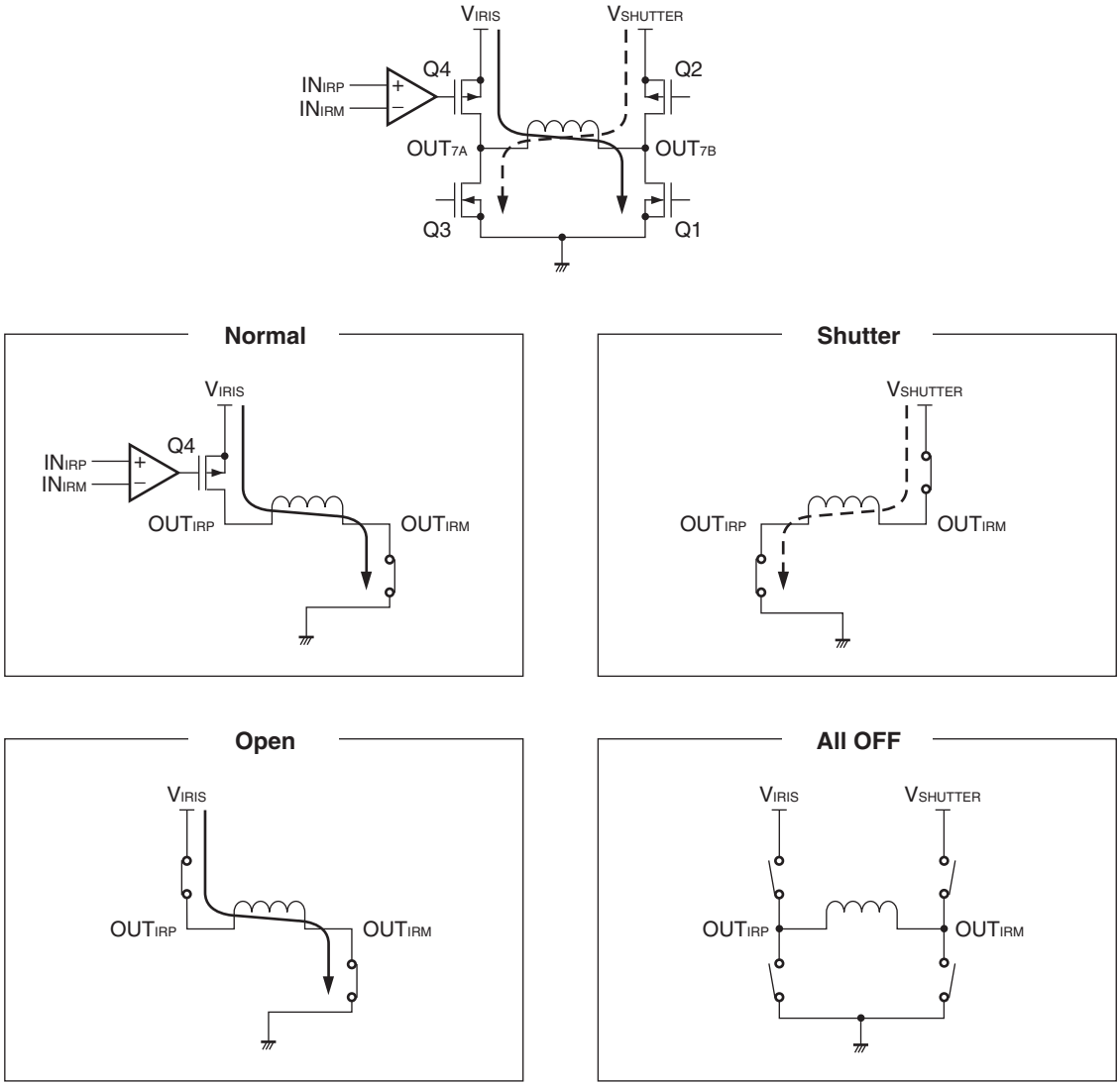
EN_{12}, EN_{34}	IN_1, IN_2, IN_3, IN_4	OUT_{1A}, OUT_{2A}, OUT_{3A}, OUT_{4A}	OUT_{1B}, OUT_{2B}, OUT_{3B}, OUT_{4B}
H	L	H	L
	H	L	H
L	L	Hi-Z	Hi-Z
	H	Hi-Z	Hi-Z

3.3 IRIS Motor Driving Block

Table 3–2. I/O Truth Table of the IRIS Driving Block

IR_{IN1}	IR_{IN2}	Operation Mode	Output State of H-bridge				OUT_{IRP}	OUT_{IRM}
			Q1	Q2	Q3	Q4		
L	L	Normal operation (Amp. control)	ON	OFF	OFF	ON (Linear)	Linear	Linear
L	H	Shutter	OFF	ON	ON	OFF	L	H
H	L	IRIS open	ON	OFF	OFF	ON	H	L
H	H	Output all OFF	OFF	OFF	OFF	OFF	Hi-Z	Hi-Z

Figure 3–1. Description of the Operation Figure of the IRIS Motor Driving Block



4. FUNCTIONAL DEPLOYMENT

4.1 Undervoltage Lockout (UVLO) Circuit

This function is to forcibly stop the operation of the μPD168103 to prevent malfunctioning if LV_{DD} drops.

When UVLO operates, the driver output and amplifier circuit are the OFF status.

The UVLO circuit detects a voltage drop if LV_{DD} drops to 1.7 V TYP. in the non-reset status (RESETB = H). In the reset status (RESETB = L), it detects a voltage drop if LV_{DD} drops to 0.6 V TYP. This circuit may not operate if the LV_{DD} voltage abruptly drops for just a few μs.

4.2 Overheat Protection (TSD) Circuit

This function is to forcibly stop the operation of the driver output to protect it from destruction due to overheating if the chip temperature of the μPD168103 rises.

The overheat protection circuit operates when the chip temperature rises to 150°C or more. When overheat is detected, the driver output is stopped.

When RESETB = L (the reset status) or when UVLO is detected, the overheat protection circuit does not operate.

4.3 Power Up Sequence

The μPD168103 has a circuit that prevents current from flowing into the V_M, $V_{SHUTTER}$ and V_{IRIS} pins (from the next, these are written as the motor power supply pins) when LV_{DD} = 0 V or AV_{DD} = 0 V. Therefore, the current that flows into the motor power supply pins are cut off when LV_{DD} = 0 V.

Because the LV_{DD} pin voltage, the AV_{DD} pin voltage and the motor power supply pins voltage are monitored, a current of 1 μA TYP. flows into each one of the motor power supply pins when LV_{DD} is applied.

5. NOTE ON CORRECT USE

5.1 Pin Processing of Unused Circuit

The input/output pins of an unused circuit must be processed as specified below.

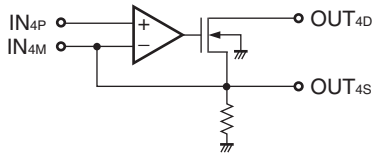
A pull-down or pull-up resistor is connected inside to the logic input pins. Connect the input pins to the GND or LV_{DD} (IN_{IR1} and IN_{IR2}) potential when they are not used.

A pull-down resistor is not connected to the RESETB pin. Be sure to fix the RESETB pin to the LV_{DD} or GND potential when it is used.

5.2 OUT_{4S} pin

Keep the voltage in the OUT_{4S} pin to 2 V or less.

If an application circuit like the one shown below is used, the input voltage range of the amplifier is also 2 V or less.



6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, glass epoxy board of 100 mm x 100 mm x 1 mm with copper foil area of 15%)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	LV_{DD}	Control block	−0.5 to +6.0	V
	AV_{DD}	Analog block	−0.5 to +6.0	V
	V_{M12}, V_{M34}	Stepping motor block	−0.5 to +6.0	V
	$V_{SHUTTER}$, V_{IRIS}	IRIS block	−0.5 to +6.0	V
Input voltage Note1	V_{IN}		−0.5 to LV_{DD} + 0.5	V
Output pin voltage 1	V_{OUT1}	Motor block	6.2	V
Output pin voltage 2	V_{OUT2}	Amplifier block	−0.5 to AV_{DD} + 0.5	V
DC output current	$I_{D1(DC)}$	DC (stepping motor)	±0.3	A/ch
	$I_{D2(DC)}$	DC (IRIS)	±0.2	A/ch
Instantaneous output current	$I_{D(pulse)}$	PW < 10 ms, Duty Cycle ≤ 20%	±0.7	A/ch
Power consumption	P_T		1.0	W
Peak junction temperature Note2	$T_{ch(MAX)}$		150	°C
Storage temperature	T_{stg}		−55 to +150	°C

Notes 1. Keep V_{IN} to less than 6 V.

2. The overheat protection circuit operates at T_{ch} > 150°C. When overheat is detected, all the circuits are stopped. The overheat protection circuit does not operate at reset or on detection of ULVO.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = 25°C, glass epoxy board of 100 mm x 100 mm x 1 mm with copper foil area of 15%)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage	LV_{DD}	Control block	2.7		3.6	V
	AV_{DD}	Analog block	4.5		5.5	V
	V_{M12}, V_{M34}	Stepping motor block	2.7		5.5	V
	$V_{SHUTTER}$, V_{IRIS}	IRIS block	2.7		5.5	V
Input voltage	V_{IN}		0		V_{DD}	V
DC output current	$I_{D1(DC)}$	DC (stepping motor, when 2 chs are driven at same time)	−0.2		+0.2	A/ch
	$I_{D2(DC)}$	DC (IRIS), maximum current when the shutter operates	−0.1		+0.1	A/ch
Amplifier output current	I_{OUT_AMP1}	AMP1 to AMP3	−5		+5	mA/ch
Amplifier output sink current	I_{OUT_AMP2}	AMP4	0		+5	mA
Logic input frequency	f_{IN}				100	kHz
Operating temperature range	T_A		−10		70	°C

Caution Design each output current so that the junction temperature does not exceed 150ºC.

Electrical Characteristics (Unless otherwise specified, T_A = 25°C, LV_{DD} = 3.0 V, AV_{DD} = 5.0 V, V_M = $V_{SHUTTER}$ = V_{IRIS} = 5.0 V)

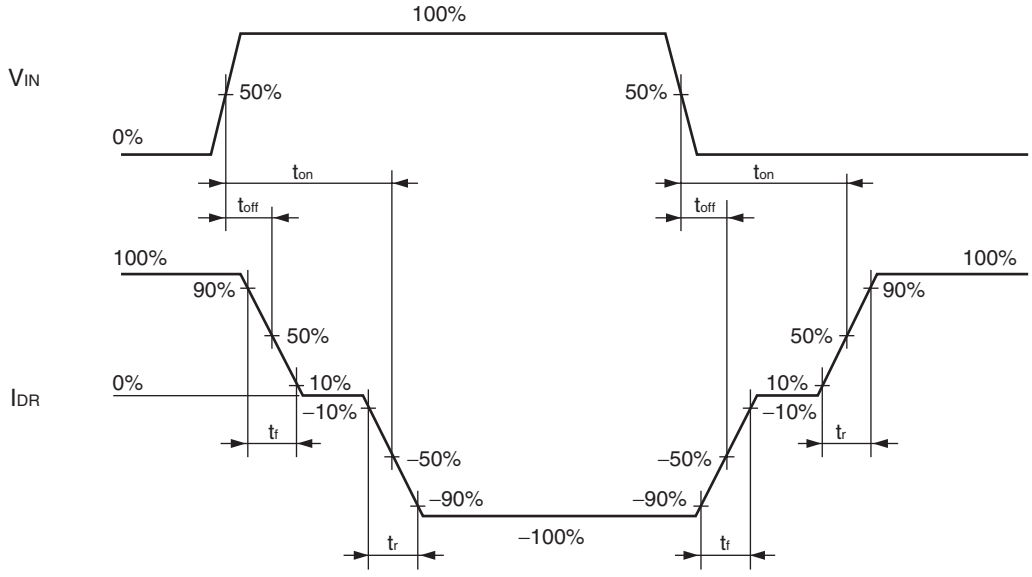
Overall and H-bridge block (stepping motor)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LV_{DD} pin current in standby mode	$ILV_{DD(STB)}$	RESETB = 0 V			1.0	μA
AV_{DD} pin current in standby mode	$IAV_{DD(STB)}$	RESETB = 0 V			1.0	μA
V_M pin current in standby mode	$IV_{M(STB)}$	RESETB = 0 V			1.0	μA
LV_{DD} pin current in during operation	$I_{DD(ACT)}$	RESETB = LV_{DD}			2.0	mA
High-level input current	I_{IH}	V_{IN} = LV_{DD}			60	μA
Low-level input current	I_{IL}	V_{IN} = 0 V	−1.0			μA
Input pull-down resistance	R_{IND}		50		200	kΩ
High-level input voltage	V_{IH}		0.7 x V_{DD}			V
Low-level input voltage	V_{IL}				0.3 x V_{DD}	V
H-bridge on-state resistance	R_{on}	I_M = 0.2 A, sum of upper and lower stages		2.0	3.0	Ω
Output leakage current Note 1	$I_{M(off)}$	Per V_M pin, All control pins: low level			1.0	μA
Low-voltage detection voltage Note 2	V_{DDS1}	RESETB = H		1.7	2.5	V
Output turn-on time	t_{on}	R_L = 20 Ω		0.5	1.0	μs
Output turn-off time	t_{off}			0.1	0.4	μs
Output rise time	t_r		0.05	0.2	0.4	μs
Output fall time	t_f			50	100	ns

Notes 1. μPD168103 has a circuit that prevents current from flowing into the V_M pin when LV_{DD} = 0 V.

2. Unlike normal operations, after a reset the detection voltage becomes 0.6 V TYP.

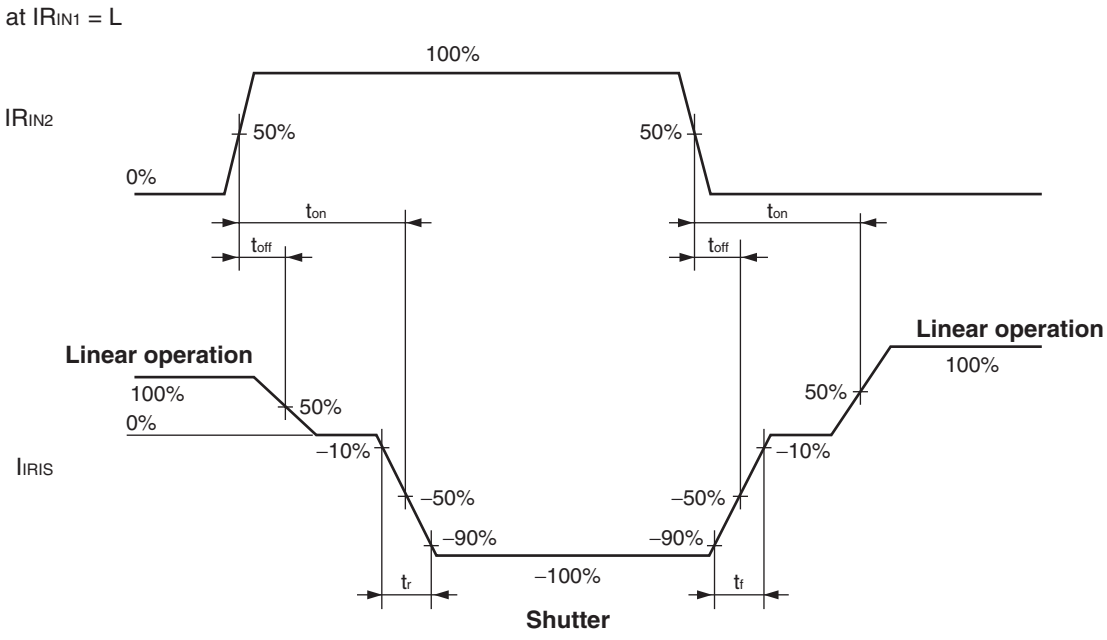
Figure 6–1. Switching Characteristic Waveform of the Stepping Motor Driving Block



H-bridge block (IRIS motor)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
V_{IRIS} pin current in standby mode	$IV_{IRIS(STB)}$	RESETB = 0 V			1.0	μA
$V_{SHUTTER}$ pin current in standby mode	$IV_{SHUTTER(STB)}$	RESETB = 0 V			1.0	μA
High-level input current	I_{IH}	$V_{IN} = LV_{DD}$			1.0	μA
Low-level input current	I_{IL}	V_{IN} = 0 V	−60			μA
Input pull-up resistance	R_{IND}		50		200	kΩ
High-level input voltage	V_{IH}		0.7 x V_{DD}			V
Low-level input voltage	V_{IL}				0.3 x V_{DD}	V
H-bridge on-state resistance	R_{on1}	R_L = 50 Ω, sum of upper and lower stages		2.5	3.5	Ω
Output turn-on time	t_{onH1}	When linear driving, R_L = 50 Ω	0.01	25	35	μs
	t_{onH2}	When full ON, R_L = 50 Ω	0.01	1.0	2.0	μs
Output turn-off time	t_{offH}		0.01	1.0	2.0	μs
Output rise time	t_{rH}			60		ns
Output fall time	t_{fH}			80		ns
Control amplifier offset voltage	V_{IO}	AMP5		±5	±7.5	mV

Figure 6–2. Switching Characteristic Waveform of the IRIS Motor Driving Block

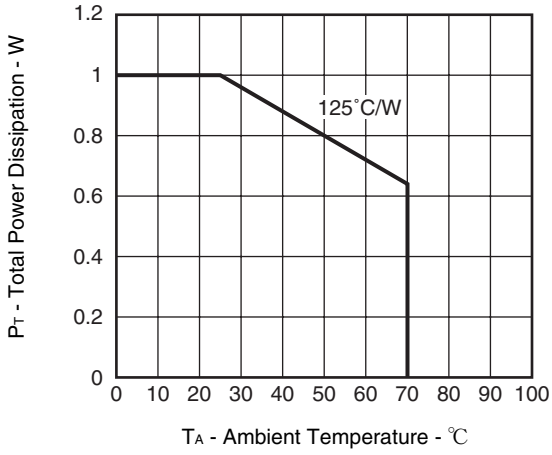


Operational amplifier block

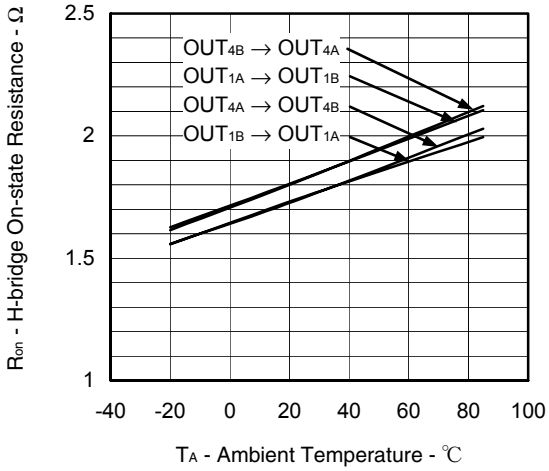
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
AV_{DD} pin current in during operation	IA_{DD}	Output open			3.0	mA
Input offset voltage 1	V_{IO1}	AMP1 to AMP3, AMP5		±3	±5	mV
Input offset voltage 2	V_{IO2}	AMP4		±5	±7	mV
Common mode input voltage range 1	V_{ICM1}	AMP1 to AMP3, AMP5	0		AV_{DD} – 1.5	V
Common mode input voltage range 2	V_{ICM2}	AMP4	0		AV_{DD} – 2.0	V
High-level output voltage	V_{OH}	AMP1 to AMP3, when I_{OUT} = +2 mA	AV_{DD} – 0.2			V
Low-level output voltage	V_{OL}	AMP1 to AMP3, when I_{OUT} = –2 mA			0.2	V
Large amplitude voltage gain	A_V	AMP1 to AMP3, DC	80			dB
Slew-rate	SR	AMP1 to AMP3, A_V = 1 dB ,$R_L \geq 10$ kΩ		0.5		V/μs
1/2 AV_{DD} output voltage accuracy	V_O	AMP0, I_{OUT} = ±100 μA	2.4	2.5	2.6	V

7. TYPICAL CHARACTERISTICS (Unless otherwise specified, T_A = 25°C, LV_{DD} = 3.0 V, AV_{DD} = V_M = $V_{SHUTTER}$ = V_{IRIS} = 5.0 V)

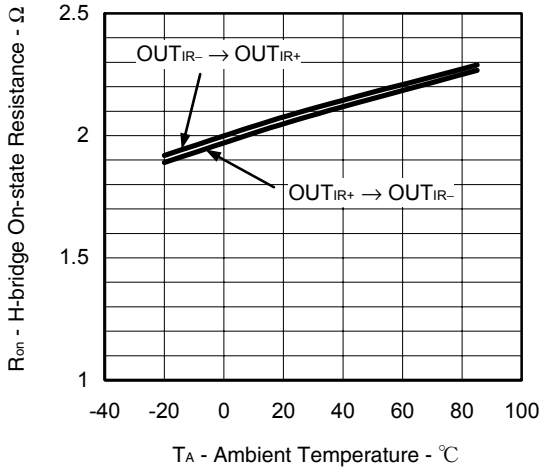
P_T vs. T_A CHARACTERISTIC



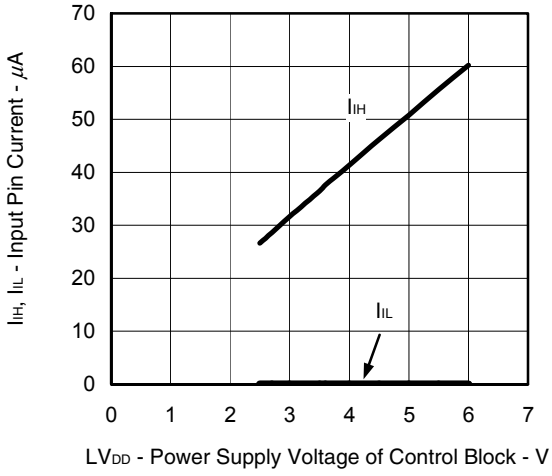
R_{on} vs. T_A CHARACTERISTIC (H-bridge 1 to 4)



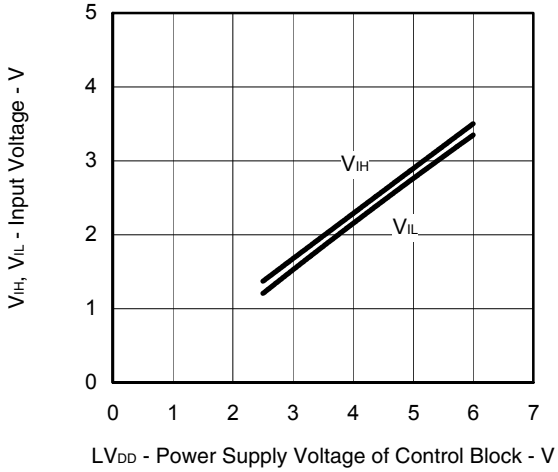
R_{on} vs. T_A CHARACTERISTIC (H-bridge IRIS)



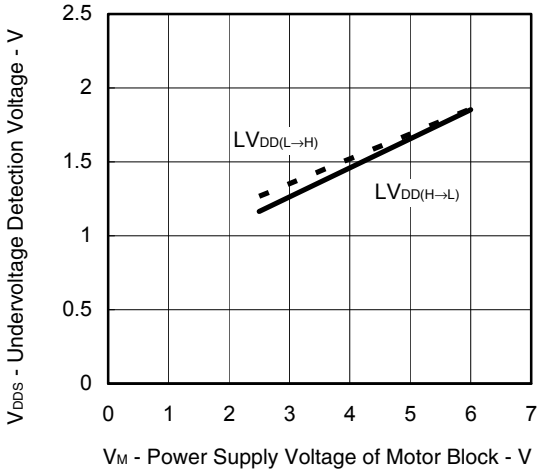
I_{IH}, I_{IL} vs. LV_{DD} CHARACTERISTIC



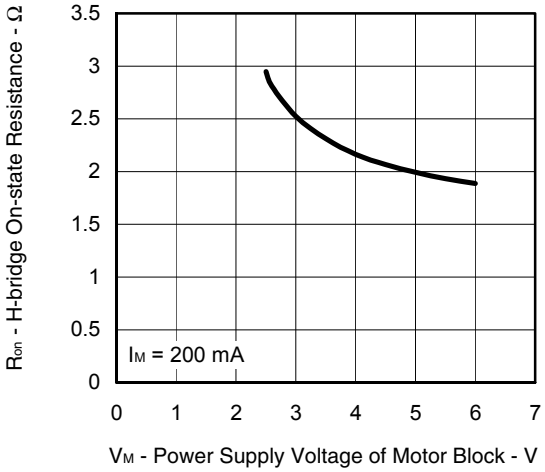
V_{IH}, V_{IL} vs. LV_{DD} CHARACTERISTIC



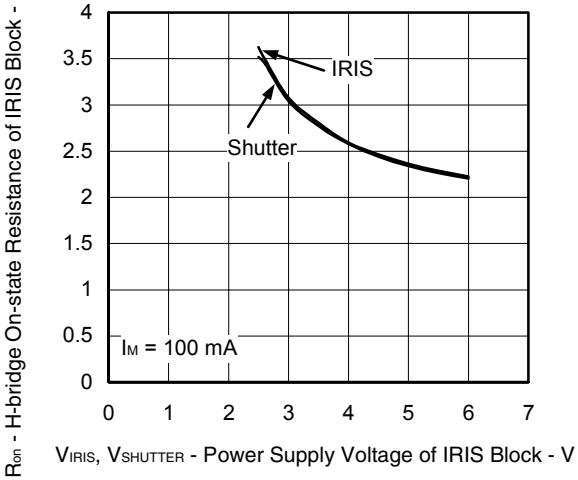
UNDERVOLTAGE LOCKOUT CIRCUIT CHARACTERISTIC



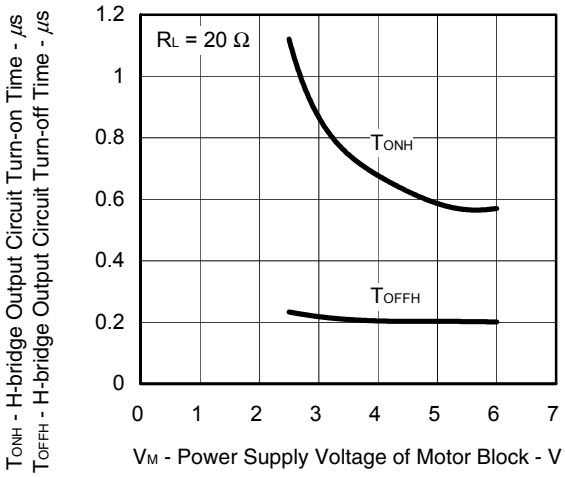
R_{on} vs. V_M CHARACTERISTIC



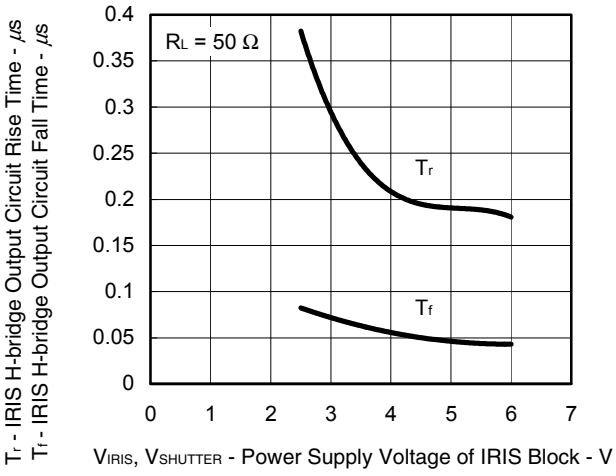
R_{on} vs. V_{IRIS}, $V_{SHUTTER}$ CHARACTERISTIC



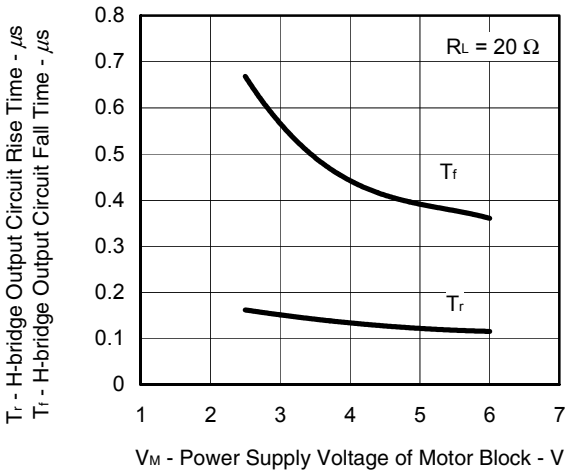
T_{ONH}, T_{OFFH} vs. V_M CHARACTERISTIC



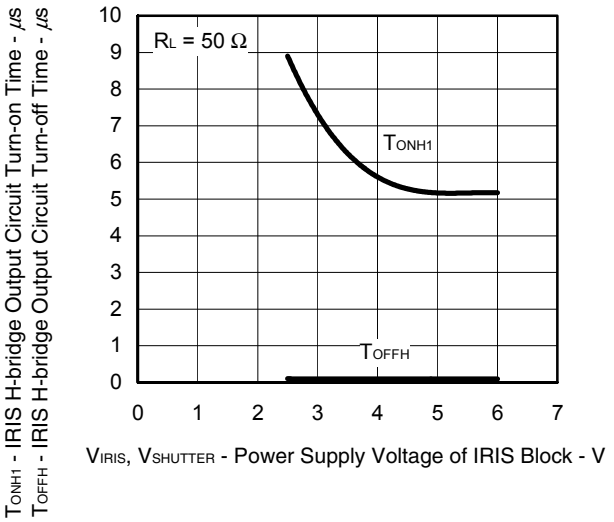
T_r, T_f vs. V_{IRIS}, $V_{SHUTTER}$ CHARACTERISTIC (when full ON)



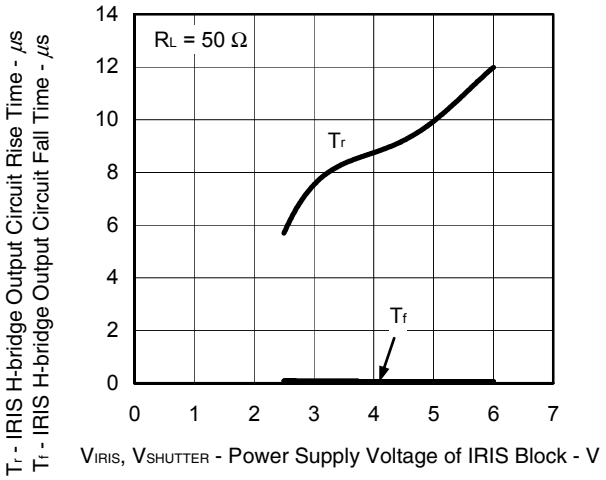
T_r, T_f vs. V_M CHARACTERISTIC



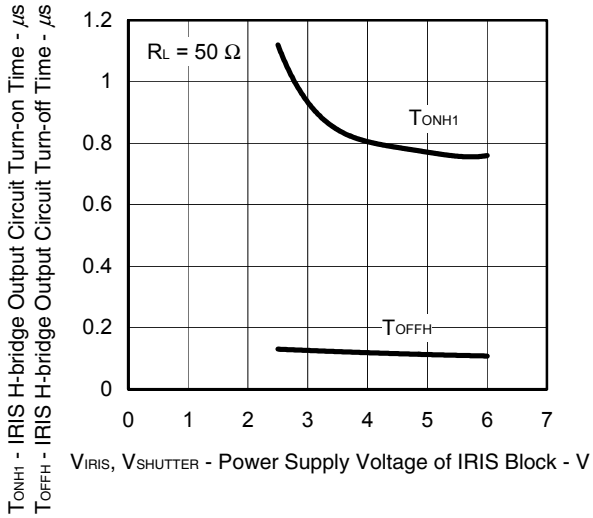
T_{ONH1}, T_{OFFH} vs. V_{IRIS}, $V_{SHUTTER}$ CHARACTERISTIC (when Linear)



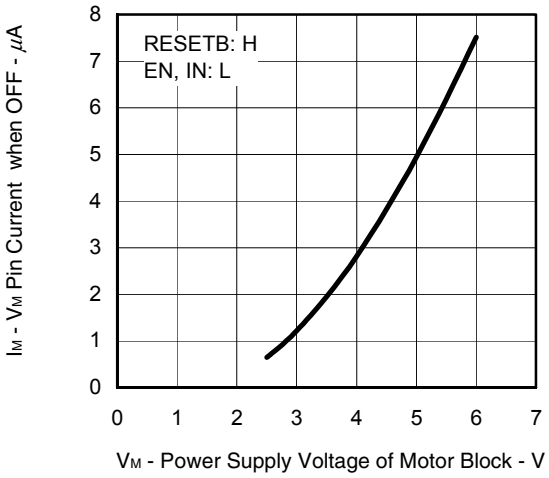
T_r, T_f vs. V_{IRIS}, $V_{SHUTTER}$ CHARACTERISTIC (when Linear)



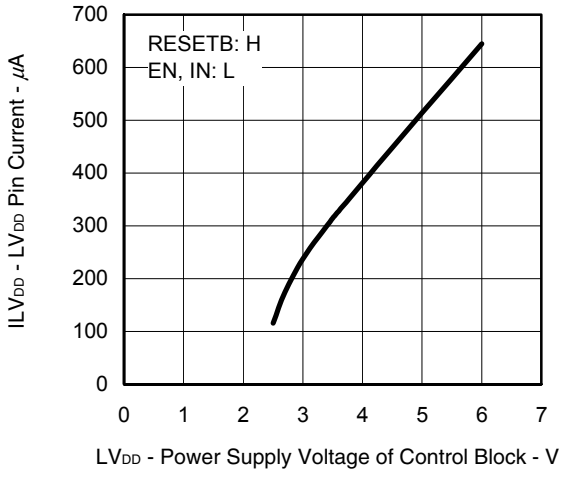
T_{ONH1}, T_{OFFH} vs. V_{IRIS}, $V_{SHUTTER}$ CHARACTERISTIC (when full ON)



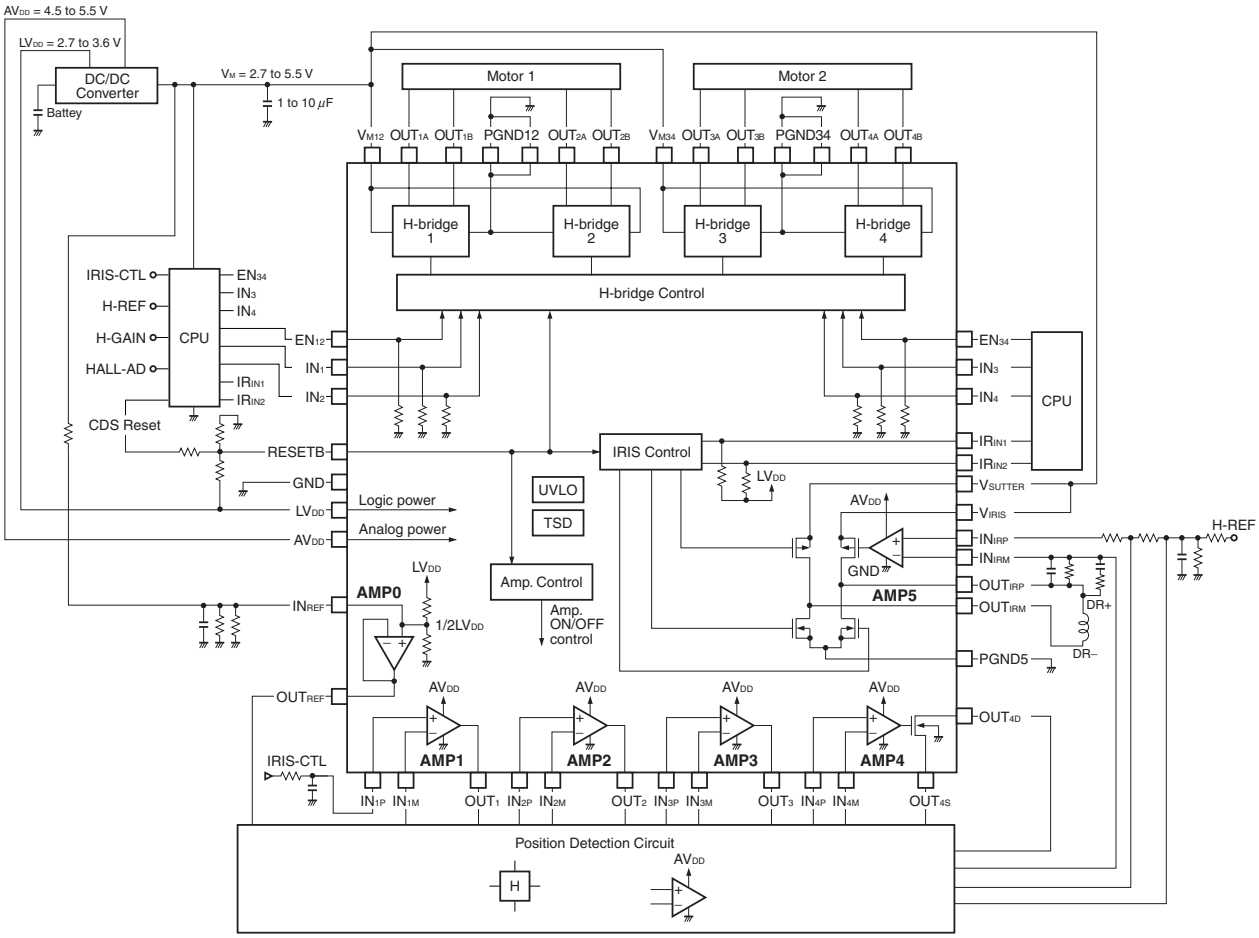
I_M vs. V_M CHARACTERISTIC



ILV_{DD} vs. LV_{DD} CHARACTERISTIC

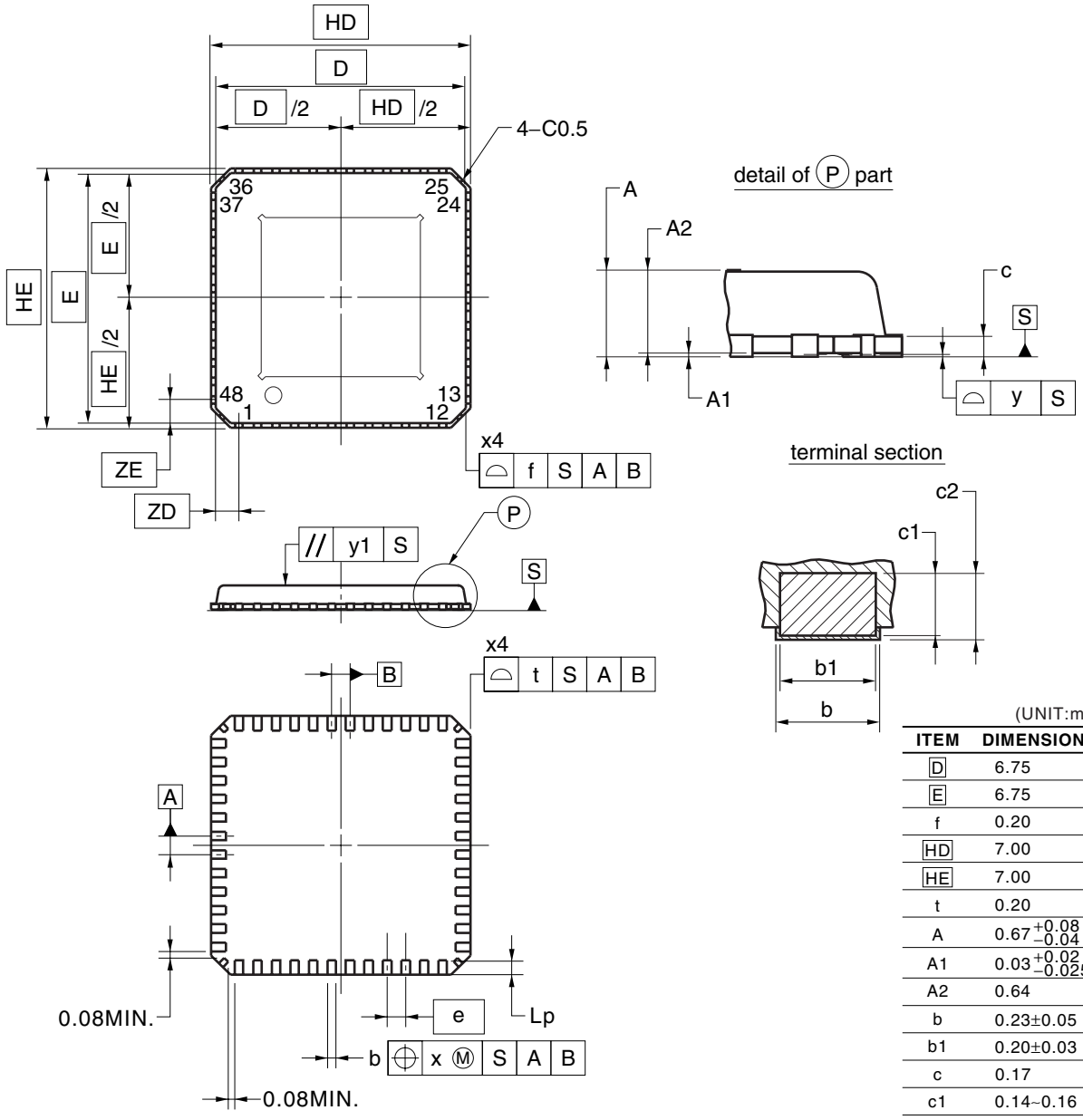


8. STANDARD CONNECTION EXAMPLE



9. PACKAGE DRAWING

48-PIN PLASTIC WQFN (7x7)



(UNIT:mm)

ITEM	DIMENSIONS
D	6.75
E	6.75
f	0.20
HD	7.00
HE	7.00
t	0.20
A	$0.67^{+0.08}_{-0.04}$
A1	$0.03^{+0.02}_{-0.025}$
A2	0.64
b	0.23±0.05
b1	0.20±0.03
c	0.17
c1	0.14~0.16
c2	0.14~0.20
e	0.50
Lp	0.40±0.10
x	0.05
y	0.08
y1	0.10
ZD	0.625
ZE	0.625

P48K9-50-5B4-1

NOTES

※1 "t" AND "f" EXCLUDES MOLD FLASH

※2 ALTHOUGH THERE ARE 4 TERMINALS IN THE CORNER PART OF A PACKAGE, THESE TERMINALS ARE NOT DESIGNED FOR INTERCONNECTION, BUT FOR MANUFACTURING PROCESS OF THE PACKAGE, THEREFOR DO NOT INTEND TO SOLDER THESE 4 TERMINALS, SOLDERABLITY OF THE 4 TERMINALS ARE NOT GUARANTEED.

10. RECOMMENDED SOLDERING CONDITIONS

The μPD168103 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Type of Surface Mount Device

μPD168103K9-5B4-A [Note1]: 48-pin plastic WQFN (7 x 7)

Process	Conditions	Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds MAX. (at 220°C or higher) , Count: Three times or less, Exposure limit: 3 days [Note2] (after that, prebake at 125°C for 10 hours) , Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. <Precaution> Products other than in heat-resistant trays (such as those packaged in a magazine, taping, or non-thermal-resistant tray) cannot be baked in their package.	IR60-103-3

Notes 1. Pb-free (This product does not contain Pb in external electrode and other parts.)

2. After opening the dry pack, store it a 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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