

Token Ring Front End Filter Module

EPT7068G

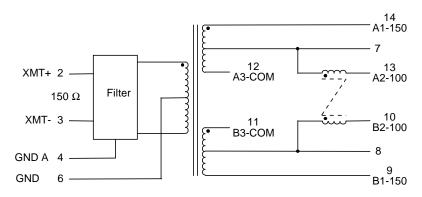


- Optimized for 150 Ω Voltage Source Drivers •
- Enhanced Common Mode Rejection Capability
 - Low Profile, Single Channel Module •
- Complies with or exceeds IEEE 802.5 Requirements •

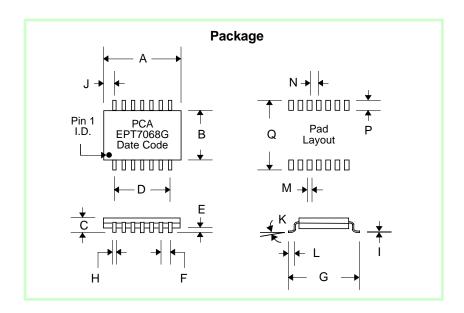
Electrical Parameters @ 25° C

Impedance (Ω) [Xmit/Rcv]	Insertion Loss (dB)				Return Loss (dB Min.)			Common Mode Rejection (dB Min.)			
Media Side 150	1-16 MHz (Max.)	32 MHz (Min.)	36 MHz (Min.)	44 MHz (Min.)	1-6 MHz	6-17 MHz	17-25 MHz	1-30 MHz	30-100 MHz	100-200 MHz	200-300 MHz
Cable Side 150/100	8	-7	-18	-30	-18	-12	-8	-40	-20	-15	-10

Schematic



Pins 1 & 5 are not connected.



Dimensions

	((Inches)		(millimeters)				
Dim.	Min.	Max.	Nom.	Min.	Max.	Nom.		
Α	.780	.800	.790	19.81	20.32	20.07		
В	.510	.530	.520	12.95	13.46	13.21		
С	.090	.100	.095	2.29	2.54	2.41		
D	.595	.605	.600	15.11	15.37	15.24		
E	.003	.010	.005	.076	.254	.127		
F	.097	.103	.100	2.46	2.62	2.54		
G	.660	.680	.670	16.76	17.27	17.02		
H	.017	.022	.020	.432	.559	.508		
	.008	.013	.011	.203	.330	2.79		
J	.090	.100	.095	2.29	2.54	2.41		
K	0°	8°	4°	0°	8°	4°		
L	.025	.045	.040	.635	1.14	1.02		
M			.030			.762		
N			.100			2.54		
Р			.085			2.16		
Q			.700			17.78		

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The circuit below is a guideline for interconnecting PCA's EPT7068G with a typical Token Ring PHY chip for 4 Mb/16Mb applications over STP or UTP cable. Further details of system design should be obtained from the specific chip manufacturer. Note that this module is optimized for a "voltage source" driver such as TI380C series. Only one type of cable should be driven by the module: either UTP or STP. If you are using 120Ω cable or desire to install only one RJ45 connector thus leaving the STP use with a dongle when needed, please refer to PCA part numbers EPT7069 or similar parts optimized for 120Ω cable.

Note that the receiver side filtering is identical, thus making it possible for use in a DTR application as well. Consider this a cost effective solution for almost all Token Ring applications using this chip or similar chips.

The pull down resistors to chassis via a cap shown around the RJ45 connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. This is specially true if driving UTP cable. Their placement and use are to be considered carefully before a design is finalized.

No specific recommendation is made here for phantom circuitry, implementation varies. Please note that additional emission control has been observed if both nodes of the phantom bypass capacitor on the transmit channel are pulled to the chassis ground via suitable capacitors.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPT7068G. There need not be any ground plane beyond this point.

For best results, PCB designer should design the outgoing traces preferably to be $75\Omega/50\Omega$, balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit Connection to TI380C30 (or Equivalent)

