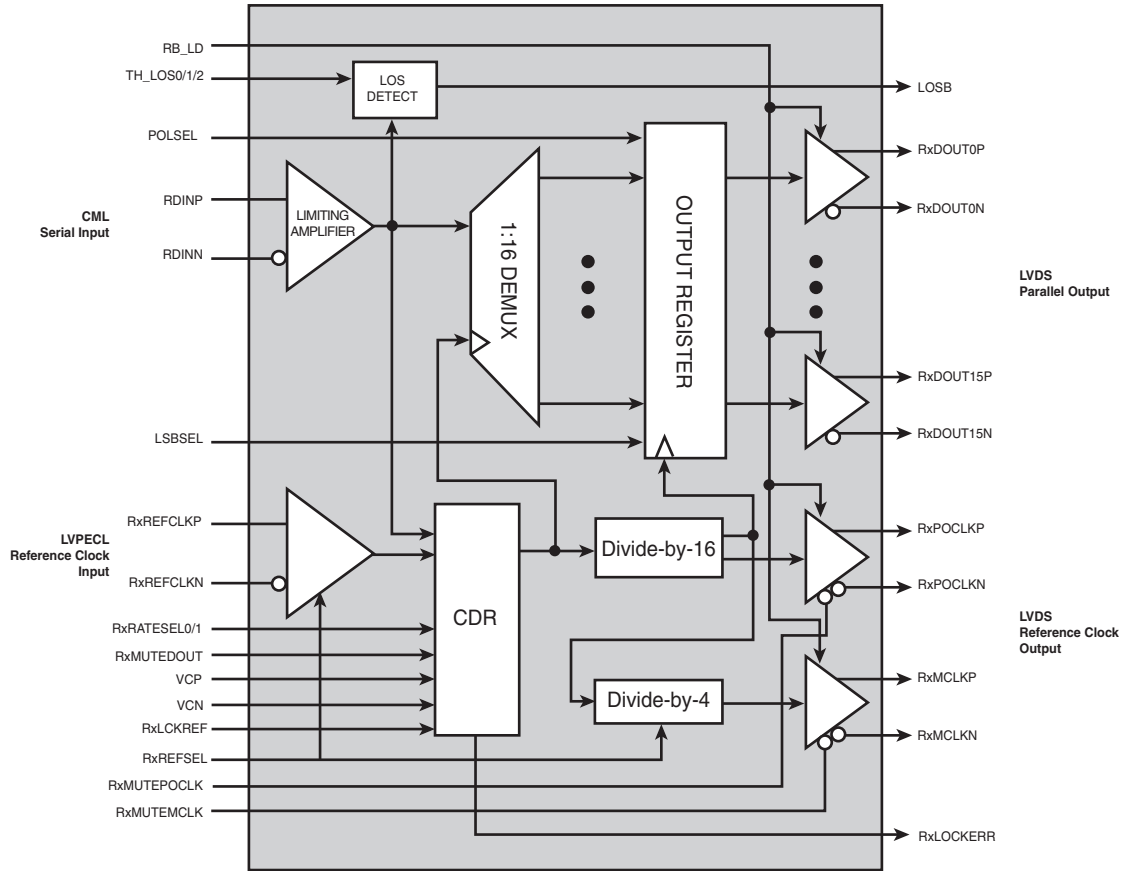


OVERVIEW



The **BCM8125** is a fully integrated MSA-compatible quad-rate SONET/SDH/10GE receiver operating at OC-192/STM-64, 10GE, and two different FEC (Forward Error Correction) data rates (9.953, 10.3125, 10.664, and 10.709 Gbps) with deserializer, clock and data recovery (CDR), and loss-of-signal (LOS) detection circuitry. The **BCM8125** provides high-jitter tolerance and low-jitter generation to comply with Optical Internetworking Forum (OIF), IEEE 802.3ae, Telcordia, ANSI, and ITU-T standards.

The **BCM8125** reference clock input frequency is user-selectable to the line rate divided by either 16 or 64. The reference clock output and the LVDS receive parallel bus output can be squelched under user control. An integrated limiting amplifier provides the **BCM8125** with input sensitivity down to 10 mV single ended, saving the customer cost and power.

The **BCM8125** can be powered with a single 1.8V supply or dual 1.8/3.3V supply without any special power supply sequencing requirements.

The **BCM8125** comes in an 11 x 11 mm, 127-pin BGA package.

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