6-Bit Programmable 2-/3-Phase Synchronous Buck Controller

ADP3197

FEATURES

Selectable 2-phase and 3-phase operation at up to 1 MHz per phase
±10 mV worst-case differential sensing error over temperature
Logic-level PWM outputs for interface to external high power drivers
Enhanced PWM flex mode for excellent load transient performance
Active current balancing between all output phases
Built-in power good/crowbar blanking that supports on-the-fly VID code changes
Digitally programmable 0.3750 V to 1.55 V output
Programmable short-circuit protection with programmable latch-off delay

APPLICATIONS

Desktop PC power supplies for
Next-generation AMD processors
Voltage regulator modules (VRM)

GENERAL DESCRIPTION

The ADP3197[1] is a highly efficient multiphase synchronous buck switching regulator controller optimized for converting a 12 V main supply into the core supply voltage required by high performance, Advanced Micro Devices, AMD processors. It uses an internal 6-bit digital-to-analog converter (DAC) to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 0.3750 V and 1.55 V. It uses a multimode pulse-width modulation (PWM) architecture to drive the logic level outputs at a programmable switching frequency that can be optimized for VR size and efficiency. The phase relationship of the output signals can be programmed to provide 2-phase or 3-phase operation, allowing for the construction of up to three complementary buck switching stages.

The ADP3197 supports a programmable slope function to adjust the output voltage as a function of the load current so it is always optimally positioned for a system transient. This can be disabled by connecting the LLSET pin to the CSREF pin.

The ADP3197 also provides accurate and reliable short-circuit protection, adjustable current limiting, and a delayed power-good output that accommodates on-the-fly output voltage changes requested by the CPU.

[1]Protected by U.S. Patent Number 6,683,441; other patents pending.

FUNCTIONAL BLOCK DIAGRAM

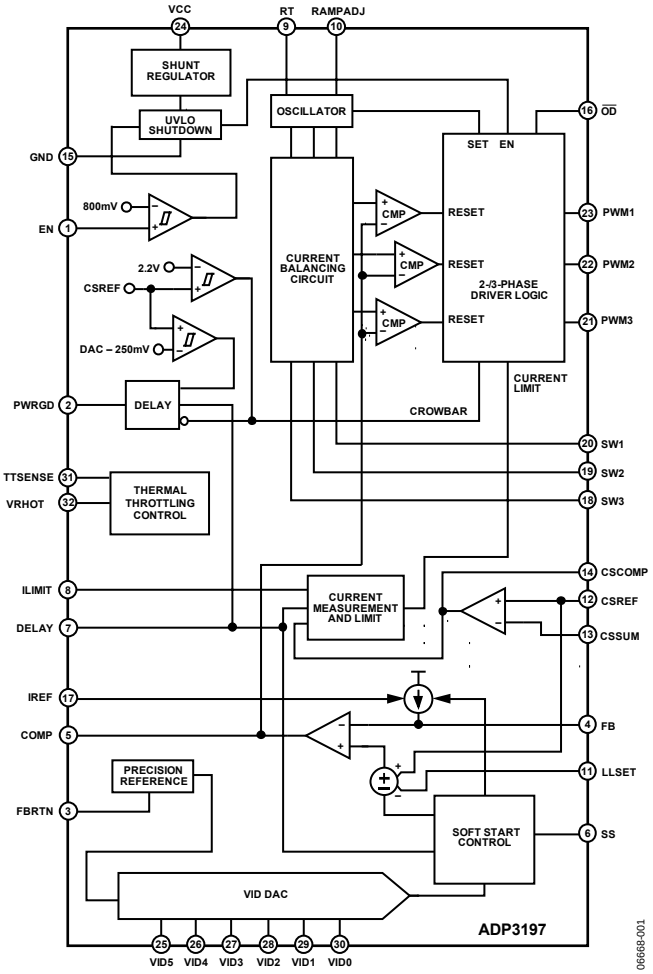

Figure 1.

The ADP3197 has a built-in shunt regulator that allows the part to be connected to the 12 V system supply through a series resistor.

The ADP3197 is specified over the extended commercial temperature range of 0°C to 85°C and is available in a 32-lead LFCSP.

Rev. 0
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REVISION HISTORY

5/07—Revision 0: Initial Version

SPECIFICATIONS

VCC = 5 V, FBRTN = GND, T_A = 0°C to 85°C, unless otherwise noted[1]

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
REFERENCE CURRENT						
Reference Bias Voltage	V_{IREF}			1.5		V
Reference Bias Current	I_{IREF}	R_{IREF} = 100 kΩ	14.25	15	15.75	µA
ERROR AMPLIFIER						
Output Voltage Range[2]	V_{COMP}		0.05		4.4	V
Accuracy	V_{FB}	Relative to nominal DAC output, referenced to FBRTN, LLSET = CSREF (see Figure 4)	−10		10	mV
Load Line Positioning Accuracy		CSREF − LLSET = 80 mV	−78	−80	−82	mV
Differential Nonlinearity			−1		+1	LSB
Input Bias Current	I_{FB}	$I_{FB} = 0.5 \times I_{IREF}$	−9	−7.5	−6	µA
FBRTN Current	I_{FBRTN}			65	200	µA
Output Current	I_{COMP}	FB forced to V_{OUT} − 3%		500		µA
Gain Bandwidth Product	$GBW_{(ERR)}$	COMP = FB		20		MHz
Slew Rate		COMP = FB		25		V/µs
LLSET Input Voltage Range	V_{LLSET}	Relative to CSREF	−250		+250	mV
LLSET Input Bias Current	I_{LLSET}		−10		+10	nA
VID INPUTS						
Input Low Voltage	$V_{IL(VID)}$	VIDx, VIDSEL			0.6	V
Input High Voltage	$V_{IH(VID)}$	VIDx, VIDSEL	1.4			V
Input Current	$I_{IN(VID)}$			−10		µA
VID Transition Delay Time[2]		VID code change to FB change	400			ns
OSCILLATOR						
Frequency Range[2]	f_{OSC}		0.25		3	MHz
Frequency Variation	f_{PHASE}	T_A = 25°C, R_T = 280 kΩ, 3-phase	180	200	220	kHz
		T_A = 25°C, R_T = 130 kΩ, 3-phase		400		kHz
		T_A = 25°C, R_T = 57.6 kΩ, 3-phase		800		kHz
Output Voltage	V_{RT}	R_T = 280 kΩ to GND	1.9	2.0	2.1	V
RAMPADJ Output Voltage	$V_{RAMPADJ}$	RAMPADJ − FB, DAC=1.55 V	−50		+50	mV
RAMPADJ Input Current Range	$I_{RAMPADJ}$		1		50	µA
CURRENT SENSE AMPLIFIER						
Offset Voltage	$V_{OS(CSA)}$	CSSUM − CSREF (see Figure 5)	−1.0		+1.0	mV
Input Bias Current	$I_{BIAS(CSSUM)}$		−10		+10	nA
Gain Bandwidth Product	$GBW_{(CSA)}$	CSSUM = CSCOMP		10		MHz
Slew Rate		C_{CSCOMP} = 10 pF		10		V/µs
Input Common-Mode Range		CSSUM and CSREF	0		3.5	V
Output Voltage Range			0.05		3.5	V
Output Current	I_{CSCOMP}			500		µA
Current Limit Latch-off Delay Time	$t_{OC(DELAY)}$	C_{DELAY} = 10 nF		8		ms
CURRENT BALANCE AMPLIFIER						
Common-Mode Range	V_{SWxCM}		−600		+200	mV
Input Resistance	R_{SWx}	SWx = 0 V	10	17	26	kΩ
Input Current	I_{SWx}	SWx = 0 V	8	12	20	µA
Input Current Matching	ΔI_{SWx}	SWx = 0 V	−4		+4	%
CURRENT LIMIT COMPARATOR						
ILIMIT Bias Current	I_{ILIMIT}	$I_{ILIMIT} = 2/3 \times I_{IREF}$	9	10	11	µA
ILIMIT Voltage	V_{ILIMIT}	R_{ILIMIT} = 121 kΩ ($V_{ILIMIT} = I_{ILIMIT} \times R_{ILIMIT}$)	1.09	1.21	1.33	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Output Voltage			3			V
Current Limit Threshold Voltage	V_{CL}	$V_{CSREF} - V_{CSCOMP}$, R_{ILIMIT} = 121 kΩ	80	100	125	mV
Current Limit Setting Ratio		V_{CL}/I_{ILIMIT}		82.6		mV/V
DELAY TIMER						
Normal Mode Output Current	I_{DELAY}	$I_{DELAY} = I_{IREF}$	12	15	18	µA
Output Current in Current Limit	$I_{DELAY(CL)}$	$I_{DELAY(CL)} = 0.25 \times I_{IREF}$	3.0	3.75	4.5	µA
Threshold Voltage	$V_{DELAY(TH)}$		1.6	1.7	1.8	V
SOFT START						
Output Current (Startup)	$I_{SS(STARTUP)}$	During startup, $I_{SS(STARTUP)} = 0.25 \times I_{IREF}$	3	3.75	4.5	µA
Output Current (DAC Code Change)	$I_{SS(DAC)}$	DAC code change, $I_{SS(DAC)} = 1.25 \times I_{IREF}$	15	18.75	22.5	µA
ENABLE INPUT						
Threshold Voltage	$V_{TH(EN)}$		750	800	850	mV
Hysteresis	$V_{HYS(EN)}$		80	100	125	mV
Input Current	$I_{IN(EN)}$			−1		µA
Delay Time	$t_{DELAY(EN)}$	EN > 950 mV, C_{DELAY} = 10 nF		2		ms
$\overline{OD}$ OUTPUT						
Output Low Voltage	$V_{OL(\overline{OD})}$			160	500	mV
Output High Voltage	$V_{OH(\overline{OD})}$		4	5		V
$\overline{OD}$ Pulldown Resistor				60		kΩ
THERMAL THROTTLING CONTROL						
TTSENSE Voltage Range		Internally limited	0		5	V
TTSENSE Bias Current			−135	−123	−111	µA
TTSENSE VRHOT Threshold Voltage			665	710	755	mV
TTSENSE Hysteresis				50		mV
VRHOT Output Low Voltage	$V_{OL(VRHOT)}$	$I_{VRHOT(SINK)}$ = −4 mA		150	300	mV
POWER-GOOD COMPARATOR						
Overvoltage Threshold	$V_{PWRGD(OV)}$	Relative to nominal DAC output; DAC = 0.5 V to 1.55 V	200	250	300	mV
		Relative to nominal DAC output; DAC = 0.375 V to 0.4785 V	190	250	310	mV
Undervoltage Threshold	$V_{PWRGD(UV)}$	Relative to nominal DAC output; DAC = 0.5 V to 1.55 V	−300	−250	−200	mV
		Relative to nominal DAC output; DAC = 0.375 V to 0.4785 V	−310	−250	−190	mV
Output Low Voltage	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = −4 mA		150	300	mV
Power-Good Delay Time						
During Soft Start[2]		C_{DELAY} = 10 nF		2		ms
VID Code Changing			100	250		µs
VID Code Static				200		ns
Crowbar Trip Point	$V_{CROWBAR}$	Relative to FBRTN	1.75	1.8	1.85	V
Crowbar Reset Point		Relative to FBRTN		300		mV
PWM OUTPUTS						
Output Low Voltage	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = −400 µA		160	500	mV
Output High Voltage	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = +400 µA	4.0	5		V
SUPPLY		V_{SYSTEM} = 12 V, R_{SHUNT} = 340 Ω (see Figure 4)				
VCC	VCC		4.65	5	5.55	V
DC Supply Current	I_{VCC}				25	mA
UVLO Turn On Current				6.5	11	mA
UVLO Threshold Voltage	V_{UVLO}	VCC rising	9			
UVLO Threshold Voltage	V_{UVLO}	VCC falling		4.1		V

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] Guaranteed by design or bench characterization; not tested in production.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC	−0.3 V to +6 V
FBRTN	−0.3 V to +0.3 V
PWM3, RAMPADJ	−0.3 V to VCC + 0.3 V
SW1 to SW3	−5 V to +25 V
<200 ns	−10 V to +25 V
All Other Inputs and Outputs	−0.3 V to VCC + 0.3 V
Storage Temperature Range	−65°C to +150°C
Operating Ambient Temperature Range	0°C to 85°C
Operating Junction Temperature	125°C
Thermal Impedance (θ_{JA})	100°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Infrared (15 sec)	260°C

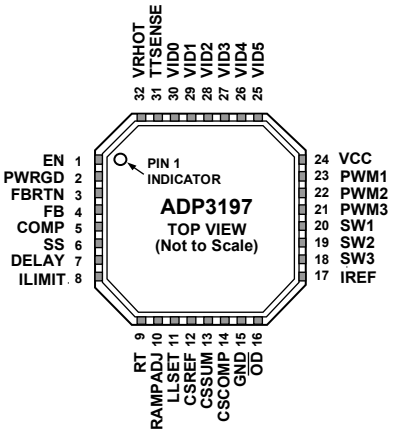
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED EPAD ON BOTTOM SIDE OF PACKAGE IS AN ELECTRICAL CONNECTION AND SHOULD BE SOLDERED TO GROUND.

06668-005

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
2	PWRGD	Power-Good Output. Open-drain output that signals when the output voltage is outside proper operating range.
3	FBRTN	Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage.
4	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no load offset point.
5	COMP	Error Amplifier Output and Compensation Point.
6	SS	Soft Start Delay Setting Input. An external capacitor connected between this pin and GND sets the soft start ramp-up time.
7	DELAY	Delay Timer Setting Input. An external capacitor connected between this pin and GND sets the overcurrent latch-off delay time, EN delay time, and PWRGD delay time.
8	ILIMIT	Current Limit Set Point. An external resistor from this pin to GND sets the current limit threshold of the converter.
9	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
10	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
11	LLSET	Output Load Line Programming Input. This pin can be directly connected to CSCOMP, or it can be connected to the center point of a resistor divider between CSCOMP and CSREF. Connecting LLSET to CSREF disables positioning.
12	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the power-good and crowbar functions. This pin should be connected to the common point of the output inductors.
13	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.
14	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determine the gain of the current sense amplifier and the positioning loop response time.
15	GND	Ground. All internal biasing and logic output signals of the device are referenced to this ground.
16	$\overline{OD}$	Output Disable Logic Output. This pin is actively pulled low when EN input is low or when VCC is below its UVLO threshold to signal to the driver IC that the driver high-side and low-side outputs should go low.
17	IREF	Current Reference Input. An external resistor from this pin to ground sets the reference current for I_{FB}, I_{DELAY}, I_{SS}, I_{ILIMIT}, and $I_{TTSENSE}$.
18 to 20	SW3 to SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SWx pins of unused phases should be left open.

Pin No.	Mnemonic	Description
21 to 23	PWM3 to PMW1	Logic Level PWM Outputs. Each output is connected to the input of an external MOSFET driver, such as the ADP3120. Connecting the PWM3 output to VCC causes that phase to turn off, allowing the ADP3197 to operate as a 2-phase or 3-phase controller.
24	VCC	A 340 Ω resistor should be placed between the 12 V system supply and the VCC pin. The internal shunt regulator maintains VCC = 5 V.
25 to 30	VID5 to VID0	Voltage Code DAC Inputs. These six pins are pulled down to GND, providing a Logic 0 if left open. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.3750 V and 1.55 V (see Table 4).
31	TTSENSE	VR Hot Thermal Throttling Sense Input. An NTC thermistor between this pin and GND is used to remotely sense the temperature at the desired thermal monitoring point.
32	VRHOT	Open-Drain Output. This output signals when the temperature at the monitoring point connected to TTSENSE exceeds the maximum operating temperature. This can be connected to the PROCHOT# (a PC system signal) output from the CPU.

TYPICAL PERFORMANCE CHARACTERISTICS

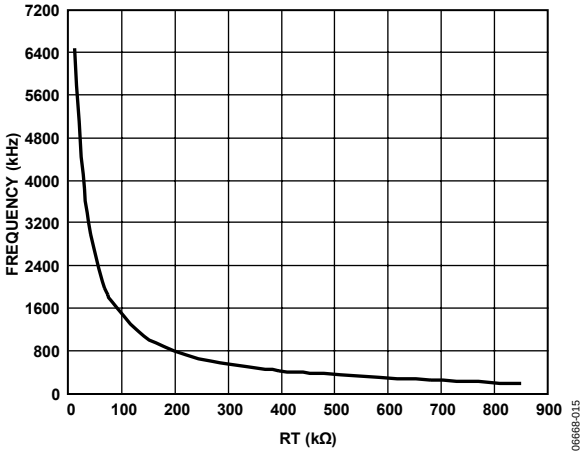


Figure 3. Master Clock Frequency vs. R_T

TEST CIRCUITS

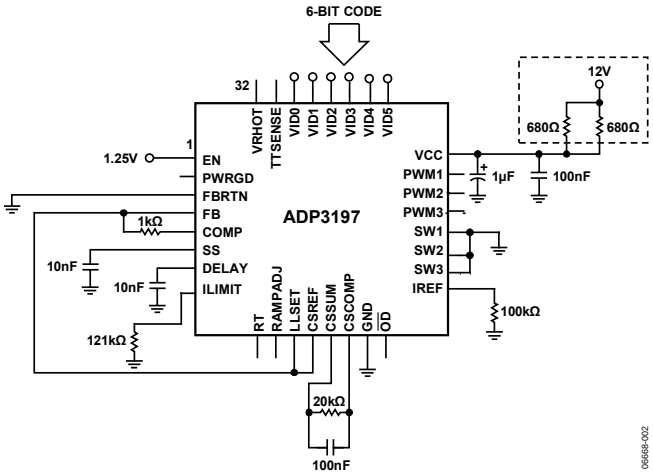


Figure 4. Closed-Loop Output Voltage Accuracy

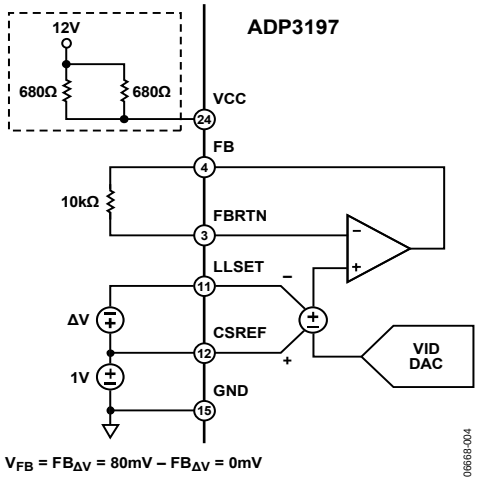


Figure 6. Positioning Voltage

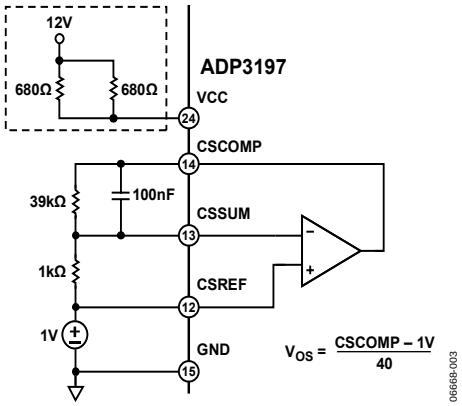


Figure 5. Current Sense Amplifier V_{OS}

THEORY OF OPERATION

The ADP3197 combines a multimode, fixed frequency PWM control with multiphase logic outputs for use in 2-phase and 3-phase synchronous buck CPU core supply power converters. The internal VID DAC is designed to interface with the AMD 6-bit CPUs.

Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling the high currents in a single-phase converter places high thermal demands on the components in the system, such as the inductors and MOSFETs.

The multimode control of the ADP3197 ensures a stable, high performance topology for

- Balancing currents and thermals between phases
- High speed response at the lowest possible switching frequency and output decoupling
- Minimizing thermal switching losses by utilizing lower frequency operation
- Tight load line regulation and accuracy, if load line is selected
- High current output from having up to 3-phase operation
- Reduced output ripple due to multiphase cancellation
- PC board layout noise immunity
- Ease of use and design due to independent component selection
- Flexibility in operation for tailoring design to low cost or high performance

START-UP SEQUENCE

The ADP3197 follows the start-up sequence shown in Figure 7. After both the EN and UVLO conditions are met, the DELAY pin goes through one cycle (TD1). The first four clock cycles of TD2 are blanked from the PWM outputs and used for phase detection, as explained in the Phase Detection Sequence section. Then the soft start ramp is enabled (TD2) and the output comes up to the programmed DAC voltage.

After TD2 has been completed and the PWRGD masking time (equal to VID on-the-fly masking) is finished, a second ramp on the DELAY pin sets the PWRGD blanking (TD3).

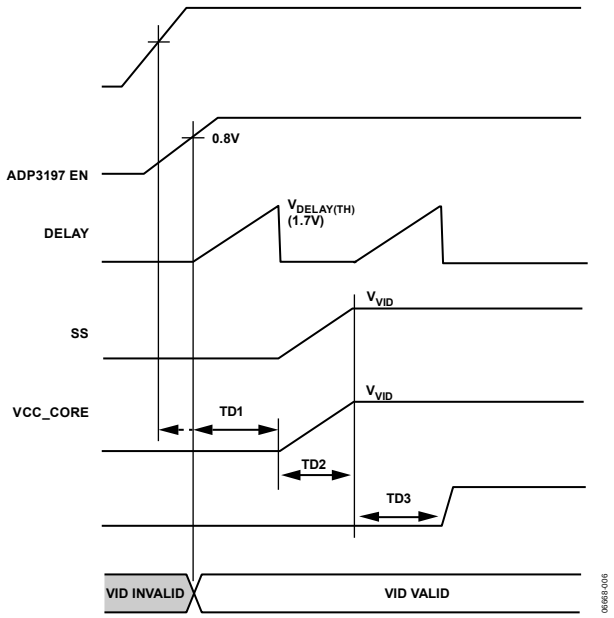


Figure 7. System Start-Up Sequence

PHASE DETECTION SEQUENCE

During startup, the number of operational phases and their phase relationships are determined by the internal circuitry that monitors the PWM outputs. Normally, the ADP3197 operates as a 3-phase PWM controller. Connecting the PWM3 pin to the VCC pin programs 2-phase operation.

While EN is low and prior to soft start, Pin PWM3 sinks approximately 100 μA. An internal comparator checks each pin voltage vs. a threshold of 3 V. If the pin is tied to VCC, it is above the threshold. Otherwise, an internal current sink pulls the pin to GND, which is below the threshold. PWM1 and PWM2 are low during the phase detection interval, which occurs during the first four clock cycles of TD2. After this time, if the remaining PWM outputs are not pulled to VCC, the 100 μA current sink is removed and the outputs function as normal PWM outputs. If they are pulled to VCC, the 100 μA current source is removed and the outputs are put into a high impedance state.

The PWM outputs are logic-level devices intended for driving external gate drivers, such as the ADP3120A. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one output can be on at the same time to allow overlapping phases.

MASTER CLOCK FREQUENCY

The clock frequency of the ADP3197 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 3. To determine the frequency per phase, the clock is divided by the number of phases in use. If all phases are in use, divide by 3. If the PWM3 pin is tied to VCC, then divide the master clock by 2 for the frequency of the remaining phases.

OUTPUT VOLTAGE DIFFERENTIAL SENSING

The ADP3197 combines differential sensing with a high accuracy VID DAC and reference and a low offset error amplifier. This maintains a worst-case specification of ±10 mV differential sensing error over its full operating output voltage and temperature range. The output voltage is sensed between the FB pin and the FBRTN pin. The FB pin should be connected through a resistor to the regulation point, usually the remote sense pin of the microprocessor. The FBRTN pin should be connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 65 μA to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

OUTPUT CURRENT SENSING

The ADP3197 provides a dedicated current sense amplifier (CSA) to monitor the total output current for proper voltage positioning vs. load current and for current limit detection. Sensing the load current at the output gives the total average current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element, such as the low-side MOSFET. This amplifier can be configured in the following ways, depending on the objectives of the system:

- Output inductor DCR sensing without a thermistor for lowest cost
- Output inductor DCR sensing with a thermistor for improved accuracy with tracking of inductor temperature
- Sense resistors for highest accuracy measurements

The positive input of the CSA is connected to the CSREF pin, which is connected to the output voltage. The inputs to the amplifier are summed together through resistors from the sensing element (such as the switch node side of the output inductors) to the inverting input, CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier, and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor. If required, an additional resistor divider connected between CSREF and CSCOMP, with the midpoint connected to LLSET, can be used to set the load line required by the microprocessor. The current information is then given as CSREF – LLSET. This difference signal is used internally to offset the VID DAC for voltage positioning.

The difference between CSREF and CSCOMP is then used as a differential input for the current limit comparator. This allows for the load line to be set independently of the current limit threshold. In the event that the current limit threshold and load line are not independent, the resistor divider between CSREF and CSCOMP can be removed and the CSCOMP pin can be directly connected to the LLSET pin. To disable voltage positioning entirely (that is, no load line), connect LLSET to CSREF.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. In addition, the sensing gain is determined by external resistors so it can be made extremely accurate.

ACTIVE IMPEDANCE CONTROL MODE

For controlling the dynamic output voltage droop as a function of output current, a signal proportional to the total output current at the LLSET pin can be scaled to be equal to the droop impedance of the regulator times the output current. This droop voltage is then used to set the input control voltage to the system. The droop voltage is subtracted from the DAC reference input voltage directly to tell the error amplifier where the output voltage should be. This allows enhanced feed-forward response.

CURRENT CONTROL MODE AND THERMAL BALANCE

The ADP3197 has individual inputs (SW1 to SW3) for each phase, which are used for monitoring the current in each phase. This information is combined with an internal ramp to create a current balancing feedback system that has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning, described in the Output Current Sensing section.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed-forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp. External resistors can be placed in series with individual phases to create an intentional current imbalance, if desired, such as when one phase may have better cooling and can support higher currents. Resistor R_{SW1} through Resistor R_{SW3} can be used for adjusting thermal balance (see the typical application circuit in Figure 10). It is best to add these resistors during the initial design, so be sure that placeholders are provided in the layout.

To increase the current in any given phase, make R_{SWx} for that phase larger (make R_{SWx} = 0 for the hottest phase and do not change during balancing). Increasing R_{SWx} to only 500 Ω makes a substantial increase in phase current. Increase each R_{SWx} value by small amounts to achieve balance, starting with the coolest phase first.

VOLTAGE CONTROL MODE

A high gain, high bandwidth voltage mode error amplifier is used for the voltage mode control loop. The control input voltage to the positive input is set via the VID logic according to the voltages listed in Figure 6 . If load line is selected, this voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FBRTN) is tied to the output sense location with Resistor R_B and is used for sensing and controlling the output voltage at this point. A current source (equal to IREF/2) flows through RB into the FB pin and is used for setting the no load offset voltage from the VID voltage. The no load offset is positive with respect to the VID DAC. The main loop compensation is incorporated into the feedback network between FB and COMP.

CURRENT REFERENCE

The IREF pin is used to set an internal current reference. This reference current sets I_{FB}, I_{DELAY}, I_{SS}, I_{LIMIT}, and $I_{TTSENSE}$. A resistor-to-ground programs the current, based on the 1.5 V output.

$$IREF = \frac{1.5\ \text{V}}{R_{IREF}}$$

Typically, R_{IREF} is set to 100 kΩ to program IREF = 15 µA. The following currents are then equal to:

$I_{FB} = 1/2 \times (IREF) = 7.5\ \mu\text{A}$

$I_{DELAY} = IREF = 15\ \mu\text{A}$

$I_{SS(STARTUP)} = 1/4 \times (IREF) = 3.75\ \mu\text{A}$

$I_{SS(DAC)} = 5/4 \times (IREF) = 18.75\ \mu\text{A}$

$I_{LIMIT} = 2/3 \times (IREF) = 10\ \mu\text{A}$

$I_{TTSENSE} = 8 \times (IREF) = 120\ \mu\text{A}$

ENHANCED PWM MODE

Enhanced PWM mode is intended to improve the transient response of the ADP3197 to a load step-up. In previous generations of controllers, when a load step-up occurred, the controller had to wait until the next turn on of the PWM signal to respond to the load change. Enhanced PWM mode allows the controller to respond immediately when a load step-up occurs. This allows the phases to respond when the load increase transition takes place.

DELAY TIMER

The delay times for the start-up timing sequence are set with a capacitor from the DELAY pin to ground. In UVLO or when EN is logic low, the DELAY pin is held at ground. After the UVLO and EN signals are asserted, the first delay time (TD1 in Figure 7) is initiated. A current flows out of the DELAY pin to charge C_{DLY}. This current is equal to IREF, which is normally 15 µA. A comparator monitors the DELAY voltage with a threshold of 1.7 V.

The delay time is, therefore, set by the IREF current charging a capacitor from 0 V to 1.7 V. This DELAY pin is used for two delay timings (TD1 and TD3) during the start-up sequence. In addition, DELAY is used for timing the current limit latch-off, as explained in the Current Limit, Short-Circuit, and Latch-Off Protection section.

SOFT START

The soft start ramp rates for the output voltage are set up with a capacitor from the soft start (SS) pin to ground. During startup, the SS pin sources a current of 3.75 µA. After startup, when a DAC code change takes place, the SS pin sinks or sources an 18.75 µA current to control the rate at which the output voltage can transition up or down.

During startup (after TD1 and the phase detection cycle have been completed), the SS time (TD2 in Figure 7) starts. The SS pin is disconnected from GND, and the capacitor is charged up to the programmed DAC voltage by the SS amplifier, which has an output current equal to 1/4 IREF (normally 3.75 µA). The voltage at the FB pin follows the ramping voltage on the SS pin, limiting the inrush current during startup. The soft start time depends on the value of the initial DAC voltage and C_{SS}. It is important to note that the DAC code needs to be set before the ADP3197 is enabled.

Once the SS voltage is within 50 mV of the programmed DAC voltage, the power-good delay time (TD3) is started.

Once TD2 has completed the SS current changes, it is changed to 18.75 µA. If the programmed DAC code changes after startup, then the SS pin sources or sinks a current of 18.75 µA to or from the SS cap until the SS voltage is within 50 mV of the newly programmed DAC voltage.

If EN is taken low or VCC drops below UVLO, DELAY and SS are reset to ground in preparation for another soft start cycle.

Figure 8 shows typical start-up waveforms for the ADP3197.

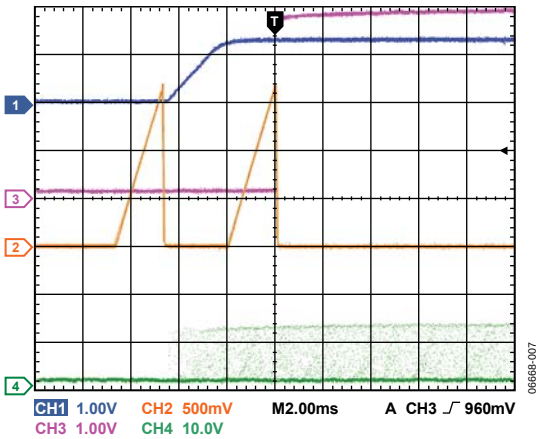


Figure 8. Typical Start-up Waveforms
Channel 1: CSREF, Channel 2: DELAY,
Channel 3: Power Good, Channel 4: Phase 1 Switch Node

CURRENT LIMIT, SHORT-CIRCUIT, AND LATCH-OFF PROTECTION

The ADP3197 compares a programmable current limit setpoint to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the ILIMIT pin to ground. During operation, the current from ILIMIT is equal to 2/3 IREF, giving 10 µA normally.

This current, through the external resistor, sets the ILIMIT voltage, which is internally scaled to give a current limit threshold of 82.6 mV/V. If the difference in voltage between CSREF and CSCOMP rises above the current limit threshold, the internal current limit amplifier controls the internal COMP voltage to maintain the average output current at the limit.

If the limit is reached and TD3 has completed, a latch-off delay time starts and the controller shuts down if the fault is not removed. The current limit delay time shares the DELAY pin timing capacitor with the start-up sequence timing. However, during current limit, the DELAY pin current is reduced to IREF/4.

A comparator monitors the DELAY voltage and shuts off the controller when the voltage reaches 1.7 V. The current limit latch-off delay time is, therefore, set by the current of IREF/4, charging the delay capacitor from 0 V to 1.7 V. This delay is four times longer than the delay time during the start-up sequence. The current limit delay time starts only after TD3 has completed. If there is a current limit during startup, the ADP3197 goes through TD1 to TD3 and then starts the latch-off time. Because the controller continues to cycle the phases during the latch-off delay time, if the short is removed before the 1.7 V threshold is reached, the controller returns to normal operation and the DELAY capacitor is reset to GND.

The latch-off function can be reset either by removing and reapplying the supply voltage to the ADP3197 or by toggling the EN pin low for a short time. To disable the short-circuit latch-off function, an external resistor should be placed in parallel with C_{DLY}.

This prevents the DELAY capacitor from charging up to the 1.7 V threshold. The addition of this resistor causes a slight increase in the delay times.

During startup, when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit controls the internal COMP voltage to the PWM comparators to 1.5 V. This limits the voltage drop across the low-side MOSFETs through the current balance circuitry.

An inherent per phase current limit protects individual phases if one or more phases stop functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage. Typical overcurrent latch-off waveforms are shown in Figure 9.

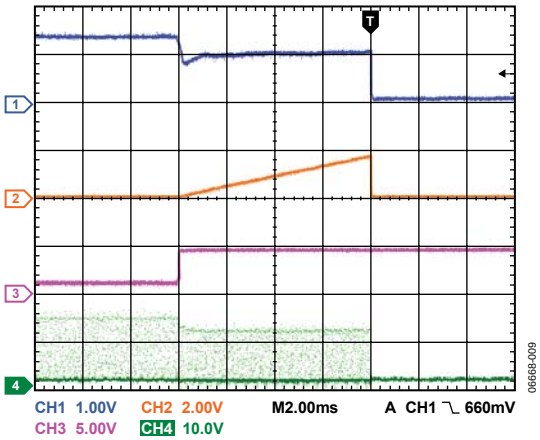


Figure 9. Overcurrent Latch-Off Waveforms Channel 1: CSREF, Channel 2: DELAY, Channel 3: COMP, Channel 4: Phase 1 Switch Node

DYNAMIC VID

The ADP3197 has the ability to respond to dynamically changing VID inputs while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as VID on-the-fly (OTF). A VID OTF can occur under either light or heavy load conditions. The processor signals the controller by changing the VID inputs in multiple steps from the start code to the finish code. This change can be positive or negative.

When a VID input changes state, the ADP3197 detects the change and ignores the DAC inputs for a minimum of 400 ns. This time prevents a false code due to logic skew while the six VID inputs are changing. Additionally, the first VID change initiates the power-good and crowbar blanking functions for a minimum of 250 µs to prevent a false power-good or crowbar event. Each VID change resets the internal timer.

POWER-GOOD MONITORING

The power-good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the nominal limits defined in the Power-Good Comparator section of the Specifications table, based on the VID voltage setting. PWRGD goes low if the output voltage is outside of this specified range.

The PWRGD circuitry also incorporates an initial turn-on delay time (TD3) based on the DELAY timer. Prior to the SS voltage reaching the programmed VID DAC voltage and the PWRGD masking time finishing, the PWRGD pin is held low. Once the SS pin is within 50 mV of the programmed DAC voltage, the capacitor on the DELAY pin begins to charge up. A comparator monitors the DELAY voltage and enables PWRGD when the voltage reaches 1.7 V. The PWRGD delay time is, therefore, set by a current of IREF charging a capacitor from 0 V to 1.7 V.

OUTPUT CROWBAR

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low-side MOSFETs) when the output voltage exceeds the upper crowbar threshold.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output over-voltage is due to a short in the high-side MOSFET, this action current limits the input supply or blows its fuse, protecting the microprocessor from being destroyed.

OUTPUT ENABLE AND UVLO

For the ADP3197 to begin switching, the input supply (VCC) to the controller must be higher than the UVLO threshold, the EN pin must be higher than its 0.85 V threshold, and the DAC code must be valid. This initiates a system start-up sequence.

If either UVLO or EN is less than its respective threshold, the ADP3197 is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and forces the PWRGD and $\overline{\text{OD}}$ signals low.

In the application circuit (see Figure 10), the $\overline{\text{OD}}$ pin should be connected to the $\overline{\text{OD}}$ inputs of the ADP3120A drivers. Grounding $\overline{\text{OD}}$ disables the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs are not disabled, a negative voltage can be generated during output due to the high current discharge of the output capacitors through the inductors.

THERMAL MONITORING

The ADP3197 includes a thermal monitoring circuit to detect when a point on the VR has exceeded two different user-defined temperatures. The thermal monitoring circuit requires an NTC thermistor to be placed between TTSENSE and GND. A fixed current of eight times IREF (normally giving 123 μA) is sourced out of the TTSENSE pin and into the thermistor. The current source is internally limited to 5 V. An internal circuit compares the TTSENSE voltage to a 0.81 V threshold and outputs an open-drain signal at the VRHOT outputs, respectively.

The VRHOT open-drain output goes high once the voltage on the TTSENSE pin goes below the VRHOT thresholds and signals the system that an overtemperature event has occurred. Because the TTSENSE voltage changes slowly with respect to time, 50 mV of hysteresis is built into these comparators. The thermal monitoring circuitry does not depend on EN and is active when UVLO is above its threshold. When UVLO is below its threshold, VRHOT is forced low.

Table 4. VID Codes

OUTPUT	VID5	VID4	VID3	VID2	VID1	VID0
1.550	0	0	0	0	0	0
1.525	0	0	0	0	0	1
1.500	0	0	0	0	1	0
1.475	0	0	0	0	1	1
1.450	0	0	0	1	0	0
1.425	0	0	0	1	0	1
1.400	0	0	0	1	1	0
1.375	0	0	0	1	1	1
1.350	0	0	1	0	0	0
1.325	0	0	1	0	0	1
1.300	0	0	1	0	1	0
1.275	0	0	1	0	1	1
1.250	0	0	1	1	0	0
1.225	0	0	1	1	0	1
1.200	0	0	1	1	1	0
1.175	0	0	1	1	1	1
1.150	0	1	0	0	0	0
1.125	0	1	0	0	0	1
1.100	0	1	0	0	1	0
1.075	0	1	0	0	1	1
1.050	0	1	0	1	0	0
1.025	0	1	0	1	0	1
1.000	0	1	0	1	1	0
0.975	0	1	0	1	1	1
0.950	0	1	1	0	0	0
0.925	0	1	1	0	0	1
0.900	0	1	1	0	1	0
0.875	0	1	1	0	1	1
0.850	0	1	1	1	0	0
0.825	0	1	1	1	0	1
0.800	0	1	1	1	1	0
0.775	0	1	1	1	1	1
0.7625	1	0	0	0	0	0
0.7500	1	0	0	0	0	1
0.7375	1	0	0	0	1	0
0.7250	1	0	0	0	1	1
0.7125	1	0	0	1	0	0
0.7000	1	0	0	1	0	1
0.6875	1	0	0	1	1	0
0.6750	1	0	0	1	1	1
0.6625	1	0	1	0	0	0
0.6500	1	0	1	0	0	1
0.6375	1	0	1	0	1	0
0.6250	1	0	1	0	1	1
0.6125	1	0	1	1	0	0
0.6000	1	0	1	1	0	1
0.5875	1	0	1	1	1	0
0.5750	1	0	1	1	1	1
0.5625	1	1	0	0	0	0
0.5500	1	1	0	0	0	1
0.5375	1	1	0	0	1	0
0.5250	1	1	0	0	1	1
0.5125	1	1	0	1	0	0
0.5000	1	1	0	1	0	1
0.4875	1	1	0	1	1	0
0.4750	1	1	0	1	1	1
0.4625	1	1	1	0	0	0
0.4500	1	1	1	0	0	1
0.4375	1	1	1	0	1	0
0.4250	1	1	1	0	1	1
0.4125	1	1	1	1	0	0
0.4000	1	1	1	1	0	1
0.3875	1	1	1	1	1	0
0.3750	1	1	1	1	1	1

TYPICAL APPLICATION CIRCUIT

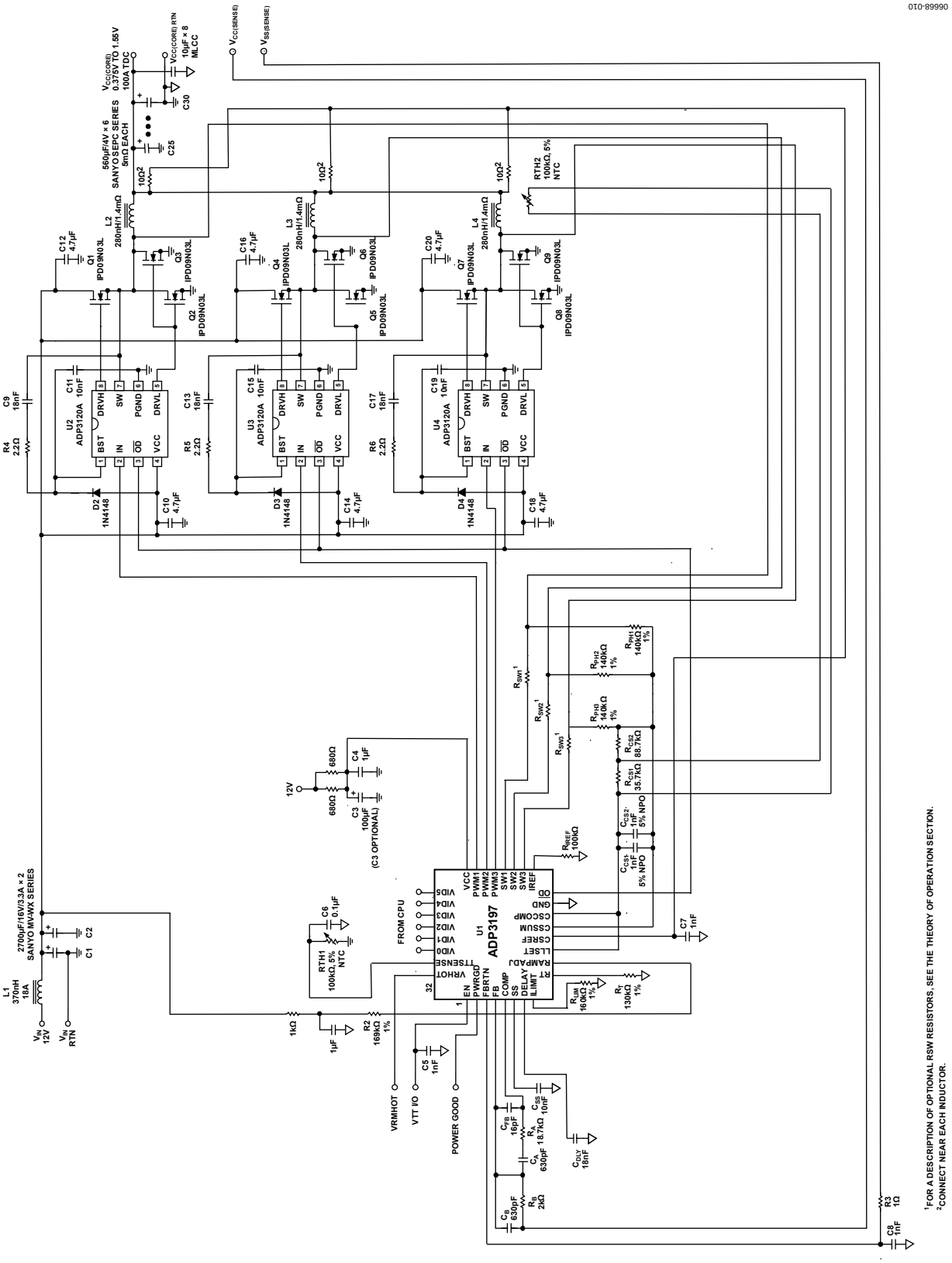


Figure 10. Typical Application of 3-Phase VR

APPLICATIONS INFORMATION

The design parameters for a typical AMD socket AM2 CPU application are as follows:

- Input voltage (V_{IN}) = 12 V
- VID setting voltage (V_{VID}) = 1.300 V
- Duty cycle (D) = 0.108
- Maximum static output voltage error ($\pm V_{SRER}$) = ±50 mV
- Maximum dynamic output voltage error ($\pm V_{DRER}$) = ±100 mV
- Error voltage allowed for controller and ripple ($\pm V_{RERR}$) = ±20 mV
- Maximum output current (I_O) = 110 A
- Maximum output current step (ΔI_O) = 70 A
- Static output droop resistance (R_O) based on
  - No load output voltage set at upper output voltage limit $V_{ONL} = V_{VID} + V_{SERR} - V_{RERR}$ = 1.330 V
  - Full load output voltage set at lower output voltage limit $V_{OFL} = V_{VID} - V_{SERR} + V_{RERR}$ = 1.270 V
  - $R_O = (V_{ONL} - V_{OFL})/I_O$ = (1.33 V – 1.27 V)/110 A = 0.545 mΩ
- Dynamic output droop resistance (R_{OD}) based on
  - Output current step to no load with output voltage set at upper output dynamic voltage limit $V_{ONLD} = V_{VID} + V_{DERR} - V_{RERR}$ = 1.380 V
  - Output voltage prior to load change (at $I_{OUT} = \Delta I_O$) $V_{OL} = V_{ONL} - (\Delta I_O \times R_O)$ = 1.292 V
  - $R_{OD} = (V_{ONLD} - V_{OL})/\Delta I_O$ = (1.380 V – 1.292 V)/70 A = 1.25 mΩ
- Number of phases (n) = 3
- Switching frequency per phase (f_{SW}) = 330 kHz

SETTING THE CLOCK FREQUENCY

The ADP3197 uses a fixed frequency control architecture. The frequency is set by an external timing resistor (R_T). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to switching losses as well as the sizes of the inductors, the input capacitors, and output capacitors. With n = 3 for three phases, a clock frequency of 1.32 MHz sets the switching frequency (f_{SW}) of each phase to 330 kHz, which represents a practical trade-off between the switching losses and the sizes of the output filter components. Figure 3 shows that to achieve a 1.32 MHz oscillator frequency, the correct value for R_T is 130 kΩ.

Alternatively, the value for R_T can be calculated using

$$R_T = \frac{1}{n \times f_{SW} \times 6\text{ pF}} \quad (1)$$

where 6 pF is the internal IC component value. For good initial accuracy and frequency stability, a 1% resistor is recommended.

SOFT START DELAY TIME

The value of C_{SS} sets the soft start time on initial power-up and, additionally, whenever the output voltage is modified by a change in the VID code. The ramp is generated with a 3.75 µA internal current source during startup and by an 18.75 µA internal current source during a VID code change. The value for C_{SS} can be found using the following equations:

During startup,

$$C_{SS} = 3.75\ \mu\text{A} \times \frac{TD2}{V_{VID}} \quad (2)$$

where:
TD2 is the desired soft start time.
V_{VID} is set by the VID inputs.

The slew rate during a VID code change is five times faster than the startup slew rate (because the internal current source is five times larger).

$$C_{SS} = 18.75\ \mu\text{A} \times \frac{TD}{\Delta V_{VID}}$$

The Advanced Micro Devices, AMD specification calls for a minimum slew rate of 2 mV/µs for VID code changes. For example, if the VID code changes from 1.0 V to 1.2 V, then TD is 10 ms. This means C_{SS} equals 9.375 nF. The closest standard capacitor value available is 10 nF.

CURRENT-LIMIT LATCH-OFF DELAY TIMES

The start-up and current-limit delay times are determined by the capacitor connected to the DELAY pin. The first step is to set C_{DLY} for the TD1 and TD3 delay times (see Figure 7). The DELAY ramp (I_{DELAY}) is generated using a 15 µA internal current source. The value for C_{DLY} can be approximated using

$$C_{DLY} = I_{DELAY} \times \frac{TD(x)}{V_{DELAY(TH)}} \quad (3)$$

where *TD(x)* is the desired delay time for TD1 and TD3.

The DELAY threshold voltage ($V_{DELAY(TH)}$) is given as 1.7 V. In this example, 2 ms is chosen for all delay times, which meets the AMD specifications (of not greater than 6 ms). Solving for C_{DLY} gives a value of 17.6 nF. The closest standard value for C_{DLY} is 18 nF.

When the ADP3197 enters current limit, the internal current source changes from 15 µA to 3.75 µA. This makes the latch-off delay time four times longer than the start-up delay time. Longer latch-off delay times can be achieved by placing a resistor in parallel with C_{DLY}.

INDUCTOR SELECTION

The choice of inductance for the inductor determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and conduction losses in the MOSFETs. However, using smaller inductors allows the converter to meet a specified peak-to-peak transient deviation with less total output capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but more output capacitance is required to meet the same peak-to-peak transient deviation.

In any multiphase converter, a practical value for the peak-to-peak inductor ripple current is less than 50% of the maximum dc current in the same inductor. Equation 4 shows the relationship between the inductance, oscillator frequency, and peak-to-peak ripple current in the inductor.

$$I_R = \frac{V_{VID} \times (1 - D)}{f_{SW} \times L} \quad (4)$$

Equation 5 can be used to determine the minimum inductance based on a given output ripple voltage.

$$L \geq \frac{V_{VID} \times R_{OD} \times (1 - (n \times D))}{f_{SW} \times V_{RIPPLE}} \quad (5)$$

Solving Equation 5 for a 10 mV p-p output ripple voltage yields

$$L \geq \frac{1.3\ \text{V} \times 1.25\ \text{m}\Omega \times (1 - 0.324)}{330\ \text{kHz} \times 10\ \text{mV}} = 333\ \text{nH}$$

If the resulting ripple voltage is less than what it is designed for, the inductor can be made smaller until the ripple value is met. This allows optimal transient response and minimum output decoupling.

The smallest possible inductor should be used to minimize the number of output capacitors. For this example, choosing a 400 nH inductor is a good starting point and gives a calculated ripple current of 8.78 A. The inductor should not saturate at the peak current of 41.06 A and should be able to handle the sum of the power dissipation caused by the average current of 36.7 A in the winding and core loss.

Another important factor in the inductor design is the dc resistance (DCR), which is used for measuring the phase currents. A large DCR may cause excessive power losses, though too small a value may lead to increased measurement error. A good rule is to have the DCR (R_L) be about 1 to 1½ times the droop resistance (R_{OD}). This example uses an inductor with a DCR of 1.875 mΩ.

Designing an Inductor

Once the inductance and DCR are known, the next step is either to design an inductor or find a standard inductor that comes as close as possible to meeting the overall design goals. It is also important to have the inductance and DCR tolerance specified to control the accuracy of the system. Reasonable tolerances most manufacturers can meet are 15% inductance and 7% DCR at room temperature.

The first decision in designing the inductor is choosing the core material. Several possibilities for providing low core loss at high frequencies include the powder cores (from Micrometals, Inc., for example, or Kool Mu® from Magnetics) and the gapped soft ferrite cores (for example, 3F3 or 3F4 from Philips). Low frequency powdered iron cores should be avoided due to their high core loss, especially when the inductor value is relatively low and the ripple current is high.

The best choice for a core geometry is a closed-loop type such as a potentiometer core (PQ, U, or E core) or toroid. A good compromise between price and performance is a core with a toroidal shape.

Many useful magnetics design references are available for quickly designing a power inductor, such as

- Intusoft Magnetic Designer Software
- *Designing Magnetic Components for High Frequency Dc-Dc Converters* by William T. McLyman, Kg Magnetics, Inc., ISBN 1883107008

Selecting a Standard Inductor

The following power inductor manufacturers can provide design consultation and deliver power inductors optimized for high power applications upon request.

- Coilcraft, Inc.
- Coiltronics/Div of Cooper Bussmann
- Sumida Corporation

CURRENT SENSE AMPLIFIER

Most designs require the regulator output voltage, measured at the CPU pins, to droop when the output current increases. The specified voltage droop corresponds to a dc output resistance (R_O), also referred to as a load line. The ADP3197 has the flexibility of adjusting R_O independent of current-limit or compensation components, and it can also support CPUs that do not require a load line.

For designs requiring a load line, the impedance gain of the CS amplifier (R_{CSA}) must be greater than or equal to the load line. All designs, whether they have a load line or not, should keep $R_{CSA} \geq 1$ mΩ.

The output current is measured by summing the voltage across each inductor and passing the signal through a low-pass filter. This summer filter is the CS amplifier configured with Resistors $R_{PH(x)}$ (summers) and Resistor R_{CS} and Capacitor C_{CS} (filters). The impedance gain of the regulator is set by the following equations where R_L is the DCR of the output inductors:

$$R_{CSA} = \frac{R_{CS}}{R_{PH(x)}} \times R_L \quad (6)$$

$$C_{CS} = \frac{L}{R_L \times R_{CS}} \quad (7)$$

The user has the flexibility to choose either R_{CS} or $R_{PH(x)}$.

However, it is best to select R_{CS} equal to 100 kΩ, and then solve for $R_{PH(x)}$ by rearranging Equation 6. Here, R_{CSA} = 1 mΩ because this is equal to the design load line.

$$R_{PH(x)} = \frac{R_L}{R_{CSA}} \times R_{CS}$$

$$R_{PH(x)} = \frac{1.875\ \text{m}\Omega}{1.0\ \text{m}\Omega} \times 100\ \text{k}\Omega = 187.5\ \text{k}\Omega$$

Next, use Equation 7 to solve for C_{CS}.

$$C_{CS} = \frac{400\ \text{nH}}{1.875\ \text{m}\Omega \times 100\ \text{k}\Omega} = 2\ \text{nF}$$

It is best to have a dual location for C_{CS} in the layout so that standard values can be used in parallel to get as close as possible to the desired value. For best accuracy, C_{CS} should be a 5% or 10% NPO capacitor. This example uses a 5% combination for C_{CS} of two 1 nF capacitors in parallel. Recalculating R_{CS} and $R_{PH(X)}$ using this capacitor combination yields 110 kΩ and 140 kΩ. The closest standard 1% value for $R_{PH(X)}$ is 187 kΩ.

INDUCTOR DCR TEMPERATURE CORRECTION

When the inductor DCR is used as the sense element and copper wire is used as the source of the DCR, the user needs to compensate for temperature changes of the inductor's winding. Fortunately, copper has a well-known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite and equal percentage change in resistance to that of the wire, it cancels the temperature variation of the inductor DCR. Due to the nonlinear nature of NTC thermistors, Resistor R_{CS1} and Resistor R_{CS2} are needed. See Figure 11 to linearize the NTC and produce the desired temperature tracking.

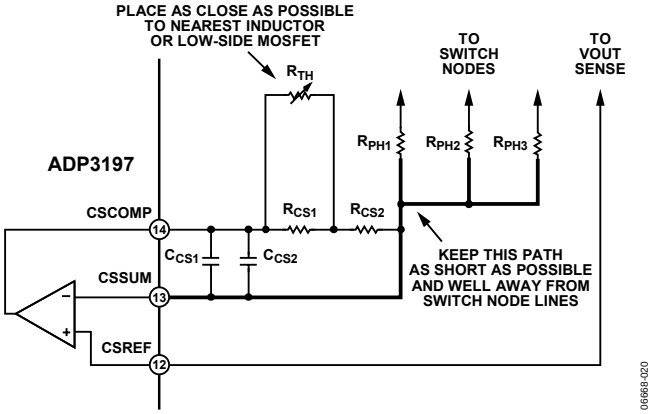


Figure 11. Temperature Compensation Circuit Values

The following procedure and equations yield values to use for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value:

1. Select an NTC based on type and value. Because the value is unknown, use a thermistor with a value close to R_{CS}. The NTC should also have an initial tolerance of greater than 5%.
2. Based on the type of NTC, find its relative resistance value at two temperatures. The temperatures that work well are 50°C and 90°C. These resistance values are called A ($R_{TH(50°C)}$)/$R_{TH(25°C)}$) and B ($R_{TH(90°C)}$)/$R_{TH(25°C)}$). The relative value of the NTC is always 1 at 25°C.
3. Find the relative value of R_{CS} required for each of these temperatures. The relative value of R_{CS} is based on the percentage change needed, which in this example is initially 0.39%/°C. These temperatures are called r_1.

   $r_1 = 1/(1 + TC \times (T_1 - 25°C))$

   and r_2

   $r_2 = 1/(1 + TC \times (T_2 - 25°C))$

   where:
   TC = 0.0039 for copper.
   T_1 = 50°C.
   T_2 = 90°C.

   From this, r_1 = 0.9112 and r_2 = 0.7978.
4. Compute the relative values for R_{CS1}, R_{CS2}, and R_{TH} using

$$R_{CS2} = \frac{(A-B) \times r_1 \times r_2 - A \times (1-B) \times r_2 + B \times (1-A) \times r_1}{A \times (1-B) \times r_1 - B \times (1-A) \times r_2 - (A-B)} \quad (8)$$

$$R_{CS1} = \frac{(1-A)}{\dfrac{1}{1-R_{CS2}} - \dfrac{A}{r_1 - R_{CS2}}} \quad (9)$$

$$R_{TH} = \frac{1}{\dfrac{1}{1-R_{CS2}} - \dfrac{1}{R_{CS1}}} \quad (10)$$

   Calculate $R_{TH} = r_{TH} \times R_{CS}$, then select the closest value of thermistor available. Also, compute a scaling factor (K) based on the ratio of the actual thermistor value used relative to the computed one.

$$K = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad (11)$$

5. Calculate values for R_{CS1} and R_{CS2} using Equation 12 and Equation 13.

$$R_{CS1} = R_{CS} \times K \times R_{CS1} \quad (12)$$

$$R_{CS2} = R_{CS} \times ((1 - K) + (K \times R_{CS2})) \quad (13)$$

In this example, R_{CS} is calculated to be 114 kΩ. Look for an available 100 kΩ thermistor, 0603 size. One such thermistor is the Vishay NTHS0603N01N1003JR NTC thermistor with A = 0.3602 and B = 0.09174. From these values, r_{CS1} = 0.3795, r_{CS2} = 0.7195, and r_{TH} = 1.075.

Solving for R_{TH} yields 122.55 kΩ, so 100 kΩ is chosen, making K = 0.816. Next, find R_{CS1} and R_{CS2} to be 35.3 kΩ and 87.9 kΩ. Finally, choose the closest 1% resistor values, which yields a choice of 35.7 kΩ and 88.7 kΩ.

Load Line Setting

For load line values greater than 1 mΩ, R_{CSA} can be set equal to R_O, and the LLSET pin can be directly connected to the CSCOMP pin. When the load line value needs to be less than 1 mΩ, two additional resistors are required. Figure 12 shows the placement of these resistors.

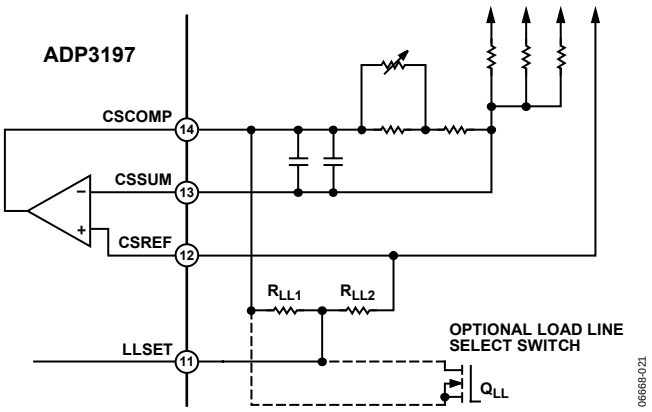


Figure 12. Load Line Setting Resistors

The two resistors, R_{LL1} and R_{LL2}, set up a divider between the CSCOMP pin and CSREF pin. This resistor divider is input into the LLSET pin to set the load line slope R_O of the VR according to the following equation:

$$R_O = \frac{R_{LL2}}{R_{LL1} + R_{LL2}} \times R_{CSA} \tag{14}$$

The resistor values for R_{LL1} and R_{LL2} are limited by two factors.

- The minimum value is based on the loading of the CSCOMP pin. This pin's drive capability is 500 µA, and the majority of this should be allocated to the CSA feedback. If the current through R_{LL1} and R_{LL2} is limited to 10% of this (50 µA), the following limit can be placed for the minimum value for R_{LL1} and R_{LL2}:

$$R_{LL1} + R_{LL2} \geq \frac{I_{LIM} \times R_{CSA}}{50 \times 10^{-6}} \tag{15}$$

  Here, I_{LIM} is the current-limit current, which is the maximum signal level that the CSA responds to.

- The maximum value is based on minimizing induced dc offset errors based on the bias current of the LLSET pin. To keep the induced dc error less than 1 mV, which makes this error statistically negligible, place the following limit to the parallel combination of R_{LL1} and R_{LL2}:

$$\frac{R_{LL1} \times R_{LL2}}{R_{LL1} + R_{LL2}} \leq \frac{1 \times 10^{-3}}{120 \times 10^{-9}} = 8.33\ \text{k}\Omega \tag{16}$$

When selecting the resistors, it is best to minimize their values to reduce the noise and parasitic susceptibility of the feedback path.

By combining Equation 16 with Equation 14 and selecting minimum values for the resistors, the following equations result:

$$R_{LL2} = \frac{I_{LIM} \times R_O}{50\ \mu\text{A}} \tag{17}$$

$$R_{LL1} = \left(\frac{R_{CSA}}{R_O} - 1\right) \times R_{LL2} \tag{18}$$

Therefore, both R_{LL1} and R_{LL2} need to be in parallel and equal to less than 8.33 kΩ.

Another useful feature for some VR applications is the ability to select different load lines. Figure 12 shows an optional MOSFET switch that allows this feature. Here, design for $R_{CSA} = R_{O(MAX)}$ (selected with Q_{LL} on) and then use Equation 14 to set $R_O = R_{O(MIN)}$ (selected with Q_{LL} off).

For this design, $R_{CSA} = R_O = 1$ mΩ. As a result, connect LLSET directly to CSCOMP; the R_{LL1} and R_{LL2} resistors are not needed.

OUTPUT OFFSET

The Advanced Micro Devices, AMD specification requires that at no load the nominal output voltage of the regulator be offset to a value higher than the nominal voltage corresponding to the VID code. The offset is set by a constant current source flowing into the FB pin (I_{FB}) and flowing through R_B. The value of R_B can be found using Equation 19.

$$R_B = \frac{V_{ONL} - V_{VID}}{I_{FB}}$$

$$R_B = \frac{1.33\ \text{V} - 1.3\ \text{V}}{15\ \mu\text{A}} = 4.00\ \text{k}\Omega \tag{19}$$

The closest standard 1% resistor value is 4.00 kΩ.

C_{OUT} SELECTION

The required output decoupling for the regulator is typically recommended by AMD for various processors and platforms. Use simple design guidelines to determine the requirements. These guidelines are based on having both bulk capacitors and ceramic capacitors in the system.

First, select the total amount of ceramic capacitance. This is based on the number and type of capacitor used. The best location for ceramic capacitors is inside the socket. Other capacitors can be placed along the outer edge of the socket.

Combined ceramic values of 30 µF to 100 µF are recommended, usually made up of multiple 10 µF or 22 µF capacitors. Select the number of ceramics and find the total ceramic capacitance (Cz).

Next, there is an upper limit imposed on the total amount of bulk capacitance (C_X) when the user considers the VID on-the-fly voltage stepping of the output (voltage step V_V in time t_V with an error of V_{ERR}).

A lower limit is based on meeting the capacitance for load release for a given maximum load step (ΔI_O) and a maximum allowable overshoot. The total amount of load release voltage is given as $\Delta V_O = \Delta I_O \times R_{OD}$.

$$C_{X(MIN)} \geq \left(\frac{L \times \Delta I_O}{n \times R_{OD} \times V_{VID}} - C_Z \right) \quad (20)$$

$$C_{X(MAX)} \leq \quad (21)$$

$$\frac{L}{nK^2 R_O^2} \times \frac{V_V}{V_{VID}} \times \left(\sqrt{1 + \left(t_V \frac{V_{VID}}{V_V} \times \frac{nKR_O}{L} \right)^2} - 1 \right) - C_Z$$

where $K = -1n\left(\frac{V_{ERR}}{V_V}\right)$

To meet the conditions of these equations and transient response, the ESR of the bulk capacitor bank (R_X) should be less than two times the dynamic input droop resistance (R_{OD}). If $C_{X(MIN)}$ is larger than $C_{X(MAX)}$, the system cannot meet the VID on-the-fly specification and may require the use of a smaller inductor or more phases (and may have to increase the switching frequency to keep the output ripple the same).

This example uses 18, 10 µF 1206 MLC capacitors (C_Z = 180 µF). The VID on-the-fly step change is 1.3 V to 0.6 V (making V_V = 0.7 V) in 100 µs with a settling error of 2.5 mV. ≈

The maximum allowable load release overshoot for this example is 3%. Therefore, solving for the bulk capacitance yields

$$C_{X(MIN)} \leq \left(\frac{400\ \text{nH} \times 70\ \text{A}}{3 \times 1.25\,\text{m}\Omega \times 1.3\ \text{V}} - 180\ \mu\text{F} \right) = 5.564\ \text{mF} \quad (22)$$

$$C_{X(MAX)} \leq \frac{400\ \text{nH} \times 700\ \text{mV}}{3 \times 3.5^2 \times (1.25\ \text{m}\Omega)^2 \times 1.3\ \text{V}} \times$$

$$\left(\sqrt{1 + \left(\frac{100\ \mu\text{s} \times 1.3\ \text{V} \times 3 \times 3.5 \times 1.25\ \text{m}\Omega}{700\ \text{mV} \times 400\ \text{nH}} \right)^2} - 1 \right) -$$

$$180\ \mu\text{F} = 19.23\ \text{mF}$$

where K = 3.5.

Using 10, 560 µF Al-Poly capacitors with a typical ESR of 6 mΩ each yields C_X = 5.6 mF with an R_X = 0.6 mΩ.

One last check should be made to ensure that the ESL of the bulk capacitors (L_X) is low enough to limit high frequency ringing during a load change.

This is tested using

$$L_X \leq C_Z \times R_O{}^2 \times Q^2$$
$$L_X \leq 180\ \mu\text{F} \times (1.25\ \text{m}\Omega)^2 \times 2 = 562\ \text{pH} \quad (23)$$

where Q^2 is limited to 2 to ensure a critically damped system.

In this example, L_X is approximately 240 pH for the 10 Al-Poly capacitors, which satisfies this limitation. If the L_X of the chosen bulk capacitor bank is too large, the number of ceramic capacitors needs to be increased, or lower ESL bulks must be used if there is excessive undershoot during a load transient.

For this multimode control technique, all ceramic designs can be used providing the conditions of Equation 20 through Equation 23 are satisfied.

POWER MOSFETS

For this example, the N-channel power MOSFETs have been selected for one high-side switch and two low-side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. The minimum gate drive voltage (the supply voltage to the ADP3120A) dictates whether standard threshold or logic-level threshold MOSFETs must be used. With V_{GATE} equal to approximately 10 V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5 V) are recommended.

The maximum output current (I_O) determines the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. With the ADP3197, currents are balanced between phases; thus, the current in each low-side MOSFET is the output current divided by the total number of MOSFETs (n_{SF}).

With conduction losses being dominant, Equation 24 shows the total power that is dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and average total output current (I_O).

$$P_{SF} = (1 - D) \times \left[\left(\frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left(\frac{n\, I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad (24)$$

Knowing the maximum output current being designed for and the maximum allowed power dissipation, the user can find the required $R_{DS(ON)}$ for the MOSFET. For D-Pak MOSFETs up to an ambient temperature of 50°C, a safe limit for P_{SF} is 1 W to 1.5 W at 120°C junction temperature.

Thus, for this example (100 A maximum), $R_{DS(SF)}$ (per MOSFET) is less than 7.5 mΩ. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C. As a result, users need to account for these conditions when selecting a low-side MOSFET. This example uses two lower-side MOSFETs at 4.8 mΩ, each at 120°C.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input needs to be small (less than 10% is recommended) to prevent accidental turn-on of the synchronous MOSFETs when the switch node goes high.

Also, the time to switch the synchronous MOSFETs off should not exceed the nonoverlap dead time of the MOSFET driver (40 ns typical for the ADP3110A). The output impedance of the driver is approximately 2 Ω and the typical MOSFET input gate resistances are about 1 Ω to 2 Ω. Therefore, a total gate capacitance of less than 6000 pF should be adhered to.

Because two MOSFETs are in parallel, the input capacitance for each synchronous MOSFET should be limited to 3000 pF.

The high-side (main) MOSFET must be able to handle two main power dissipation components: conduction and switching losses. The switching loss is related to the amount of time it takes for the main MOSFET to turn on and off and to the current and voltage being switched. Basing the switching speed on the rise and fall time of the gate driver impedance and MOSFET input capacitance, Equation 25 provides an approximate value for the switching loss per main MOSFET, where n_{MF} is the total number of main MOSFETs.

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \quad (25)$$

where:
R_G is the total gate resistance (2 Ω for the ADP3110A and about 1 Ω for typical high speed switching MOSFETs, making R_G = 3 Ω).
C_{ISS} is the input capacitance of the main MOSFET.

Adding more main MOSFETs (n_{MF}) does not help the switching loss per MOSFET because the additional gate capacitance slows switching. Use lower gate capacitance devices to reduce switching loss.

The conduction loss of the main MOSFET is given by the following, where $R_{DS(MF)}$ is the on resistance of the MOSFET:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad (26)$$

Typically, for main MOSFETs, the highest speed (low C_{ISS}) device is preferred, but these usually have higher on resistance. Select a device that meets the total power dissipation (about 1.5 W for a single D-Pak) when combining the switching and conduction losses.

For this example, an NTD40N03L is selected as the main MOSFET (six total; n_{MF} = 6), with C_{ISS} = 584 pF (maximum) and $R_{DS(MF)}$ = 19 mΩ (maximum at T_J = 120°C). An NTD110N02L is selected as the synchronous MOSFET (six total; n_{SF} = 6), with C_{ISS} = 2710 pF (maximum) and $R_{DS(SF)}$ = 4.8 mΩ (maximum at T_J = 120°C). The synchronous MOSFET C_{ISS} is less than 3000 pF, satisfying this requirement.

Solving for the power dissipation per MOSFET at I_O = 100 A and I_R = 12.55 A yields 958 mW for each synchronous MOSFET and 872 mW for each main MOSFET. A guideline to follow is to limit the MOSFET power dissipation to 1 W. The values calculated in Equation 25 and Equation 26 comply with this guideline.

Finally, consider the power dissipation in the driver for each phase. This is best expressed as Q_G for the MOSFETs and is given by Equation 27, where Q_{GMF} is the total gate charge for each main MOSFET and Q_{GSF} is the total gate charge for each synchronous MOSFET.

$$P_{DRV} = \left[\frac{f_{SW}}{2 \times n} \times \left(n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF} \right) + I_{CC} \right] \times V_{CC} \quad (27)$$

Also shown is the standby dissipation factor ($I_{CC} \times V_{CC}$) of the driver. For the ADP3110A, the maximum dissipation should be less than 400 mW. In this example, with I_{CC} = 7 mA, Q_{GMF} = 5.8 nC, and Q_{GSF} = 48 nC, there is 297 mW in each driver, which is below the 400 mW dissipation limit. See the ADP3110A data sheet for more details.

RAMP RESISTOR SELECTION

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. Equation 28 is used for determining the optimum value.

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \quad (28)$$

$$R_R = \frac{0.2 \times 400\ \text{nH}}{3 \times 5 \times 2.4\ \text{m}\Omega \times 5\ \text{pF}} = 444\ \text{k}\Omega$$

where:
A_R is the internal ramp amplifier gain.
A_D is the current balancing amplifier gain.
R_{DS} is the total low-side MOSFET on resistance.
C_R is the internal ramp capacitor value.

The internal ramp voltage magnitude can be calculated by using

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad (29)$$

$$V_R = \frac{0.2 \times (1 - 0.108) \times 1.3\ \text{V}}{444\ \text{k}\Omega \times 5\ \text{pF} \times 330\ \text{kHz}} = 317\ \text{mV}$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and noise rejection improve, but transient degrades. Likewise, if the ramp is made smaller, transient response improves at the sacrifice of noise rejection and stability.

The factor of 3 in the denominator of Equation 28 sets a ramp size that gives an optimal balance for good stability, transient response, and thermal balance.

COMP PIN RAMP

A ramp signal on the COMP pin is due to the droop voltage and output voltage ramps. This ramp amplitude adds to the internal ramp to produce the following overall ramp signal at the PWM input:

$$V_{RT} = \frac{V_R}{\left(1 - \frac{2 \times (1 - n \times D)}{n \times f_{SW} \times C_X \times R_O}\right)} \quad (30)$$

In this example, the overall ramp signal is 0.46 V. However, if the ramp size is smaller than 0.5 V, increase the ramp size to at least 0.5 V by decreasing the ramp resistor for noise immunity. Because there is only 0.46 V initially, a ramp resistor value of 444 kΩ is chosen for this example, yielding an overall ramp of 0.51 V.

CURRENT-LIMIT SETPOINT

To select the current-limit setpoint, first find the resistor value for R_{LIM}. The current-limit threshold for the ADP3197 is set with a constant current source flowing out of the ILIMIT pin, which sets up a voltage (V_{LIM}) across R_{LIM} with a gain of 82.6 mV/V (A_{LIM}). Thus, increasing R_{LIM} now increases the current limit. R_{LIM} can be found using

$$R_{LIM} = \frac{V_{CL}}{A_{LIM} \times I_{ILIMIT}} = \frac{I_{LIM} \times R_{CSA}}{82.6\ \text{mV}} \times R_{REF} \quad (31)$$

Here, I_{LIM} is the peak average current limit for the supply output. The peak average current is the dc current limit plus the output ripple current. In this example, choosing a dc current limit of 159 A and having a ripple current of 12.55 A gives an I_{LIM} of 171.55 A. This results in an R_{LIM} = 207.6 kΩ, for which 205 kΩ is chosen as the nearest 1% value.

The per-phase initial duty cycle limit and peak current during a load step are determined by

$$D_{MAX} = D \times \frac{V_{COMP(MAX)} - V_{BIAS}}{V_{RT}} \quad (32)$$

$$I_{PHMAX} \cong \frac{D_{MAX}}{f_{SW}} \times \frac{(V_{IN} - V_{VID})}{L} \quad (33)$$

For the ADP3197, the maximum COMP voltage ($V_{COMP(MAX)}$) is 4.0 V, and the COMP pin bias voltage (V_{BIAS}) is 1.1 V. In this example, the maximum duty cycle is 0.61 and the peak current is 62 A.

The limit of the peak per-phase current described previously during the secondary current limit is determined by

$$I_{PHLIM} \cong \frac{V_{COMP(CLAMPED)} - V_{BIAS}}{A_D \times R_{DS(MAX)}} \quad (34)$$

For the ADP3197, the current balancing amplifier gain (A_D) is 5 and the clamped COMP pin voltage is 2 V. Using an $R_{DS(MAX)}$ of 2.8 mΩ (low-side on resistance at 150°C) results in a per-phase peak current limit of 64 A. This current level can be reached only with an absolute short at the output, and the current-limit latch-off function shuts down the regulator before overheating can occur.

FEEDBACK LOOP COMPENSATION DESIGN

Optimized compensation of the ADP3197 allows the best possible response of the regulator output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc, and equal to the static output droop resistance (R_O). With the resistive output impedance, the output voltage droops in proportion to the load current at any load current slew rate. This ensures optimal positioning and minimizes the output decoupling.

Because of the multimode feedback structure of the ADP3197, the feedback compensation must be set to make the converter output impedance work in parallel with the output decoupling to make the load look entirely resistive. Compensation is needed for several poles and zeros created by the output inductor and the decoupling capacitors (output filter).

A type-three compensator on the voltage feedback is adequate for proper compensation of the output filter. Equation 35 to Equation 39 are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects (see the Tuning the ADP3197 section).

Computing the Time Constants

First, compute the time constants for all the poles and zeros in the system using Equation 35 to Equation 39.

$$R_E = n \times R_O + A_D \times R_{DS} + \frac{R_L \times V_{RT}}{V_{VID}} + \frac{2 \times L \times (1 - n \times D) \times V_{RT}}{n \times C_X \times R_O \times V_{VID}}$$

$$R_E = 4 \times 1\ \text{m}\Omega + 5 \times 2.4\ \text{m}\Omega + \frac{1.4\ \text{m}\Omega \times 0.51\ \text{V}}{1.3\ \text{V}} + \frac{2 \times 320\ \text{nH} \times (1 - 0.432) \times 0.51\ \text{V}}{4 \times 5.6\ \text{mF} \times 1\ \text{m}\Omega \times 1.3\ \text{V}} = 22.9\ \text{m}\Omega \quad (35)$$

$$T_A = C_X \times (R_O - R') + \frac{L_X}{R_O} \times \frac{R_O - R'}{R_X} = 5.6\ \text{mF} \times (1\ \text{m}\Omega - 0.5\ \text{m}\Omega) + \frac{240\ \text{pH}}{1\ \text{m}\Omega} \times \frac{1\ \text{m}\Omega - 0.5\ \text{m}\Omega}{0.6\ \text{m}\Omega} = 3.00\ \mu\text{s} \quad (36)$$

$$T_B = (R_X + R' - R_O) \times C_X = (0.6\ \text{m}\Omega + 0.5\ \text{m}\Omega - 1\ \text{m}\Omega) \times 5.6\ \text{mF} = 560\ \text{ns} \quad (37)$$

$$T_C = \frac{V_{RT} \times \left(L - \frac{A_D \times R_{DS}}{2 \times f_{SW}}\right)}{V_{VID} \times R_E} = \frac{0.51\ \text{V} \times \left(320\ \text{nH} - \frac{5 \times 2.4\ \text{m}\Omega}{2 \times 330\ \text{kHz}}\right)}{1.3\ \text{V} \times 22.9\ \text{m}\Omega} = 5.17\ \mu\text{s} \quad (38)$$

$$T_D = \frac{C_X \times C_Z \times R_O^2}{C_X \times (R_O - R') + C_Z \times R_O} = \frac{5.6\ \text{mF} \times 180\ \mu\text{F} \times (1\ \text{m}\Omega)^2}{5.6\ \text{mF} \times (1\ \text{m}\Omega - 0.5\ \text{m}\Omega) + 180\ \mu\text{F} \times 1\ \text{m}\Omega} = 338\ \text{ns} \quad (39)$$

where:

R' is the PCB resistance from the bulk capacitors to the ceramics.
R_{DS} is the total low-side MOSFET on resistance per phase.
$A_D = 5$.
$V_{RT} = 0.51$ V.
$R' \approx 0.5$ mΩ (assuming a 4-layer, 1 oz motherboard).
$L_X = 240$ pH for the 10 Al-Poly capacitors.

The compensation values can then be solved using

$$C_A = \frac{n \times R_O \times T_A}{R_E \times R_B} = \frac{4 \times 1\ \text{m}\Omega \times 3.00\ \mu\text{s}}{22.9\ \text{m}\Omega \times 1.00\ \text{k}\Omega} = 524\ \text{pF} \quad (40)$$

$$R_A = \frac{T_C}{C_A} = \frac{5.17\ \mu\text{s}}{524\ \text{pF}} = 9.87\ \text{k}\Omega \quad (41)$$

$$C_B = \frac{T_B}{R_B} = \frac{560\ \text{ns}}{1.00\ \text{k}\Omega} = 560\ \text{pF} \quad (42)$$

$$C_{FB} = \frac{T_D}{R_A} = \frac{338\ \text{ns}}{9.87\ \text{k}\Omega} = 34.2\ \text{pF} \quad (43)$$

These are the starting values prior to tuning the design that account for layout and other parasitic effects (see the Tuning the ADP3197 section). The final values selected after tuning are

$C_A = 560$ pF

$R_A = 10.0$ kΩ

$C_B = 560$ pF

$C_{FB} = 27$ pF

C_{IN} SELECTION AND INPUT CURRENT di/dt REDUCTION

In continuous inductor current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to n × V_{OUT}/V_{IN} and an amplitude of one-nth the maximum output current. To prevent large voltage transients, a low ESR input capacitor, sized for the maximum rms current, must be used. The maximum rms capacitor current is given by

$$I_{CRMS} = D \times I_O \times \sqrt{\frac{1}{N \times D} - 1} \tag{44}$$

$$I_{CRMS} = 0.108 \times 110\text{ A} \times \sqrt{\frac{1}{3 \times 0.108} - 1} = 17.2\text{ A}$$

The capacitor manufacturer's ripple-current ratings are often based on only 2000 hours of life. As a result, it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors can be placed in parallel to meet size or height requirements in the design. In this example, the input capacitor bank is formed by three 2700 µF, 16 V aluminum electrolytic capacitors and eight 4.7 µF ceramic capacitors.

To reduce the input current di/dt to a level below the recommended maximum of 0.1 A/µs, an additional small inductor (L > 370 nH at 18 A) should be inserted between the converter and the supply bus. This inductor also acts as a filter between the converter and the primary power source.

THERMAL MONITOR DESIGN

A thermistor is used on the TTSENSE input of the ADP3197 for monitoring the temperature of the VR. A constant current of 123 µA is sourced out of this pin and runs through a thermistor network such as the one shown in Figure 13.

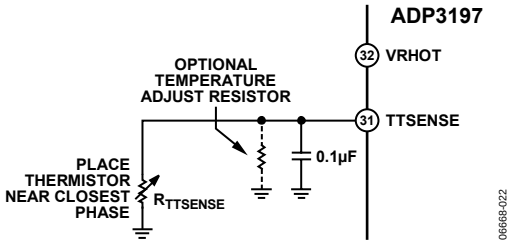


Figure 13. VR Thermal Monitor Circuit

A voltage is generated from this current through the thermistor and sensed inside the IC. When the voltage reaches 0.71 V, the VRHOT is set. This corresponds to $R_{TTSENSE}$ value of 6.58 kΩ.

These values correspond to a thermistor temperature of ~100°C and ~110°C when using the same type of 100 kΩ NTC thermistor used in the current sense amplifier.

An additional fixed resistor in parallel with the thermistor allows tuning of the trip point temperatures to match the hottest temperature in the VR, when the thermistor itself is directly sensing a proportionately lower temperature.

Setting this resistor value is best accomplished with a variable resistor during thermal validation and then fixing this value for the final design.

Additionally, a 0.1 µF capacitor should be used for filtering noise.

SHUNT RESISTOR DESIGN

The ADP3197 uses a shunt to generate 5 V from the 12 V supply range. A trade-off can be made between the power dissipated in the shunt resistor and the UVLO threshold. Figure 14 shows the typical resistor value needed to realize certain UVLO voltages. It also gives the maximum power dissipated in the shunt resistor for these UVLO voltages.

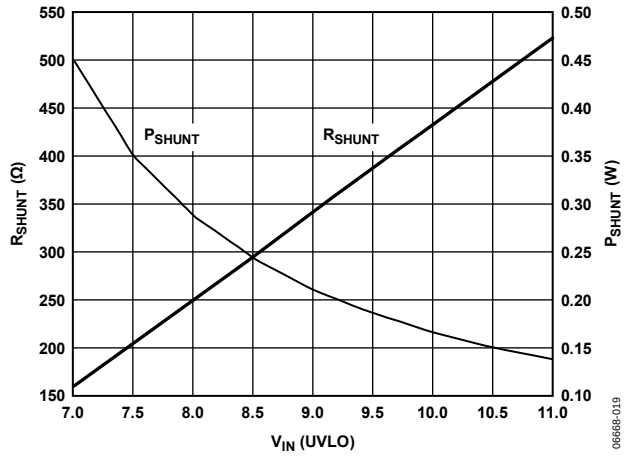


Figure 14. Typical Shunt Resistor Value and Power Dissipation for Different UVLO Voltage

The maximum power dissipated is calculated using Equation 45.

$$P_{MAX} = \frac{\left(V_{IN(MAX)} - V_{CC(MIN)}\right)^2}{R_{SHUNT}} \tag{45}$$

where:

$V_{IN(MAX)}$ is the maximum voltage from the 12 V input supply (if the 12 V input supply is 12 V ± 5%, $V_{IN(MAX)}$ = 12.6 V; if the 12 V input supply is 12 V ± 10%, $V_{IN(MAX)}$ = 13.2 V).

$V_{CC(MIN)}$ is the minimum V_{CC} voltage of the ADP3197. This is specified as 4.75 V.

R_{SHUNT} is the shunt resistor value.

The CECC standard specification for power rating in surface mount resistors is: 0603 = 0.1 W, 0805 = 0.125 W, 1206 = 0.25 W.

TUNING THE ADP3197

1. Build a circuit based on the compensation values computed from the design spreadsheet.
2. Hook up the dc load to the circuit, turn it on, and verify its operation. Also, check for jitter at no load and full load.

DC Load Line Setting

3. Measure the output voltage at no load (V_{NL}). Verify that it is within tolerance.
4. Measure the output voltage at full load cold (V_{FLCOLD}). Let the board sit for ~10 minutes at full load, and then measure the output (V_{FLHOT}). If there is a change of more than a few millivolts, adjust R_{CS1} and R_{CS2} using Equation 46 and Equation 49.

$$R_{CS2(NEW)} = R_{CS2(OLD)} \times \frac{V_{NL} - V_{FLCOLD}}{V_{NL} - V_{FLHOT}} \quad (46)$$

5. Repeat Step 4 until the cold and hot voltage measurements remain the same.
6. Measure the output voltage from no load to full load using 5 A steps. Compute the load line slope for each change, and then average to find the overall load line slope (R_{OMEAS}).
7. If R_{OMEAS} is off from R_O by more than 0.05 mΩ, use Equation 47 to adjust the R_{PH} values.

$$R_{PH(NEW)} = R_{PH(OLD)} \times \frac{R_{OMEAS}}{R_O} \quad (47)$$

8. Repeat Step 6 and Step 7 to check the load line. Repeat adjustments if necessary.
9. When the dc load line adjustment is complete, do not change R_{PH}, R_{CS1}, R_{CS2}, or R_{TH} for the remainder of the procedure.
10. Measure the output ripple at no load and full load with a scope, and make sure it is within specifications.

AC Load Line Setting

11. Remove the dc load from the circuit and hook up the dynamic load.
12. Hook up the scope to the output voltage and set it to dc coupling with the time scale at 100 µs/div.
13. Set the dynamic load for a transient step of about 40 A at 1 kHz with 50% duty cycle.
14. Measure the output waveform (use dc offset on scope to see the waveform). Try to use a vertical scale of 100 mV/div or finer. This waveform should look similar to Figure 15.

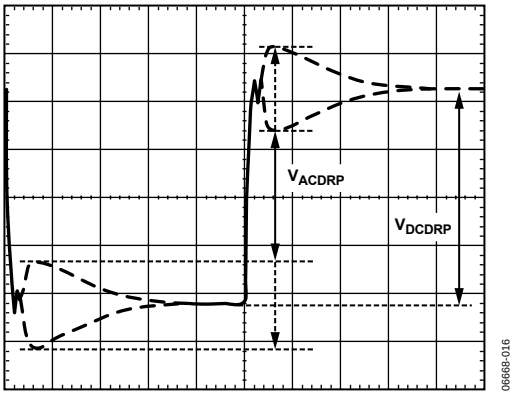


Figure 15. AC Load Line Waveform

15. Use the horizontal cursors to measure V_{ACDRP} and V_{DCDRP}, as shown in Figure 15. Do not measure the undershoot or overshoot that happens immediately after this step.
16. If V_{ACDRP} and V_{DCDRP} are different by more than a few millivolts, use Equation 49 to adjust C_{CS}. Users may need to parallel different values to get the right one because limited standard capacitor values are available. It is a good idea to have locations for two capacitors in the layout for this.

$$C_{CS(NEW)} = C_{CS(OLD)} \times \frac{V_{ACDRP}}{V_{DCDRP}} \quad (48)$$

17. Repeat Step 11 to Step 13 and repeat the adjustments, if necessary. Once complete, do not change C_{CS} for the remainder of the procedure. Set the dynamic load step to maximum step size. Do not use a step size larger than needed. Verify that the output waveform is square, which means that V_{ACDRP} and V_{DCDRP} are equal.

$$R_{CS1(NEW)} = \frac{1}{\dfrac{R_{CS1(OLD)} + R_{TH(25°C)}}{R_{CS1(OLD)} \times R_{TH(25°C)} + \left(R_{CS1(OLD)} - R_{CS2(NEW)}\right) \times \left(R_{CS1(OLD)} - R_{TH(25°C)}\right)} - \dfrac{1}{R_{TH(25°C)}}} \quad (49)$$

Initial Transient Setting

18. With the dynamic load still set at the maximum step size, expand the scope time scale to either 2 µs/div or 5 µs/div. The waveform can have two overshoots and one minor undershoot (see Figure 16). Here, V_{DROOP} is the final desired value.

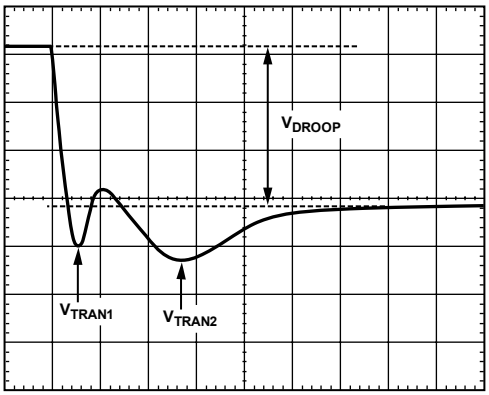


Figure 16. Transient Setting Waveform

19. If both overshoots are larger than desired, try making the adjustments using the following suggestions:
    - Make the ramp resistor larger by 25% (R_{RAMP}).
    - For V_{TRAN1}, increase C_B or increase the switching frequency.
    - For V_{TRAN2}, increase R_A and decrease C_A by 25%.

    If these adjustments do not change the response, the design is limited by the output decoupling. Check the output response every time a change is made, and check the switching nodes to ensure that the response is still stable.
20. For load release (see Figure 17), if $V_{TRANREL}$ is larger than the allowed overshoot, there is not enough output capacitance. Either more capacitance is needed, or the inductor values need to be made smaller. When changing inductors, start the design again using a spreadsheet and this tuning procedure.

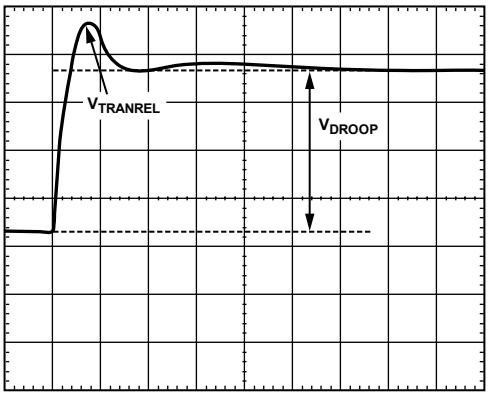


Figure 17. Transient Setting Waveform

Because the ADP3197 turns off all of the phases (switches inductors to ground), no ripple voltage is present during load release. Therefore, the user does not have to add headroom for ripple. This allows load release $V_{TRANREL}$ to be larger than V_{TRAN1} by the amount of ripple and still meet specifications.

If V_{TRAN1} and $V_{TRANREL}$ are less than the desired final droop, capacitors can be removed. When removing capacitors, also check the output ripple voltage to make sure it is still within specifications.

LAYOUT AND COMPONENT PLACEMENT

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Recommendations

For good results, a PCB with at least four layers is recommended. This provides the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input and output power, and wide interconnection traces in the remainder of the power delivery current paths. Keep in mind that each square unit of 1 oz copper trace has a resistance of ~0.53 mΩ at room temperature.

Whenever high currents must be routed between PCB layers, use vias liberally to create several parallel current paths, so the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.

If critical signal lines (including the output voltage sense lines of the ADP3197) must cross through power circuitry, it is best to interpose a signal ground plane between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.

An analog ground plane should be used around and under the ADP3197 as a reference for the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground and should not be tied to any other power circuitry to prevent power currents from flowing into it.

The components around the ADP3197 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB pin and the CSSUM pin. The output capacitors should be connected as close as possible to the load (or connector), for example, a microprocessor core, that receives the power. If the load is distributed, the capacitors should also be distributed and generally be in proportion to where the load tends to be more dynamic.

Avoid crossing any signal lines over the switching power path loop (as described in the Power Circuitry Recommendations section).

Power Circuitry Recommendations

The switching power path should be routed on the PCB to encompass the shortest possible length to minimize radiated switching noise energy (EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system and noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. Using short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing; and it accommodates the high current demand with minimal voltage loss.

When a power dissipating component, for example, a power MOSFET, is soldered to a PCB, it is recommended that vias be used liberally, both directly on the mounting pad and immediately surrounding it. Two important reasons for this are improved current rating through the vias and improved thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer the heat to the air. Make a mirror image of any pad being used to heat-sink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation in the air around the board. To further improve thermal performance, use the largest possible pad area.

The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

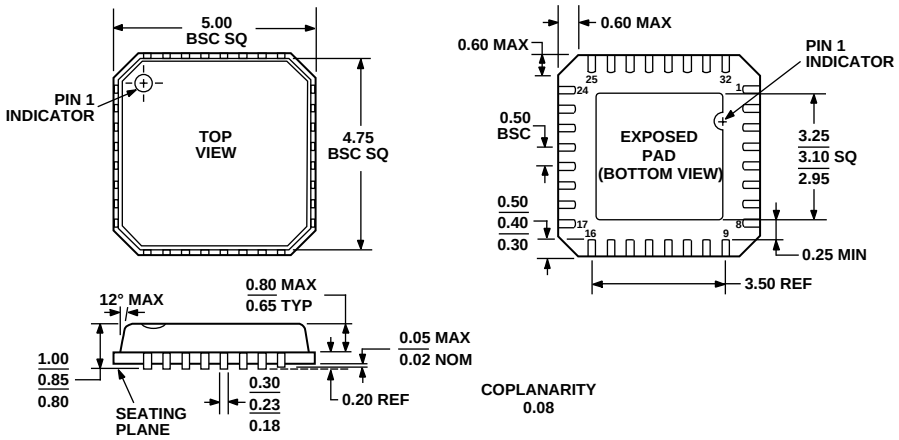
For best EMI containment, a solid power ground plane should be used as one of the inner layers extending fully under all the power components.

Signal Circuitry Recommendations

The output voltage is sensed and regulated between the FB pin and the FBRTN pin, which connect to the signal ground at the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be small. Thus, the FB trace and FBRTN trace should be routed adjacent to each other on top of the power ground plane back to the controller.

The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be connected to the output voltage at the nearest inductor to the controller.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 18. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADP3197JCPZ-RL[1]	0°C to 85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2	2,500

[1] Z = RoHS Compliant Part.

NOTES

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