Video Crosspoint Switch Simplifies Large Matrix Designs

The DG884 is a digitally selectable eight-input to four-output monolithic bidirectional crosspoint IC suitable for wideband analog and digital signal routing. Wideband here is used to define signals with bandwidths in the range of 60 to 200 MHz. Fabricated with the Vishay Siliconix D/CMOS technology, the DG884 incorporates n-channel DMOS switching FETs with low-power CMOS control logic, drivers, and latches. The low-capacitance DMOS FETs are connected as low on-resistance T-switches to achieve high levels of off-isolation and low levels of crosstalk. On-chip TTL-compatible address latches and data readback are included to simplify microprocessor interfacing. Double buffering of the switch addressing allows update information to be loaded without affecting the existing state of the crosspoint. A single SALVO command is all that is required to transfer previously set information to the current event latches. This single command significantly speeds up the setup time, especially in large matrices requiring more than one DG884.

The Signal Path

The internal function blocks of the DG884 are shown in Figure 1, and the signal path from one input to one output is shown in Figure 2. The signal path is composed of a T-switch at the matrix and an additional low-resistance switch in series with each output. The T-switch connection maximizes the off-isolation by shunting to ground any signal that feeds through the small series capacitances of the off series switches. The series output switches offer a number of advantages, namely:

- They provide an extra stage of isolation at the output
- They reduce the off-state output capacitance, which is necessary when other DG884 outputs are connected in parallel.
- They reduce the off-output leakage.

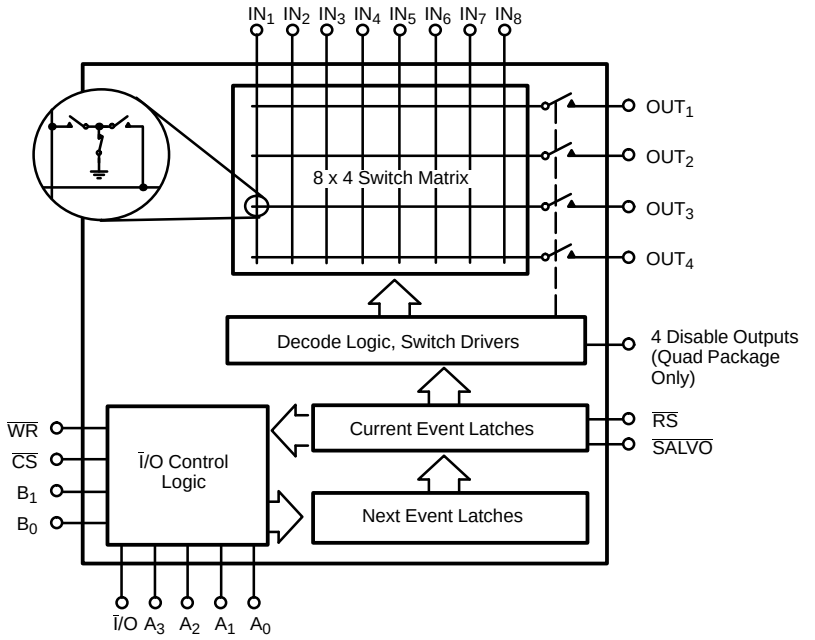
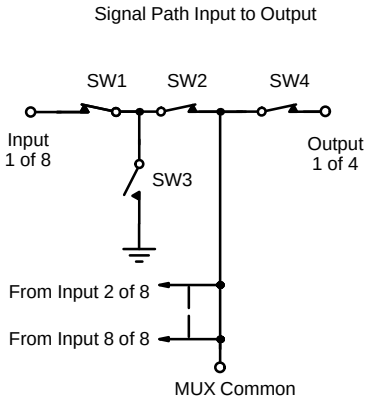


FIGURE 1. DG884 Block Diagram



Typical on-resistances at 25°C:
SW1 = SW2 = 20 Ω
SW3 = 200 Ω
SW4 = 10 Ω

FIGURE 2. DG884 Signal Path

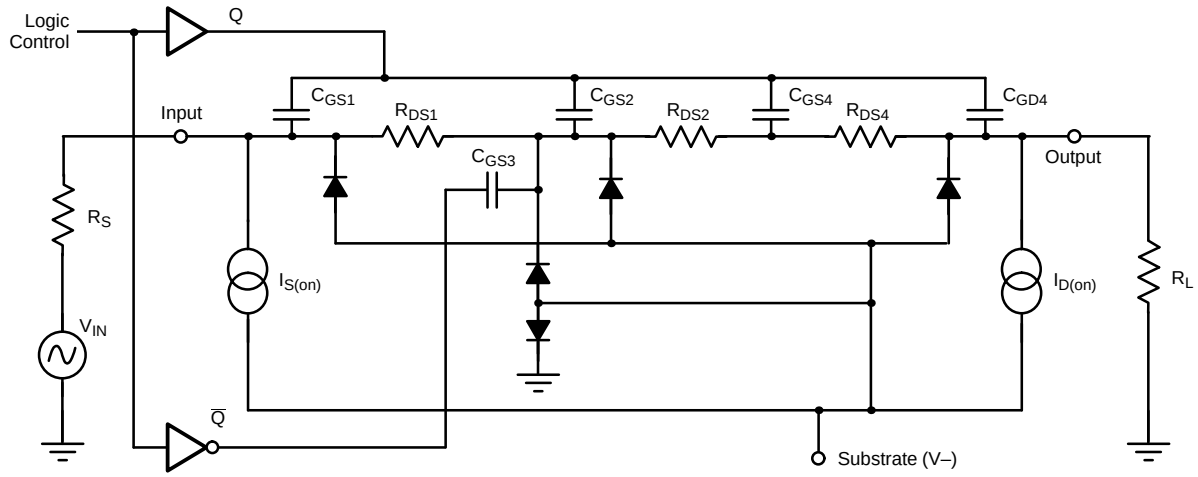
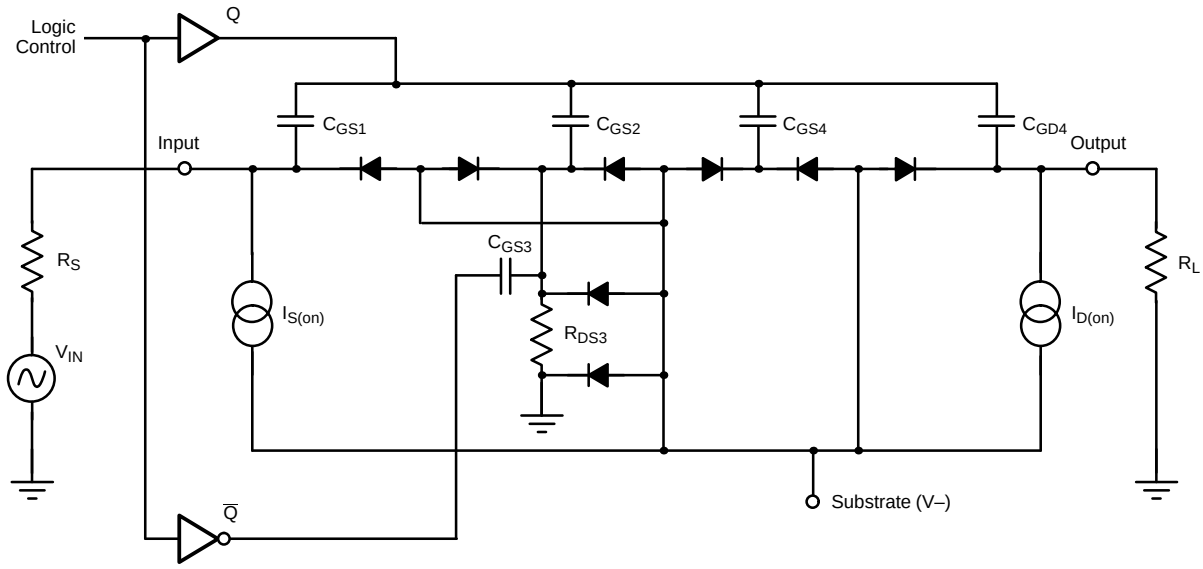


FIGURE 3. On-State Model



Note: Individual drain-source capacitances not shown for clarity.

FIGURE 4. Off-State Model

Figures 3 and 4 show low-frequency models of an “on” channel and an “off” channel, respectively. The models allow us to visualize the effects of leakage, low-frequency transmission loss, and analog overvoltage on the overall circuit performance. The term “low-frequency” is used for the models because they use single components to represent the characteristics of the channel. In other words, components distributed over an area of silicon are lumped together for simplicity’s sake. An accurate high-frequency model of an “on” channel demands a more complex RC network (more on this later).

Leakage-Generated Offsets

Depending on the value of source and load impedances connected to input and output, leakage-generated offset voltages can be obtained using Ohms Law. In practice, however, the DG884 will be used surrounded by fast linear circuitry whose bias currents will be much higher than the nanoampere leakage currents of the D/CMOS process. Thus, offset voltages will be dominated by the external circuitry around the crosspoint and not the DG884.

Transmission Loss

Transmission loss is a function of the load connected to the crosspoint output for a fixed channel on-resistance and source impedance. Transmission loss is given by

$$\text{Loss (dB)} = 20 \log_{10} \frac{R_{load}}{R_{source} + R_{channel} + R_{load}}$$

Where $R_{channel} = R_{DS1} + R_{DS2} + R_{DS4}$.

This equation is accurate at frequencies below 1 MHz, where device capacitances (i.e., on-state input capacitance) can be safely ignored.

Input Overvoltage

Overvoltage effects are the third important characteristic that can be visualized from the models shown in Figures 3 and 4. Unlike mechanical switches, solid-state analog switches have electrical “end-stops” beyond which the switch ceases to behave as a switch. These “end-stops” are defined by the power supply rails. For an ”on” channel, a signal at the input can swing to the negative rail before the shunt-switch body diodes (Figure 3) begin to conduct. When these diodes conduct, a large current from the negative rail can result. This current flow should be limited to 20 mA dc as defined in the absolute maximum ratings. During the period of negative overvoltage, the crosspoint outputs will be corrupted whether they are selected or not. A single diode in series with the negative rail will prevent reverse current flow and output corruption during negative overvoltage.

In the positive direction, if the input is allowed to continue rising towards the positive supply rail, its amplitude should be limited to the breakdown voltage of the body-to-source junction of the switching FETs. This is specified in the data sheet maximum ratings section, where a value of 14 V above the negative rail is quoted. Where rails of +15 V and –5 V are used, the body-source breakdown voltage is the maximum positive limit of the signal at the source (input) or the drain (output) terminals. In a power down situation, where the positive and negative rails are at zero, the maximum positive input signal is also 14 V above the negative rail. No output corruption will occur during positive overvoltage.

Distortion

The change of on-resistance with signal swing, explained above, will give rise to distortion unless specific precautions are taken. A study of the equation for transmission loss reveals that distortion caused by changing on-resistance is inversely proportional to load resistance. Thus, distortion is given by

$$\text{DIST} = 20 \times \log (\Delta R_{on}/R_{load})$$

From the above, the decibel level below the fundamental may be calculated. Figure 5 shows how the on-resistance varies with signal swing. ΔR_{on} is 5 Ω for a signal swing of ± 5 V. Thus, for R_{load} = 5 kΩ, distortion is –60 dB. For low-frequency operation of the DG884 (where isolation and crosstalk performance may be critical in demanding applications), signal swings are usually much greater than those found at video frequencies and above. Thus, R_{load} should be increased accordingly. In all cases, some form of high-performance buffer/amplifier will be required at the output to translate the crosspoint load resistance to a lower “interface” value, i.e., 50 to 75 Ω for high-frequency designs.

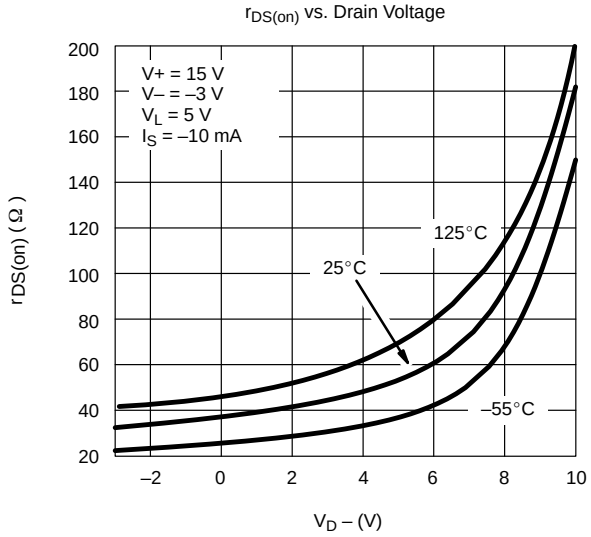


FIGURE 5. Change of On-Resistance with Signal Amplitude

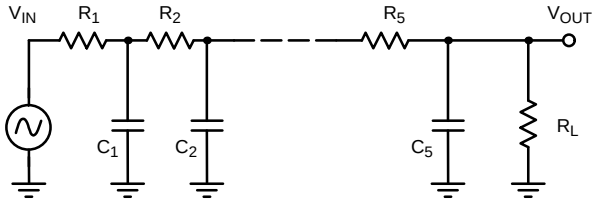
Decoupling

A high-frequency signal path exists between the analog channel and the power rails via the gate-to-source capacitances of the switching FETs, as shown in Figures 3 and 4. This is because the drive logic applies either rail voltage to the gate via a low impedance path. Good decoupling shunts this signal leakage harmlessly to ground.

High-Frequency Model

The parameters that determine the frequency response of the selected crosspoint are input capacitance and on-resistance. Input capacitance is made up of interconnect lines on the chip, FET capacitance, and small bond wire and interconnect capacitances. On-resistance is made up of the three series FETs that form the crosspoint path. DMOS FETs are very efficient at providing low on-resistance in a small area; however, the resistance is spread over the entire channel length. Thus, resistance and capacitance are distributed, and the simple lumped models of Figures 3 and 4 are inadequate for high frequencies. Figure 6 shows a suitable model of an "on" channel. The five-stage model is easily obtained from the data sheet by taking on-resistance and capacitance values and dividing them by five to obtain the element values, as shown in Figure 6. Worst-case values are those obtained from a one input to four output set-up condition. Note that we show the model driven by a voltage source with zero output impedance — the importance of this in maximizing operating bandwidth should not be underestimated. To generate the data sheet frequency curves, Vishay Siliconix uses a network analyzer to obtain V_{out}/V_{in} with respect to frequency. In this way, the device plots are independent of source impedance.

The DG884 is a high-performance device and must be driven by very high-performance analog buffers, such as the Vishay Siliconix CLC111 and CLC410. The accompanying performance curves were derived from an evaluation board consisting of CLC111s at the inputs and gain-of-two CLC410s at the outputs of a DG884.



$R_1 + R_2 + R_3 + ...R_n = r_{DS(on)}$
$C_1 + C_2 + C_3 + ...C_n = (C_S + C_D)$ (on)

FIGURE 6. Wideband On-Channel Equivalent Circuit

The Digital Interface

The DG884 has comprehensive microprocessor interface facilities. A brief explanation of the sequence of commands required to set up the device follows.

A $\overline{\text{RESET}}$ command may be used as a power on reset. This will clear the current event latches and will result in all outputs being turned off. The $\overline{\text{RESET}}$ command operates on the current event address latches only. This is to allow existing or new data to be retained in the next event latches independent of the $\overline{\text{RESET}}$ operation.

To address the device, $\overline{\text{CHIP SELECT}}$ should be set low, Ī/O low, and $\overline{\text{RESET}}$, $\overline{\text{WRITE}}$, and $\overline{\text{SALVO}}$ all high. The input-to-output path is selected by $A_0 – A_3$ for the input, and B_0, B_1 for the output. Each addressing byte ($A_0 – A_3$) is latched into the next event latch (selected by the B_0, B_1 address) by the $\overline{\text{WRITE}}$ line going low and returning high again. This is repeated three more times to address all four output lines. Note that the internal logic forbids any addressing that tries to connect two separate inputs to the same output.

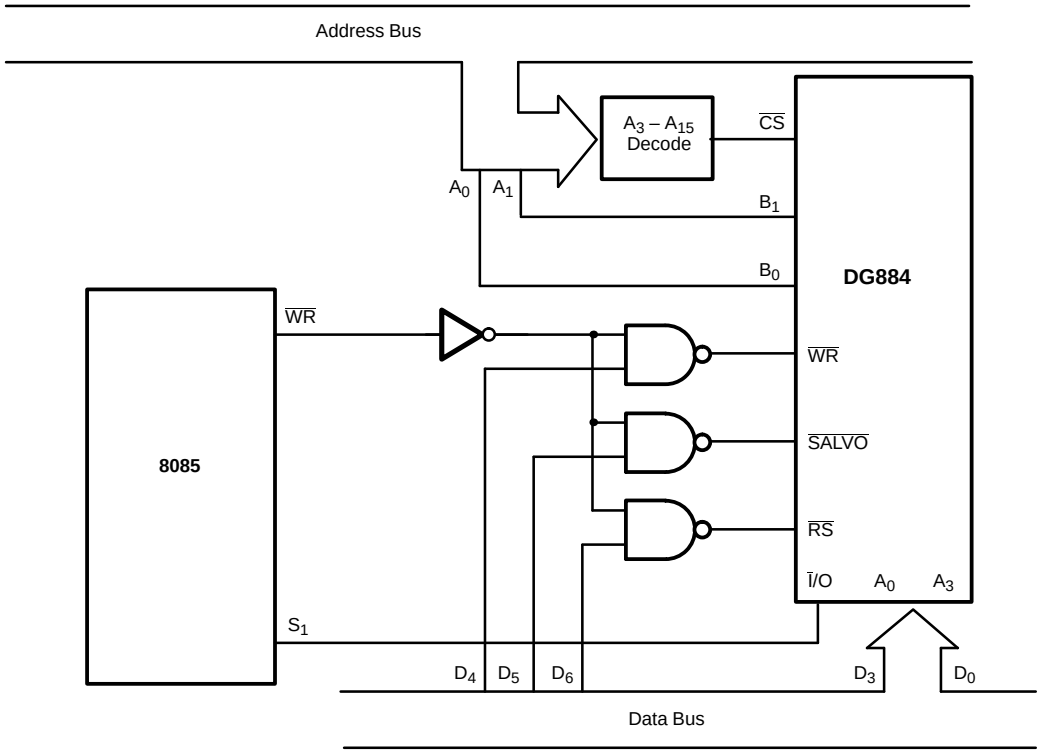
Having set four input-to-output paths into the next-event latches with four $\overline{\text{WRITE}}$ commands, the current event latches are then simultaneously loaded by $\overline{\text{SALVO}}$ going low and returning high.

The $A_0 – A_3$ address inputs are tri-stated when $\overline{\text{CHIP SELECT}}$ returns to high, along with $\overline{\text{RESET}}$, Ī/O, $\overline{\text{WRITE}}$, and $\overline{\text{SALVO}}$. This ensures that no bus contention will occur during input addressing or data readback when a number of devices are connected in parallel.

The DG884 has data readback built in. This useful facility enables a form of handshaking to verify that a particular address has been set. Data readback is enabled by the Ī/O line going high and $\overline{\text{CHIP SELECT}}$ going low on the device being interrogated.

Address A_3 functions as an output turn-off command. There are four open-drain $\overline{\text{DISABLE}}$ pins that are active low when the particular output is off. They are designed to interface directly with the disable pin of the CLC410 current feedback op amp. For other uses, the DG884 $\overline{\text{DIS}}$ outputs look like 200 Ω to V–, when V+ = 15 V.

Figure 7 shows a memory mapped interface scheme for an 8085 microprocessor. From the circuit diagram, assume that the address decode gives a base address to the DG884 of 0 N_1 N_2 N_3 0 H, where N is a specific hex number. The A_0 and A_1 address lines connected to B_0 and B_1 inputs, respectively, of the DG884, map its address from 0 $N_{1\text{-}3}$ 0 H through to 0 $N_{1\text{-}3}$ 3 H (i.e., four address locations).



Data									Result
D_7	D_6	D5	D_4	D_3	D_2	D_1	D_0	WR	
X	0	0	0	B	B	B	B		Nothing; $D_4 = 0$
X	0	0	1	B	B	B	B		4 -bit binary data written into one of four next event latches. The latch is decided by status of B_0 and B_1 lines.
X	0	1	0	X	X	X	X		Salvo pulse – updates current event latches.
X	1	0	0	X	X	X	X		Reset or clear pulse resets all latches and sets all switches to open circuit.

FIGURE 7. 8085 Microprocessor Interface

Four-bit data to be written to or read from the DG884 is applied to the $A_0 – A_3$ input lines. These inputs are connected to $D_0 – D_3$ of the computer data bus. Three of the higher order data bus lines, $D_{4,5,6}$ (D_7 is not used at all with the DG884), are used to gate the $\overline{\text{WRITE}}$ pulse through to either the $\overline{\text{WRITE}}$, $\overline{\text{RESET}}$, or $\overline{\text{SALVO}}$ inputs. The truth table gives the implementation of the gating shown in the circuit diagram.

To read four-bit data from the DG884 (i.e., the current event latch status), the $\overline{\text{I}}$/O terminal is connected to the S_1 output of the 8085. This signal provides an advance Read/Write control to the DG884. A read operation from the above four separate memory locations will give the status of each current event latch. Data being read from the DG884 will appear on the four lower data lines, $D_0 – D_3$, of the computer data bus.

Differential Applications

Although the DG884 is a single-ended 8 x 4 crosspoint, it may be used as a differential 4 x 2 crosspoint. Address A_2 defines inputs 1 - 4 or 5 - 8, while address B_1 defines the outputs, namely 1 and 2, or 3 and 4. A suitable wideband differential amplifier (CLC410) at the output will provide common-mode rejection of incoming signals and charge injection thanks to the inherent path match within the crosspoint IC.

There is also a need for wideband two-input/output crosspoint systems when dealing with S-VHS

(Super-VHS) signals. S-VHS is a much enhanced form of the VHS system from JVC, and it virtually eliminates signal degradation caused by multi-separation and combination of the luminance (Y) and chrominance (C) components that make up a color video signal. In S-VHS, separate Y and C signals are fed to the recorder, and at playback, Y and C signals are obtained for feeding directly to a suitable TV monitor, i.e., one fitted with an S-connector (SCART).

The S-VHS frequency spectrum extends the peak white portion of the FM signal from 4.8 MHz to 7 MHz. Thus there is a need for wideband two input/output crosspoint systems such as the DG884. Figure 8 outlines the DG884 as a 4 x 2 x 2 crosspoint. A key feature of this use is the reduced change of capacitance at the inputs, compared to the normal 8 x 4 connection. The worst-case input capacitance for one input to two outputs is 80 pF, and the worst case for one input to one output remains the same at 40 pF. Substituting these values into the HF model outlined above, bandwidth and source impedance trade-offs can be evaluated.

Power Supplies

The DG884 requires three power supplies for ground-referenced signal handling (V+, V–, and V_L = 5 V). The negative and positive supplies should always be established first. The logic supply should not be allowed to rise above the V+ pin during power supply on/off sequencing. This is because a PN junction exists between the V+ and V_L pins, and large currents could flow if this junction becomes forward biased. If both V+ and V_L are derived from the same supply there will be no problems. Figure 9 shows power supplies and decoupling for bipolar signal operation.

The DG884 may be operated in single supply situations (with V– connected to 0 V) with no loss of logic threshold accuracy. However, the signal should be offset to +3 V to preserve signal fidelity through the device.

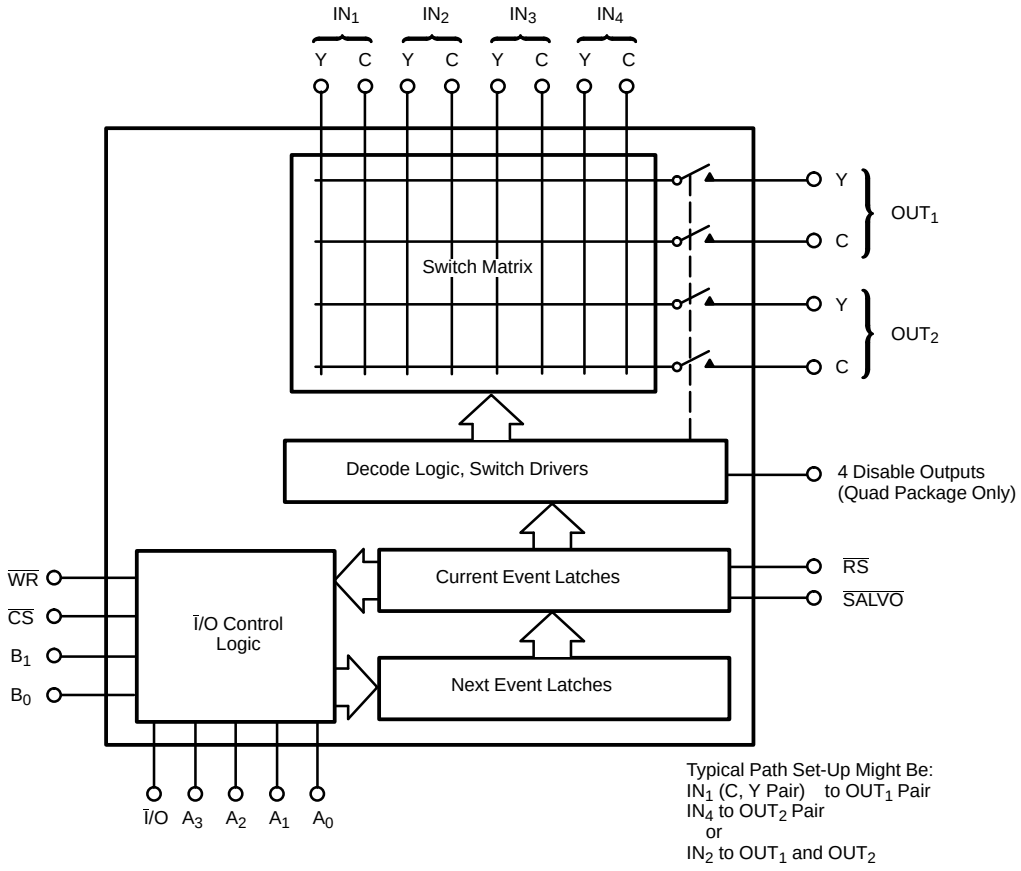


FIGURE 8. 4 × 2 × 2 Crosspoint

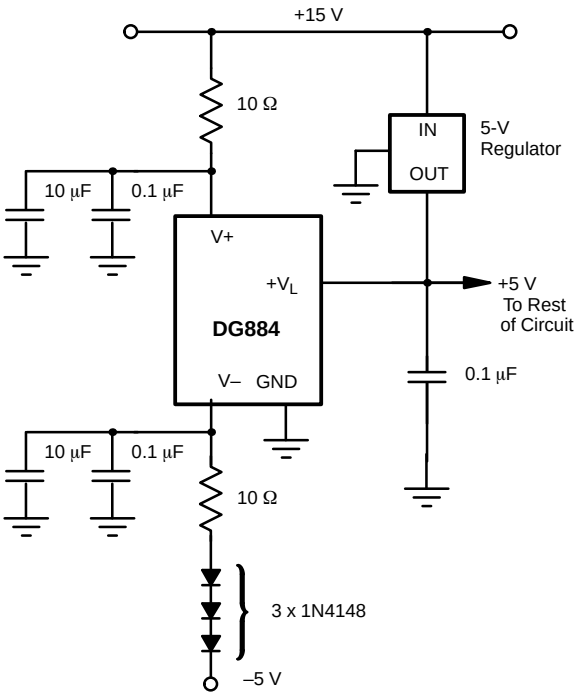


FIGURE 9. Power Supplies for DG884

Audio Operation

While the DG884 was designed for wide bandwidth applications, its excellent crosstalk and isolation specifications resulting from the T-switch configuration, together with the high level of integration (four 8-channel multiplexers in one package), make the part very attractive for audio applications. Used with load resistors of 1 MΩ or more, the distortion is below 0.01% for audio signals at –10 dBu (0.316 V_{RMS}) level when powered from +12 V and –5 V supplies. The high value load resistors can cause excessive levels of noise at the output amplifier when the crosspoint is disabled. This can be reduced by using the $\overline{\text{DISABLE}}$ outputs of the crosspoint to shunt the high value load resistors to ground during disable mode.

Layout Considerations

As with all high-frequency work, good PCB layout practice is essential if the inherent device performance is not to be degraded. Maximum ground plane area ensures that circuit ac ground really has low impedance. The inter-channel ground pins of the DG884 provide essential screening between channels right to the silicon, as well as separate return paths for each input. Thus input crosstalk is doubly improved. Similar considerations apply for the output inter-channel grounds.

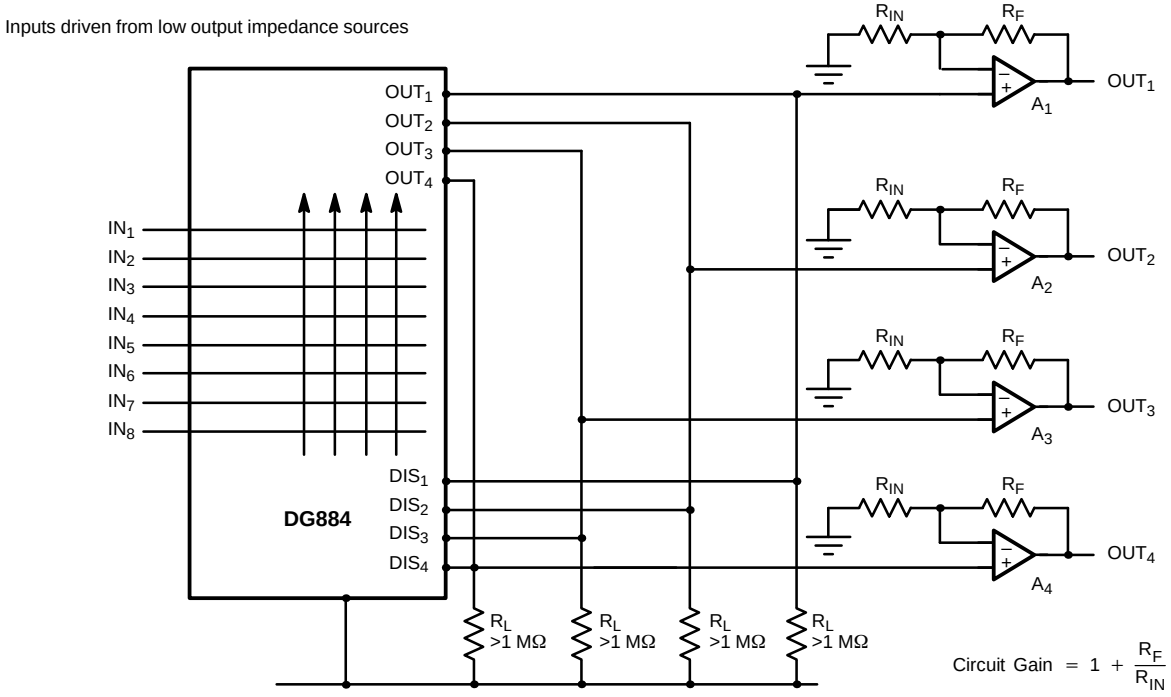


FIGURE 10. Audio Voltage–Mode Crosspoint

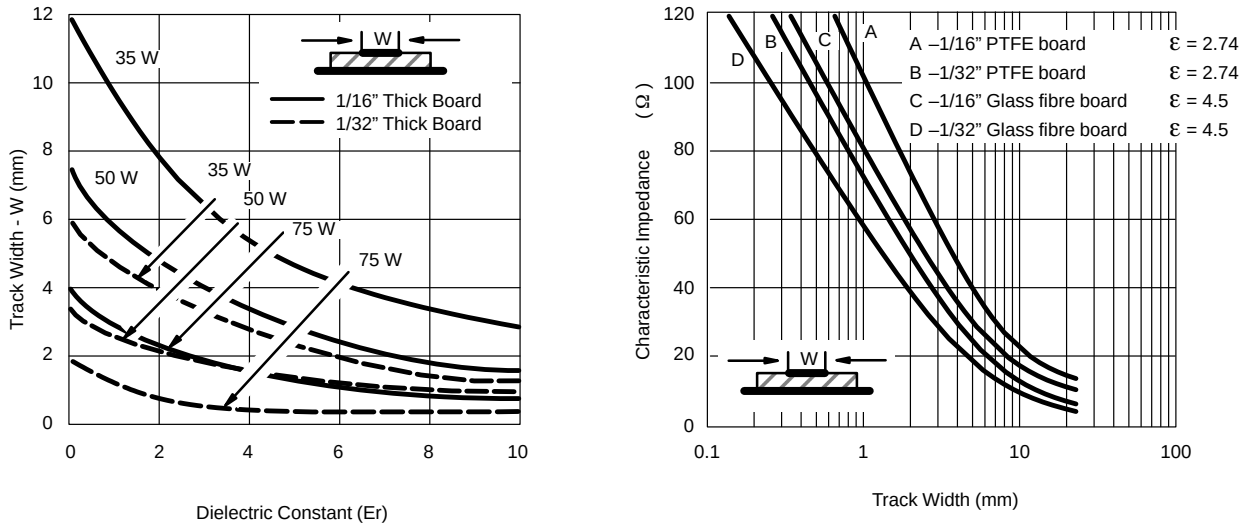


FIGURE 11. PCB Trace Characteristic Impedance

The inherent channel match of the monolithic DG884 can be upset by poor external layout. Ideally all input lines to and from the inputs and outputs should be exactly the same electrical length to minimize external path (and therefore phase) differences between the channels.

It may be useful to incorporate transmission lines on the PCB where the layout forces lengthy track runs. In this case, the curves in Figure 11 will help define trace geometry to obtain particular characteristic impedances, such as 50 to 75 Ω.

The importance of good decoupling has already been mentioned. However, it is worth stressing that component placement should ensure the absolute minimum track length from the decoupling point to ground.

Evaluation Results

Figure 12 shows the circuit diagram of the DG884 evaluation board used with the CLC111 as an input buffer and the CLC410 gain-of-two amplifier at the output. The CLC410s provide output disable and "loss-less" cable termination. Thanks to its excellent reverse gain characteristics, the input CLC111 provides a solid input impedance of 75 Ω that is independent of the path setting of the DG884. Ideally, the outputs of the CLC111s should feed directly to the crosspoint inputs. However, the capacitive load presented by the DG884 reacts with the open-loop output impedance of the CLC111 to cause amplitude peaking by reducing the feedback within the buffer at increasing frequencies. A series resistance at the output of the buffer corrects for this. From the CLC111 data sheet, a value of 12 Ω is required for load capacitances of about 150 pF, which corresponds to the worst-case on-state capacitance of the DG884 when set for one input to all outputs.

At the output, the 4.7-kΩ load is chosen as a compromise between loading and output offset. With this value, offsets will typically be less than 10 mV.

Figures 13 and 14 show gain and phase plots obtained from the circuitry shown in Figure 12. Figure 13, the response for one input to one output, shows a bandwidth of 150 MHz. Figure 15, the response for one input to four outputs simultaneously, shows a bandwidth of 55 MHz. Figure 14 shows the measurement setup. The plots are typical of all channel selections and demonstrate the change in bandwidth between best- and worst-case path selections. The prototype showed a maximum delta phase shift of 10° at 30 MHz across inputs 1 through 8. This equates to a differential delay of 0.9 ns and is probably due to the input trace layout on the PCB, adding some 10 cm (worst case) differential path length.

The isolation available from a disabled output (all other outputs driven and terminated) is in reality a measure of the output adjacent crosstalk of the prototype and shows a healthy –50 dB at 30 MHz (Figure 16).

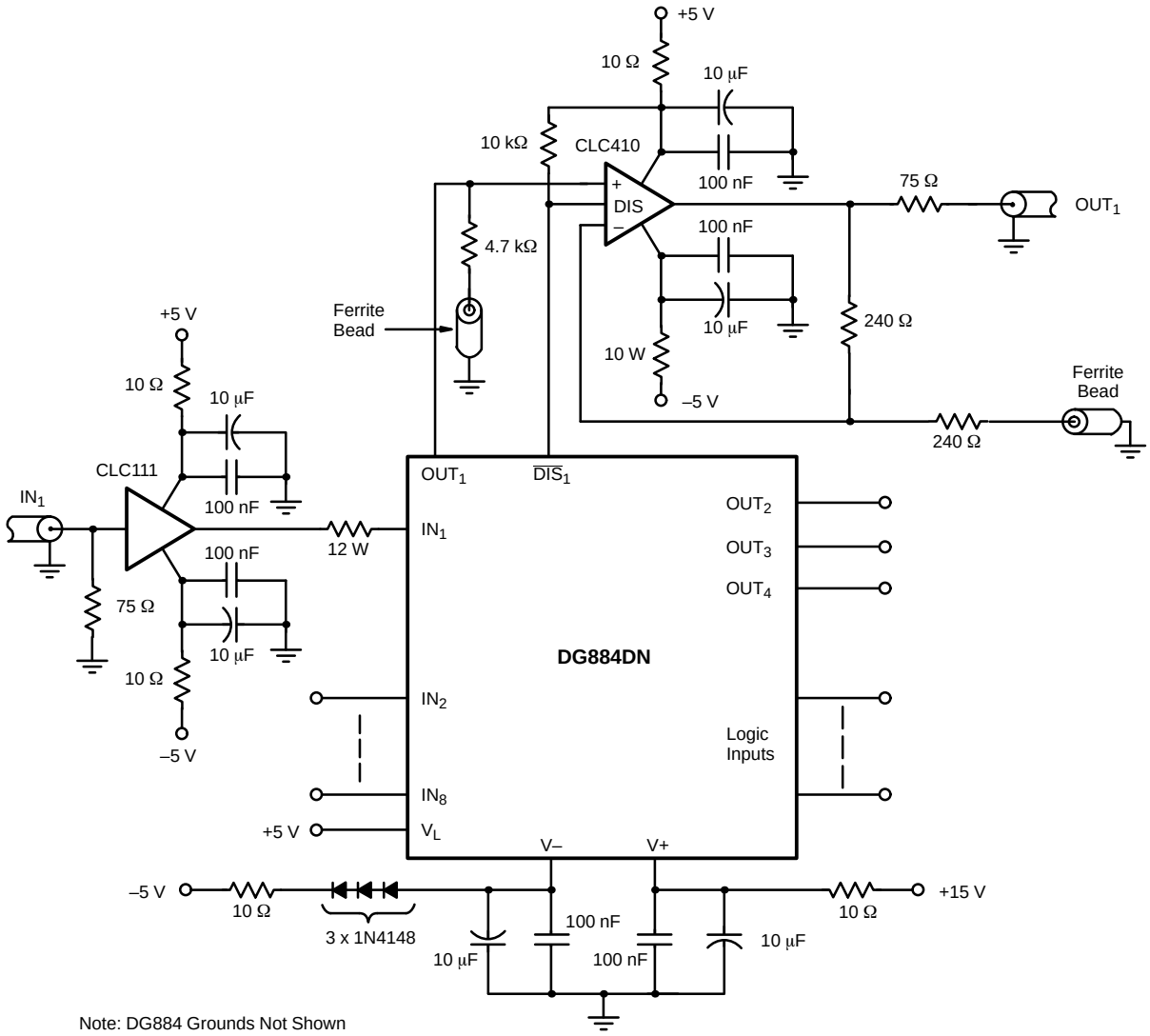


FIGURE 12. DG884 Wideband Crosspoint

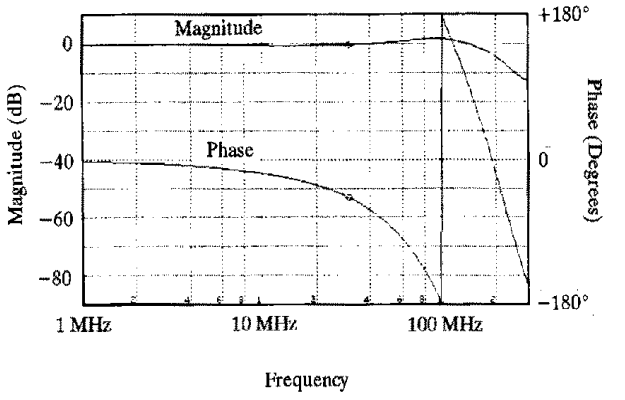


FIGURE 13. Response For One Input to One Output

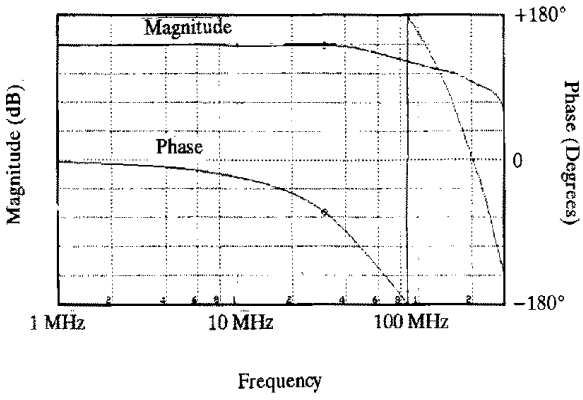


FIGURE 14. Response For One Input Going to All Four Outputs.

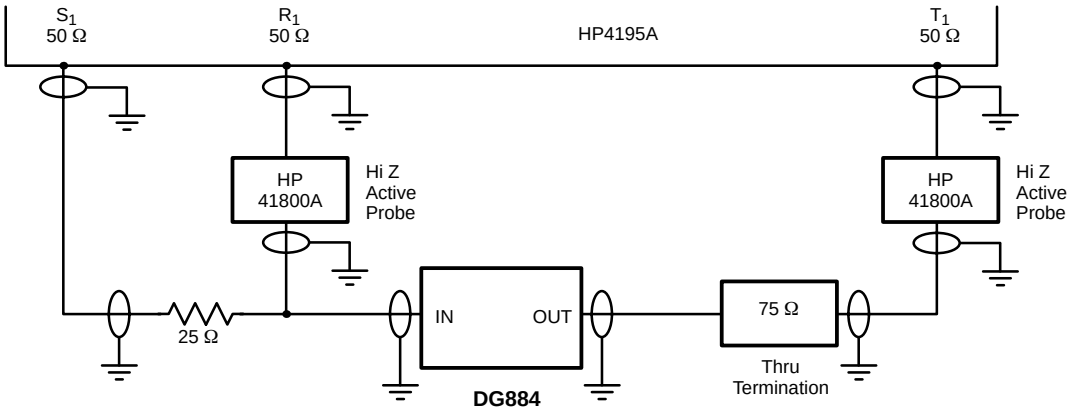


FIGURE 15. Network Measurement

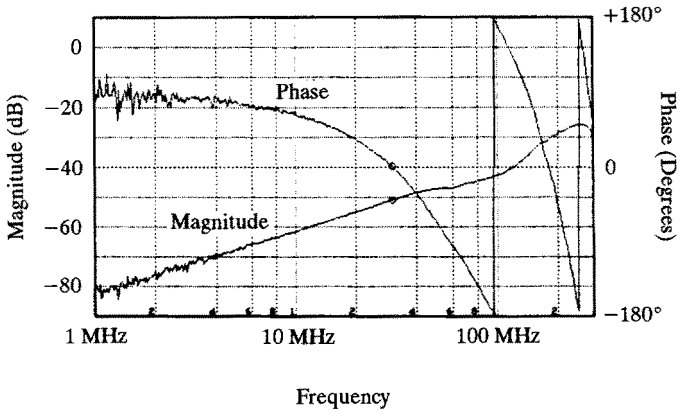


FIGURE 16. Output Isolation

To measure the overall distortion of the DG884 setup, two methods were chosen. Differential gain and phase are well known to the video community and show how well the overall signal path maintains a constant small-signal gain and phase for the low-level color carrier at 4.43 MHz (PAL) or 3.58 MHz (NTSC) as the brightness (luminance) signal is ramped through its specified range. The second method uses a two-tone intermodulation test to determine large signal performance and arrive at a figure of merit known as third-order intercept point. This is well known to communication engineers who need to judge the ability of a channel to resolve small signals in the presence of many large ones without the benefit (and complexity) of filter selectivity. The differential gain and phase measurements were made using a network analyzer (HP4195A), and a distortion analyzer (Marconi TF2910/4) was used to provide a cross check. Figure 17 shows the measurement setup for the analyzer, and Figure 18 shows the Marconi setup.

The results from the analyzer are shown in Figure 19 for one input to one output, and in Figure 20, for one input to four outputs, the latter being the worst-case loading. The analyzer test signal was a ramp of 700 mV with a 280 mV peak, 4.43-MHz signal superimposed to represent the dynamics of a video signal. The analyzer plots clearly show the gain reduction (negative slope) at peak brightness and also the phase change .

Tests with the Marconi set up showed that differential gain and phase measurements were below 0.08% and 0.05°, respectively, when the test waveform was an EBU International Test Line signal C. Measurements below 0.1% and 0.1° are difficult to resolve with the Marconi setup, which is why the analyzer method was tried as well.

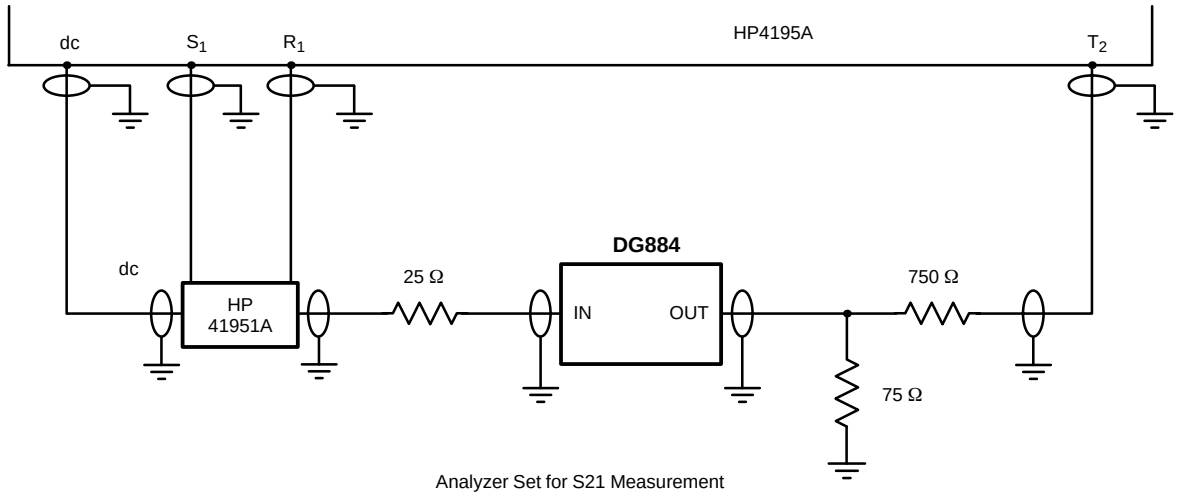


FIGURE 17. Differential Gain and Phase

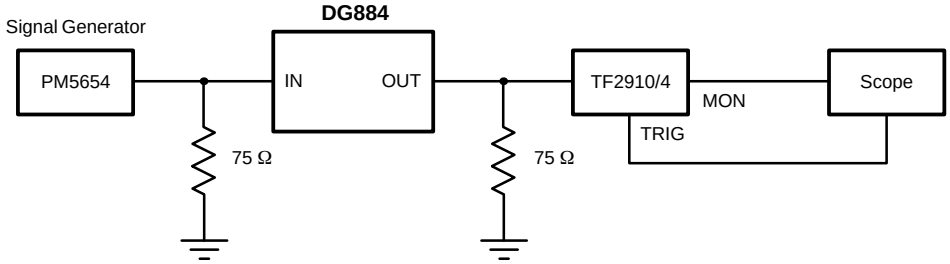


FIGURE 18. Marconi TF2910/4 Setup

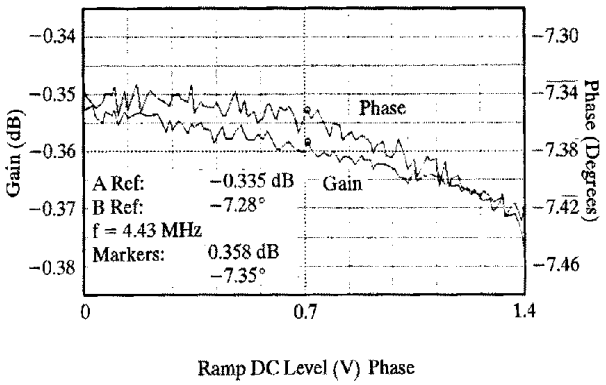


FIGURE 19. One Input to One Output

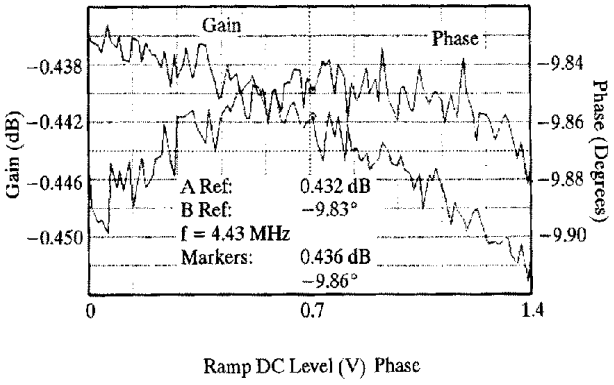


FIGURE 20. One Input to Four Outputs

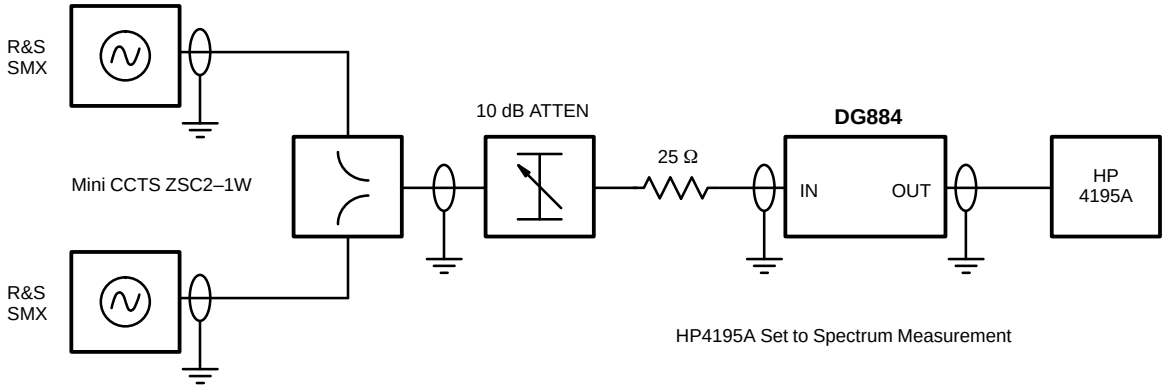


FIGURE 21. Two-Tone Intermodulation Test

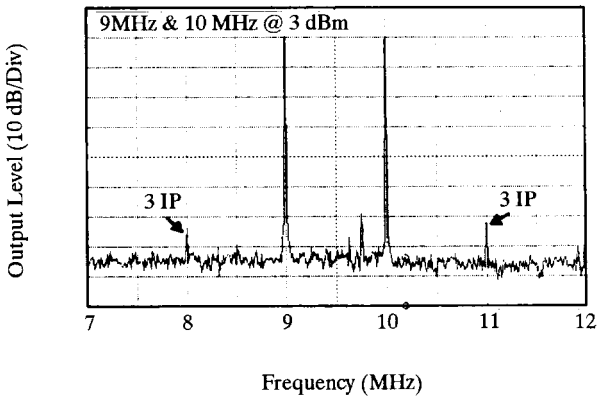


FIGURE 22. Third Order Intercept Points

The setup for the third-order intercept measurement is shown in Figure 21, and a plot of the of results is shown in Figure 22. The test was for one input to four outputs simultaneously. A signal spacing of 1 MHz was chosen to reflect the broadband nature of the crosspoint setup. For two signals at –10 dB, the third-order products were –60 dB, giving an intercept point of +30 dBm—a very respectable figure.

Summary

The DG884 wideband crosspoint IC extends the state-of-the-art in monolithic wideband switching technology. Accompanied by the CLC111 and CLC410 linear ICs, the DG884 further simplifies the task of designing low-distortion wide-bandwidth crosspoint systems.

Note: an evaluation PCB, providing a working 8 x 4 wideband crosspoint with 75-Ω interface is available from Vishay Siliconix. Check with your local Vishay Siliconix sales office for details.

References

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