19-0631; Rev 1; 3/07

MAXIM

Low-Charge Injection, 8-Channel, High-Voltage Analog Switches

General Description

The MAX4800/MAX4801/MAX4802 provide high-voltage switching on eight channels for ultrasonic imaging and printer applications. The devices utilize BCDMOS process technology to provide eight high-voltage low-charge-injection SPST switches, controlled by a digital interface. Data is clocked into an internal 8-bit shift register and retained by a programmable latch with enable and clear inputs. A power-on reset function ensures that all switches are open on power-up.

The MAX4800/MAX4801/MAX4802 operate with a wide range of high-voltage supplies including: V_{PP}/V_{NN} = +100V/-100V, +185V/-15V, and +40V/-160V. The digital interface operates from a separate V_{DD} supply from +2.7V to +13.2V. Digital inputs DIN, CLK, $\overline{LE}$, and CLR are +13.2V tolerant, independent of the V_{DD} supply voltage. The MAX4802 provides integrated 35kΩ bleed resistors on each switch terminal to discharge capacitive loads.

The MAX4800 and MAX4802 are drop-in replacements for the Supertex HV20220 and HV232. The devices are available in the 48-pin TQFP, 26-bump CSBGA, 28-pin PLCC, and 48-pin TQFN packages. The MAX4801 is a drop-in replacement for the Supertex HV20320 and is available in the 28-pin PLCC package. All devices are specified for the commercial 0°C to +70°C temperature range.

Applications

Ultrasound Imaging

Printers

Features

- **Pin-Compatible Replacement for Supertex HV20220 (MAX4800)**
- **Pin-Compatible Replacement for Supertex HV20320 (MAX4801)**
- **Pin-Compatible Replacement for Supertex HV232 (MAX4802)**
- **Flexible High-Voltage Supplies Up to V_{PP} - V_{NN} = 200V**
- **Low-Charge Injection, Low-Capacitance 22Ω Switches**
- **DC to 10MHz Analog-Signal Frequency Range**
- **-77dB Off Isolation at 5MHz**
- **Low 10µA Quiescent Current**
- **Integrated Bleed Resistors (MAX4802)**
- **Available in PLCC, TQFP, TQFN, and CSBGA Packages**

Ordering Information/Selector Guide

PART	BLEED RESISTORS	SECOND SOURCE	PIN-PACKAGE	PACKAGE CODE
MAX4800CCM	No	HV20220FG	48 TQFP	C48-6
MAX4800CQI	No	HV20220PJ	28 PLCC	Q28-4
MAX4800CTM*	No	HV220**	48 TQFN	T4866-1
MAX4800CXZ*	No	HV220**	26 CSBGA	X07265-1
MAX4801CQI*	No	HV20320PJ	28 PLCC	Q28-4
MAX4802CCM	Yes	HV232FG	48 TQFP	C48-6
MAX4802CQI	Yes	HV232PJ	28 PLCC	Q28-4
MAX4802CTM*	Yes	HV230**	48 TQFN	T4866-1
MAX4802CXZ*	Yes	HV230GA	26 CSBGA	X07265-1

Note: *All devices are specified over the commercial 0°C to +70°C temperature range.*

**Future product—contact factory for availability.*

***Not pin-for-pin compatible.*

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Low-Charge Injection, 8-Channel, High-Voltage Analog Switches

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{DD} Logic-Supply Voltage .....-0.5V to +15V
V_{PP} - V_{NN} Supply Voltage 220V
V_{PP} Positive-Supply Voltage .....-0.5V to V_{NN} + 220V
V_{NN} Negative-Supply Voltage .....+0.5V to -220V
Logic Inputs $\overline{LE}$, CLR, CLK, DIN .....-0.5V to +15V
DOUT .....-0.5V to V_{DD} + 0.5V
RGND (MAX4802) .....-4.5V to + 0.5V
COM_, NO_.....V_{NN} to V_{PP}
Continuous Power Dissipation (T_A = +70°C)
28-Pin PLCC (derate 10.5mW/°C above +70°C) 842mW
48-Pin TQFP (derate 22.7mW/°C above +70°C).....1818mW
48-Pin TQFN (derate 27.8mW/°C above +70°C) 2222mW
26-Pin CSBGA (derate 11.8mW/°C above +70°C) 941mW
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature Range .....+150°C
Lead Temperature (Soldering, 10s).....+300°C
Bump Temperature (Soldering) Lead-Free.....+260°C
Bump Temperature (Soldering) Lead .....+245°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +13.2V, V_{PP} = +40V to V_{NN} + 200V, V_{NN} = -15V to -160V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$	(Note 2)			V_{NN} + 10		V_{PP} - 10	V
Small-Signal Switch On-Resistance	R_{ONS}	V_{PP} = +40V, V_{NN} = -160V, $V_{COM\_}$ = 0	I_{COM} = 5mA	T_A = 0°C			30	Ω
				T_A = +25°C		26	38	
				T_A = +70°C			48	
			I_{COM} = 200mA	T_A = 0°C			25	
				T_A = +25°C		22	27	
				T_A = +70°C			32	
		V_{PP} = +100V, V_{NN} = -100V, $V_{COM\_}$ = 0	I_{COM} = 5mA	T_A = 0°C			25	
				T_A = +25°C		22	27	
				T_A = +70°C			30	
			I_{COM} = 200mA	T_A = 0°C			18	
				T_A = +25°C		18	24	
				T_A = +70°C			27	
		V_{PP} = +160V, V_{NN} = -40V or V_{PP} = +185V, V_{NN} = -15V, $V_{COM\_}$ = 0	I_{COM} = 5mA	T_A = 0°C			23	
				T_A = +25°C		20	25	
				T_A = +70°C			30	
			I_{COM} = 200mA	T_A = 0°C			22	
				T_A = +25°C		16	25	
				T_A = +70°C			27	
Small-Signal Switch On-Resistance Matching	ΔR_{ONS}	V_{PP} = +100V, V_{NN} = -100V, $V_{COM\_}$ = 0, I_{COM} = 5mA				5	20	%
Large-Signal Switch On-Resistance	R_{ONL}	$V_{COM\_}$ = V_{PP} - 10V, I_{COM} = 1A				15		Ω
Shunt Resistance	R_{INT}	NO_ or COM_ to RGND (MAX4802), switch off			30	35	50	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +13.2V, V_{PP} = +40V to V_{NN} + 200V, V_{NN} = -15V to -160V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Switch-Off Leakage	$I_{COM\_(OFF)}$, $I_{NO\_(OFF)}$	$V_{COM\_}$, $V_{NO\_}$ = V_{PP} - 10V or unconnected; RGND unconnected (MAX4802)	T_A = +25°C		1	4	µA
			T_A = T_{MIN} to T_{MAX}			10	
Switch-Off DC Offset		R_L = 100kΩ (MAX4800/MAX4801), No load (MAX4802)			100	300	mV
Switch-On DC Offset		R_L =100kΩ (MAX4800/MAX4801), No load (MAX4802)			100	500	mV
Switch-Output Peak Current (Note 3)		$I_{COM\_}$ duty cycle ≤ 0.1%	T_A = 0°C	3			A
			T_A = +25°C	2	3		
			T_A = +70°C	2			
Switch-Output Isolation Diode Current (Note 3)		300ns pulse width, 2% duty cycle	V_{PP} – V_{NN} ≤ 200V COM_, NO1–NO7	300			mA
			V_{PP} – V_{NN} ≤ 200V, NO0	30			
			V_{PP} – V_{NN} ≤ 160V COM_, NO_	750			
SWITCH DYNAMIC CHARACTERISITICS							
Off-Isolation (Note 3)	V_{ISO}	f = 5MHz, R_L = 1kΩ, C_L = 15pF		-30	-33		dB
		f = 5MHz, R_L = 50Ω		-58	-77		
Crosstalk (Note 3)	V_{CT}	f = 5MHz, R_L = 50Ω		-60	-80		dB
COM_, NO_ Off-Capacitance (Note 3)	$C_{COM\_(OFF)}$, $C_{NO\_(OFF)}$	$V_{COM\_}$ = 0, $V_{NO\_}$ = 0, f = 1MHz		4	11	18	pF
COM_ On-Capacitance (Note 3)	$C_{COM\_(ON)}$	$V_{COM\_}$ = 0, f = 1MHz		20	36	56	pF
Output-Voltage Spike (Note 3)	V_{SPK}	R_L = 50Ω		-150		+150	mV
Charge Injection	Q	V_{PP} = +40V, V_{NN}= -160V, $V_{COM\_}$ = 0			820		pC
		V_{PP} = +100V, V_{NN} = -100V, $V_{COM\_}$ = 0			600		
		V_{PP} = +160V, V_{NN} = -40V, $V_{COM\_}$ = 0			350		
LOGIC LEVELS							
Logic-Input Low Voltage	V_{IL}	V_{DD} ≥ +4.5V				1.5	V
		V_{DD} < +4.5V				0.75	
Logic-Input High Voltage	V_{IH}	V_{DD} ≥ +4.5V		V_{DD} - 1.5			V
		V_{DD} < +4.5V		V_{DD} - 0.75			
Logic-Input Capacitance (Note 3)	C_{IN}					10	pF
Logic-Input Leakage	I_{IN}			-1		+1	µA
DOUT Low Voltage	V_{OL}	V_{DD} ≥ +4.5V, I_{SINK} = 1mA				0.4	V
		V_{DD} < +4.5V, I_{SINK} = 0.5mA				0.4	V

Low-Charge Injection, 8-Channel, High-Voltage Analog Switches

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +13.2V, V_{PP} = +40V to V_{NN} + 200V, V_{NN} = -15V to -160V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
DOUT High Voltage	V_{OH}	V_{DD} ≥ +4.5V, I_{SOURCE} = 0.5mA			V_{DD} - 0.5			V
		V_{DD} < +4.5V, I_{SOURCE} = 0.25mA			V_{DD} - 0.5			V
POWER SUPPLIES								
V_{DD} Supply Voltage					2.7		13.2	V
V_{PP} Supply Voltage					40		V_{NN} + 200	V
V_{NN} Supply Voltage					-160		-15	V
V_{DD} Supply Quiescent Current	I_{DDQ}	V_{IL} = 0, V_{IH} = V_{DD}, f_{CLK} = 0					15	µA
V_{DD} Supply Dynamic Current	I_{DD}	V_{DD} = +5V, V_{IL} = 0, V_{IH} = +5V, f_{CLK} = 5MHz					4	mA
V_{PP} Supply Quiescent Current	I_{PPQ}	All switches remain on or off, $I_{COM\_(ON)}$ = 5mA				10	50	µA
V_{PP} Supply Dynamic Current	I_{PP}	50kHz output switching frequency with no load	V_{PP} = +40V, V_{NN} = -160V	T_A = 0°C			6.5	mA
				T_A = +25°C			6.5	
				T_A = +70°C			6.5	
			V_{PP} = +100V, V_{NN} = -100V	T_A = 0°C			4.0	
				T_A = +25°C			4.0	
				T_A = +70°C			4.0	
			V_{PP} = +160V, V_{NN} = -40V	T_A = 0°C			4.0	
				T_A = +25°C			4.0	
				T_A = +70°C			4.0	
V_{NN} Supply Quiescent Current	I_{NNQ}	All switches remain on or off, $I_{COM\_(ON)}$ = 5mA				10	50	µA
V_{NN} Supply Dynamic Current	I_{NN}	50kHz output switching frequency with no load	V_{PP} = +40V, V_{NN} = -160V	T_A = 0°C			6.5	mA
				T_A = +25°C			6.5	
				T_A = +70°C			6.5	
			V_{PP} = +100V, V_{NN} = -100V	T_A = 0°C			4.0	
				T_A = +25°C			4.0	
				T_A = +70°C			4.0	
			V_{PP} = +160V, V_{NN} = -40V	T_A = 0°C			4.0	
				T_A = +25°C			4.0	
				T_A = +70°C			4.0	

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +13.2V, V_{PP} = +40V to V_{NN} + 200V, V_{NN} = -15V to -160V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Turn-On Time	t_{ON}	$V_{NO\_}$ = V_{PP} - 10V, R_L = 10kΩ, V_{NN} = -40V to -160V				5	µs
Turn-Off Time	t_{OFF}	$V_{NO\_}$ = V_{PP} - 10V, R_L = 10kΩ, V_{NN} = -40V to -160V				5	µs
Output Switching Frequency	f_{SW}	Duty cycle = 50%				50	kHz
Maximum $V_{COM\_}$, $V_{NO\_}$ Slew Rate	dV/dt	(Note 3)		20			V/ns
LOGIC TIMING (Figure 1)							
CLK Frequency	f_{CLK}	Daisy chaining	V_{DD} ≥ +4.5V			5	MHz
			V_{DD} ≤ +4.5V			2.5	
		No daisy chaining	V_{DD} ≥ +4.5V			10	
			V_{DD} < +4.5V			4	
DIN to CLK Setup Time	t_{DS}	V_{DD} ≥ +4.5V		15			ns
		V_{DD} < +4.5V		40			
DIN to CLK Hold Time	t_{DH}	V_{DD} ≥ +4.5V		35			ns
		V_{DD} < +4.5V		60			
CLK to $\overline{LE}$ Setup Time	t_{CS}	V_{DD} ≥ +4.5V		150			ns
		V_{DD} < +4.5V		300			
$\overline{LE}$ Low-Pulse Width	t_{WL}	V_{DD} ≥ +4.5V		150			ns
		V_{DD} < +4.5V		300			
CLR High-Pulse Width	t_{WC}	V_{DD} ≥ +4.5V		150			ns
		V_{DD} < +4.5V		300			
CLK Rise and Fall Times	t_R, t_F	V_{DD} ≥ +4.5V (Note 3)				1	µs
		V_{DD} < +4.5V (Note 3)				1	
CLK to DOUT Delay	t_{DO}	V_{DD} = +5V ± 10%, C_L ≤ 50pF	T_A = 0°C	55		150	ns
			T_A = +25°C	60		150	
			T_A = +70°C	70		150	
		V_{DD} = +3V ± 10%, C_L ≤ 50pF	T_A = T_{MIN} to T_{MAX}	70		280	

Note 1: Specifications at 0°C are guaranteed by correlation and design. Electrical parameters are tested at worst case conditions.

Note 2: The analog signal input $V_{COM\_}$ and $V_{NO\_}$ must satisfy V_{NN} ≤ ($V_{COM\_}$, $V_{NO\_}$) ≤ V_{PP}, or remain unconnected during power-up and power-down.

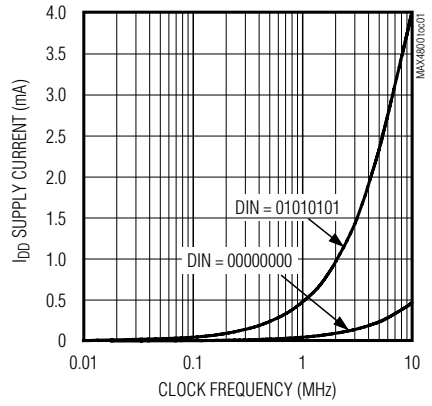
Note 3: Guaranteed by characterization; not production tested.

Low-Charge Injection, 8-Channel, High-Voltage Analog Switches

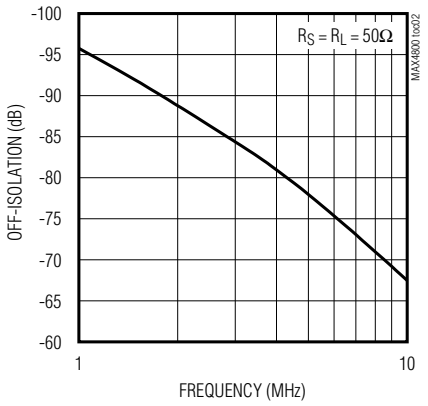
Typical Operating Characteristics

(V_{DD} = +5V, V_{PP} = +100V, V_{NN} = -100V, T_A = +25°C, unless otherwise noted.)

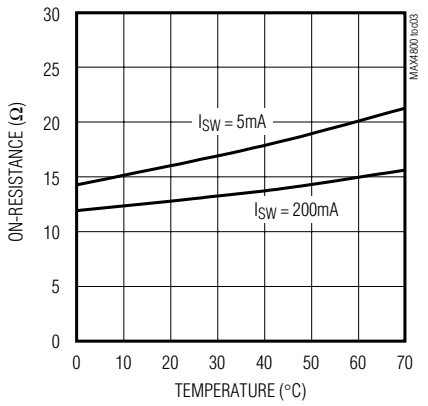
I_{DD} SUPPLY CURRENT vs. CLOCK FREQUENCY



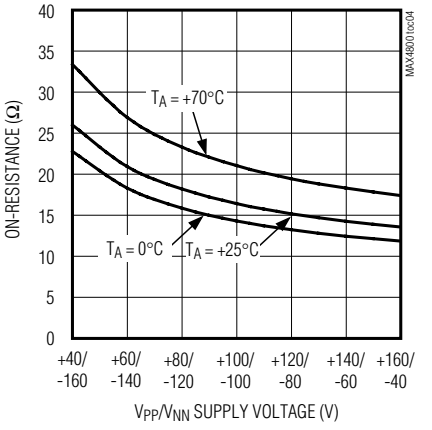
OFF-ISOLATION vs. FREQUENCY



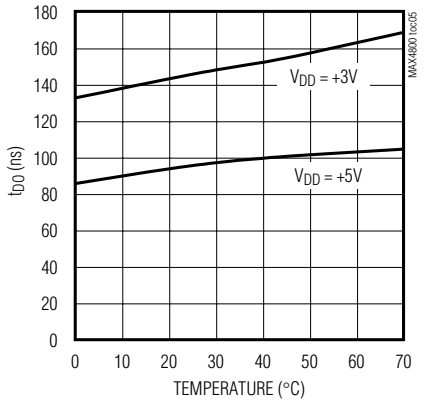
ON-RESISTANCE vs. TEMPERATURE



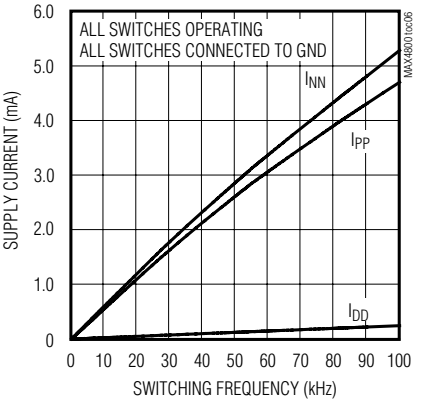
ON-RESISTANCE vs. V_{PP}/V_{NN} SUPPLY VOLTAGE



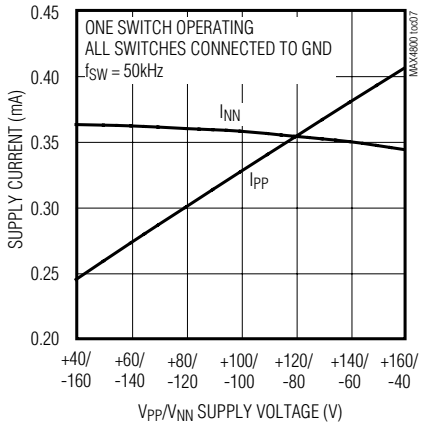
t_{DO} vs. TEMPERATURE



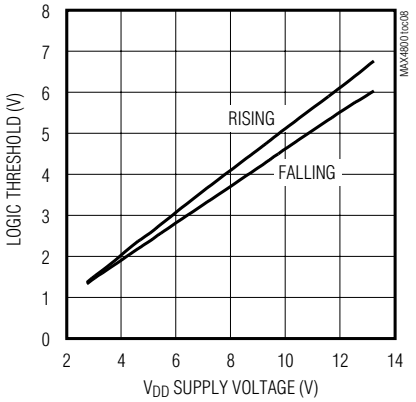
SUPPLY CURRENT vs. SWITCHING FREQUENCY



SUPPLY CURRENT vs. V_{PP}/V_{NN} SUPPLY VOLTAGE



LOGIC THRESHOLD vs. V_{DD} SUPPLY VOLTAGE



Pin Descriptions

PIN					NAME	FUNCTION
MAX4800 TQFP	MAX4800 TQFN	MAX4800 CSBGA	MAX4800 PLCC	MAX4801 PLCC		
1	48	E4	26	26	COM5	Analog Switch 5
2, 4, 6, 7, 9, 11, 13, 15, 17, 19, 21, 23, 26, 27, 30, 31, 32, 38, 40, 42, 44, 46, 48	1, 2, 4, 6, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 34, 37, 39, 41, 43, 45, 47	D6	9, 11, 15	11, 14, 15	N.C.	No Connection. Not connected internally.
3	3	E1	27	27	COM4	Analog Switch 4
5	5	E3	28	28	NO4	Analog Switch 4
8	8	D1	1	1	COM3	Analog Switch 3
10	10	D3	2	2	NO3	Analog Switch 3
12	12	D4	3	3	COM2	Analog Switch 2
14	14	C3	4	4	NO2	Analog Switch 2
16	16	C4	5	5	COM1	Analog Switch 1
18	18	A4	6	6	NO1	Analog Switch 1
20	20	C5	7	7	COM0	Analog Switch 0
22	22	D5	8	8	NO0	Analog Switch 0
24	24	C6	10	9	V_{PP}	Positive High-Voltage Supply. Bypass V_{PP} to GND with a 0.1µF or greater ceramic capacitor.
25	26	C7	12	10	V_{NN}	Negative High-Voltage Supply. Bypass V_{NN} to GND with a 0.1µF or greater ceramic capacitor.
28	29	D7	13	12	GND	Ground
29	30	D9	14	13	V_{DD}	Digital-Supply Voltage. Bypass V_{DD} to GND with a 0.1µF or greater ceramic capacitor.
33	31	E9	16	16	DIN	Serial Data Input
34	32	E7	17	17	CLK	Serial Clock Input
35	33	E6	18	18	$\overline{LE}$	Latch Enable Input, Active Low
36	35	F7	19	19	CLR	Latch Clear Input
37	36	F6	20	20	DOUT	Serial Data Output
39	38	E5	21	21	COM7	Analog Switch 7
41	40	F5	22	22	NO7	Analog Switch 7
43	42	F4	23	23	COM6	Analog Switch 6
45	44	H4	24	24	NO6	Analog Switch 6
47	46	F3	25	25	NO5	Analog Switch 5
—	EP	—	—	—	EP	Exposed Paddle. Connect exposed paddle to V_{NN}.

Low-Charge Injection, 8-Channel, High-Voltage Analog Switches

Pin Descriptions (continued)

PIN				NAME	FUNCTION
MAX4802 TQFP	MAX4802 TQFN	MAX4802 CSBGA	MAX4802 PLCC		
1	48	E4	26	COM5	Analog Switch 5
2, 4, 6, 7, 9, 11,13, 15, 17, 19, 21, 23, 26, 30, 31, 32, 38, 40, 42, 44, 46, 48	1, 2, 4, 6, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 34, 37, 39, 41, 43, 45, 47	—	9, 15	N.C.	Not Connected Internally
3	3	E1	27	COM4	Analog Switch 4
5	5	E3	28	NO4	Analog Switch 4
8	8	D1	1	COM3	Analog Switch 3
10	10	D3	2	NO3	Analog Switch 3
12	12	D4	3	COM2	Analog Switch 2
14	14	C3	4	NO2	Analog Switch 2
16	16	C4	5	COM1	Analog Switch 1
18	18	A4	6	NO1	Analog Switch 1
20	20	C5	7	COM0	Analog Switch 0
22	22	D5	8	NO0	Analog Switch 0
24	24	C6	10	V_{PP}	Positive High-Voltage Supply. Bypass V_{PP} to GND with a 0.1µF or greater ceramic capacitor.
25	26	C7	12	V_{NN}	Negative High-Voltage Supply. Bypass V_{NN} to GND with a 0.1µF or greater ceramic capacitor.
27	28	D6	11	RGND	Bleed Resistor Ground
28	29	D7	13	GND	Ground
29	30	D9	14	V_{DD}	Digital-Supply Voltage. Bypass V_{DD} to GND with a 0.1µF or greater ceramic capacitor.
33	31	E9	16	DIN	Serial Data Input
34	32	E7	17	CLK	Serial Clock Input
35	33	E6	18	$\overline{LE}$	Latch Enable Input, Active Low
36	35	F7	19	CLR	Latch Clear Input
37	36	F6	20	DOUT	Serial Data Output
39	38	E5	21	COM7	Analog Switch 7
41	40	F5	22	NO7	Analog Switch 7
43	42	F4	23	COM6	Analog Switch 6
45	44	H4	24	NO6	Analog Switch 6
47	46	F3	25	NO5	Analog Switch 5
—	EP	—	—	EP	Exposed Paddle. Connect exposed paddle to V_{NN}.

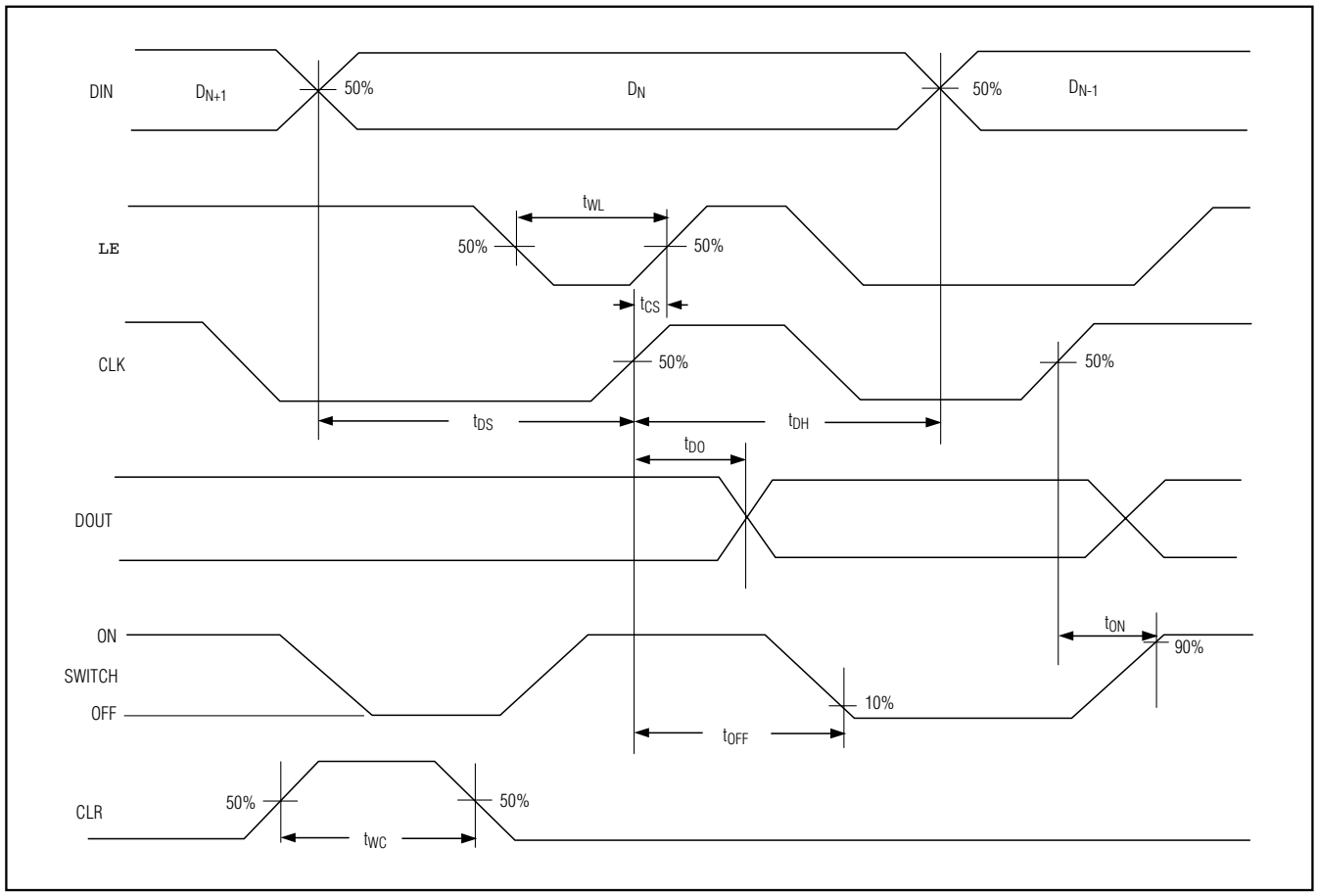


Figure 1. Serial Interface Timing

Detailed Description

The MAX4800/MAX4801/MAX4802 provide high-voltage switching on eight channels for ultrasound imaging and printer applications. The devices utilize BCDMOS process technology to provide eight high-voltage low-charge-injection SPST switches, controlled by a digital interface. Data is clocked into an internal 8-bit shift register and retained by a programmable latch with enable and clear inputs. A power-on reset function ensures that all switches are open on power-up.

The MAX4800/MAX4801/MAX4802 operate with a wide range of high-voltage supplies including: V_{PP}/V_{NN} = +100V/-100V, +185V/-15V, or +40V/-160V. The digital interface operates from a separate V_{DD} supply from +2.7V to +13.2V. Digital inputs DIN, CLK, $\overline{LE}$, and CLR are +13.2V tolerant, independent of the V_{DD} supply voltage. The MAX4802 provides integrated 35kΩ bleed resistors on each switch terminal to discharge capacitive loads.

The MAX4800 and MAX4802 are drop-in replacements for the Supertex HV20220 and HV232, respectively. The MAX4801 is a drop-in replacement for the Supertex HV20320.

Analog Switch

The MAX4800/MAX4801/MAX4802 allow a peak-to-peak analog signal range from V_{NN} + 10V to V_{PP} - 10V. Analog switch inputs must be unconnected, or satisfy $V_{NN} \le (V_{COM\_}, V_{NO\_}) \le V_{PP}$ during power-up and power-down.

High-Voltage Supplies

The MAX4800/MAX4801/MAX4802 allow a wide range of high-voltage supplies. The devices operate with V_{NN} from -160V to -15V and V_{PP} from +40V to V_{NN} + 200V.

Low-Charge Injection, 8-Channel, High-Voltage Analog Switches

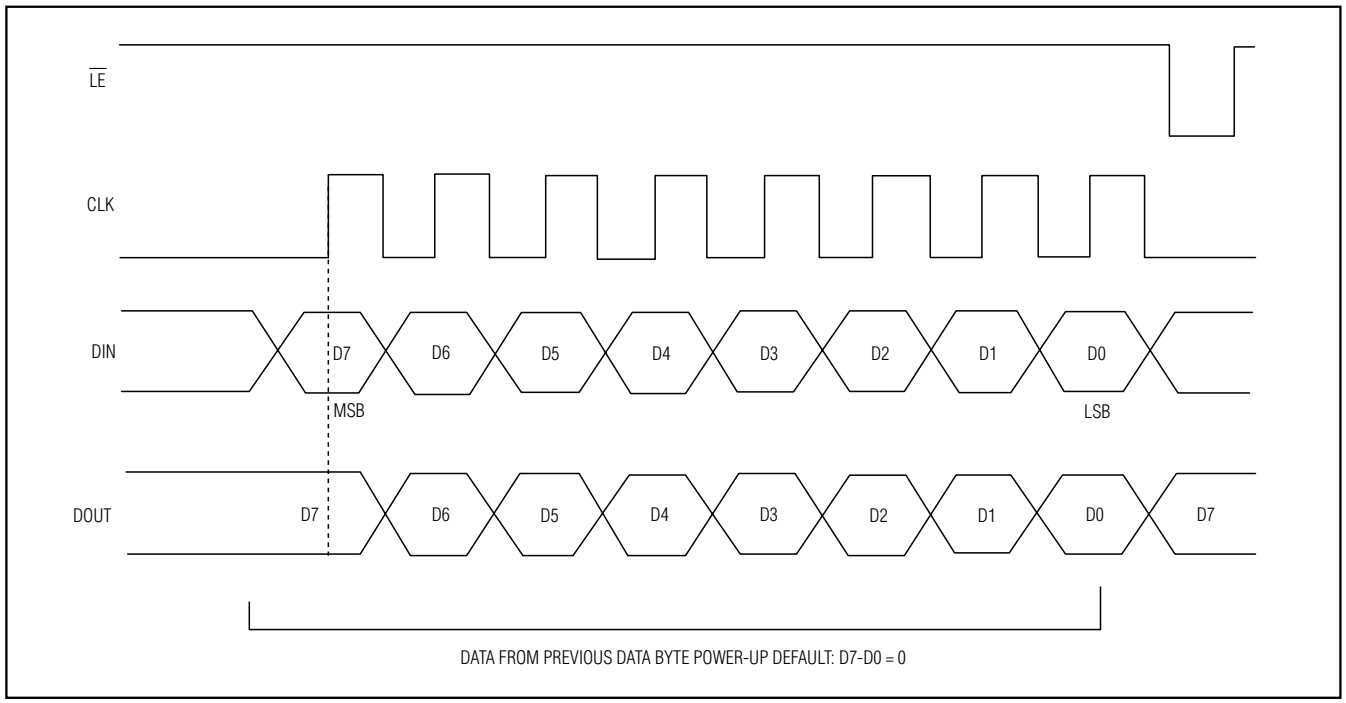


Figure 2. Latch Enable Interface Timing

When V_{NN} is connected to GND (single-supply applications), the devices operate with V_{PP} up to +200V. The V_{PP} and V_{NN} high-voltage supplies are not required to be symmetrical, but the voltage difference V_{PP} - V_{NN} must not exceed 200V.

Bleed Resistors (MAX4802)

The MAX4802 features integrated 35kΩ bleed resistors to discharge capacitive loads such as piezoelectric transducers. Each analog switch terminal is connected to RGND with a bleed resistor.

Serial Interface

The MAX4800/MAX4801/MAX4802 are controlled by a serial interface with an 8-bit serial shift register and transparent latch. Each of the eight data bits controls a single analog switch (see Table 1). Data on DIN is clocked with the most significant bit (MSB) first into the shift register on the rising edge of CLK. Data is clocked out of the shift register onto DOUT on the rising edge of CLK. DOUT reflects the status of DIN, delayed by eight clock cycles (see Figures 1 and 2).

Latch Enable ($\overline{LE}$)

Drive $\overline{LE}$ logic-low to change the contents of the latch and update the state of the high-voltage switches (Figure 2). Drive $\overline{LE}$ logic-high to freeze the contents of the latch and prevent changes to the switch states. To reduce noise due to clock feedthrough, drive $\overline{LE}$ logic-high while data is clocked into the shift register. After the data shift register is loaded with valid data, pulse $\overline{LE}$ logic-low to load the contents of the shift register into the latch.

Latch Clear (CLR)

The MAX4800/MAX4801/MAX4802 feature a latch clear input. Drive CLR logic-high to reset the contents of the latch to zero and open all switches. CLR does not affect the contents of the data shift register. Pulse $\overline{LE}$ logic-low to reload the contents of the shift register into the latch.

Power-On Reset

The MAX4800/MAX4801/MAX4802 feature a power-on reset circuit to ensure all switches are open at power-on. The internal 8-bit serial shift register and latch are set to zero on power-up.

Table 1. Serial Interface Programming

DATA BITS								CONTROL BITS		FUNCTION							
D0 (LSB)	D1	D2	D3	D4	D5	D6	D7 (MSB)	$\overline{LE}$	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

X = Don't Care

Applications Information

Logic Levels

The MAX4800/MAX4801/MAX4802 digital interface inputs CLK, DIN, $\overline{LE}$, and CLR are tolerant of up to +13.2V, independent of the V_{DD} supply voltage, allowing compatibility with higher voltage controllers.

Daisy Chaining Multiple Devices

Digital output DOUT is provided to allow the connection of multiple MAX4800/MAX4801/MAX4802 devices by daisy chaining (Figure 3). Connect each DOUT to the DIN of the subsequent device in the chain. Connect CLK, $\overline{LE}$, and CLR inputs of all devices, and drive $\overline{LE}$ logic-low to update all devices simultaneously. Drive CLR high to open all the switches simultaneously. Additional shift registers may be included anywhere in series with the MAX4800/MAX4801/MAX4802 data chain.

Supply Sequencing and Bypassing

The MAX4800/MAX4801/MAX4802 do not require special sequencing of the V_{DD}, V_{PP}, and V_{NN} supply voltages; however, analog switch inputs must be unconnected, or satisfy $V_{NN} \le (V_{COM\_}, V_{NO\_}) \le V_{PP}$ during power-up and power-down. Bypass V_{DD}, V_{NN}, and V_{PP} to GND with a 0.1µF ceramic capacitor as close to the device as possible.

Exposed Paddle

The MAX4800 and MAX4802 provide an exposed paddle for improved thermal performance in the TQFN package. Connect the exposed paddle to V_{NN}.

Chip Information

PROCESS: BCDMOS

CONNECT EXPOSED PADDLE TO V_{NN}

Low-Charge Injection, 8-Channel, High-Voltage Analog Switches

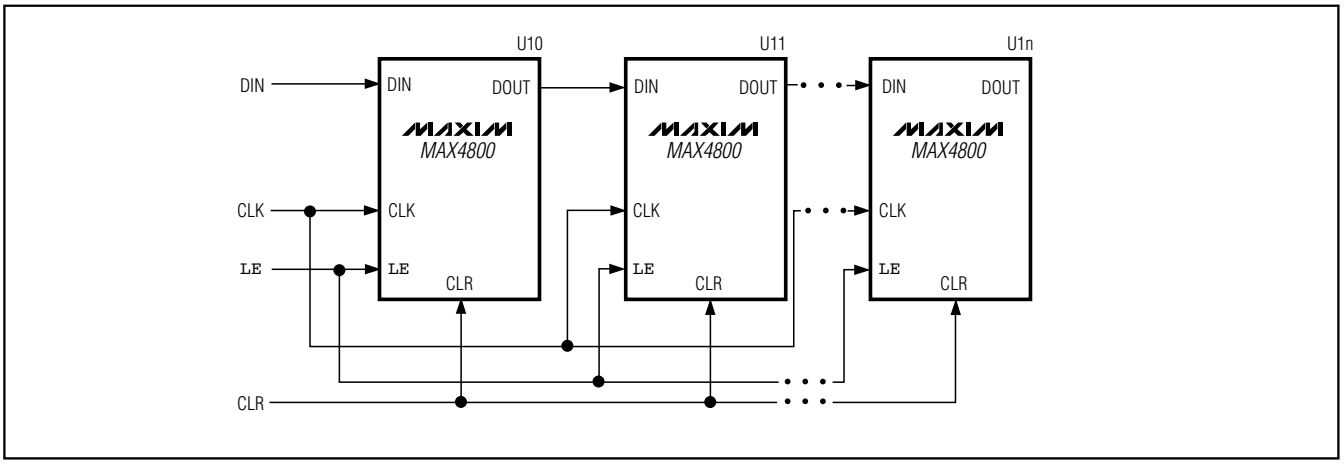
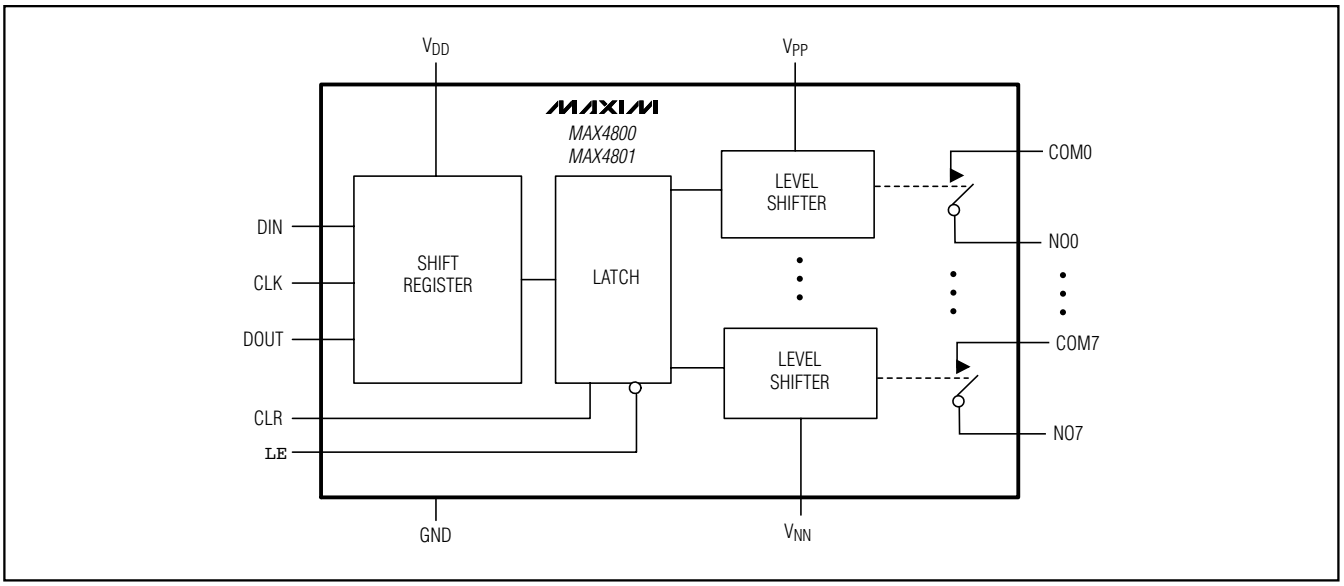
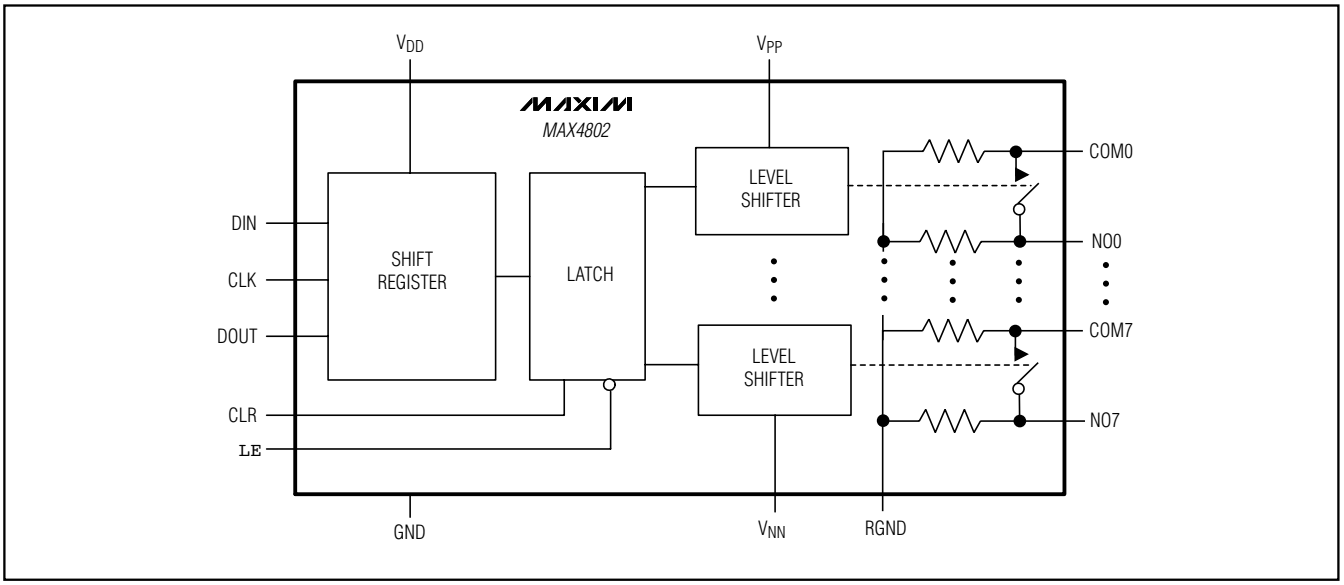


Figure 3. Interfacing Multiple Devices by Daisy-Chaining

Functional Diagrams

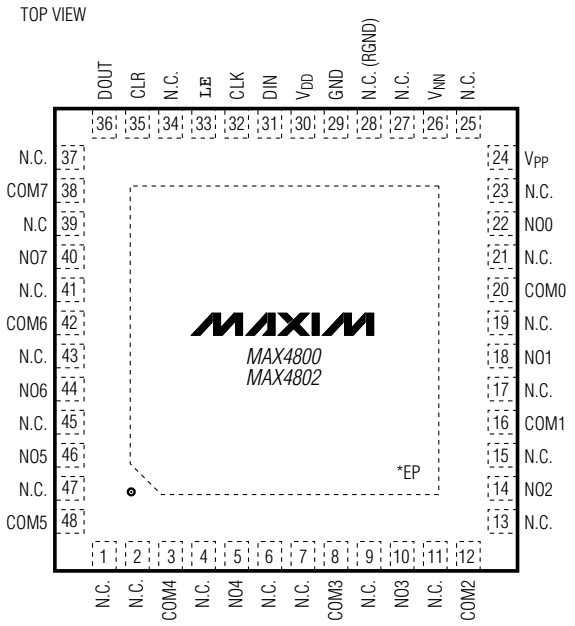


Functional Diagrams (continued)



Low-Charge Injection, 8-Channel, High-Voltage Analog Switches

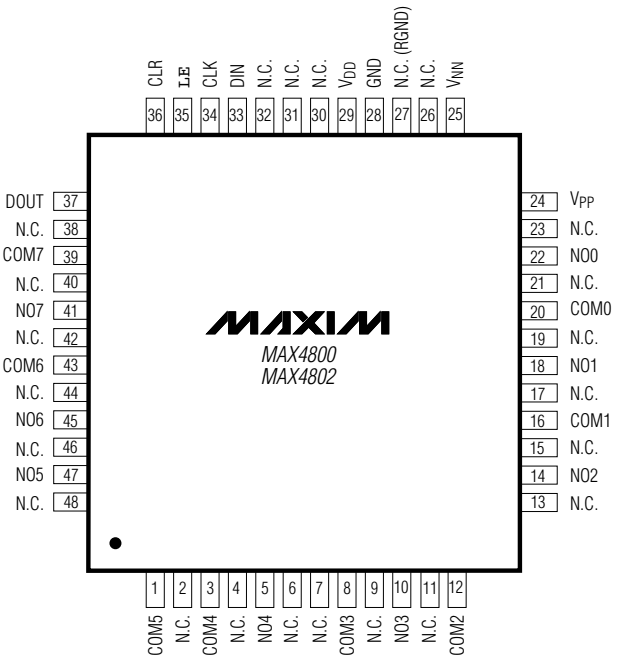
Pin Configurations



TQFN
6mm x 6mm

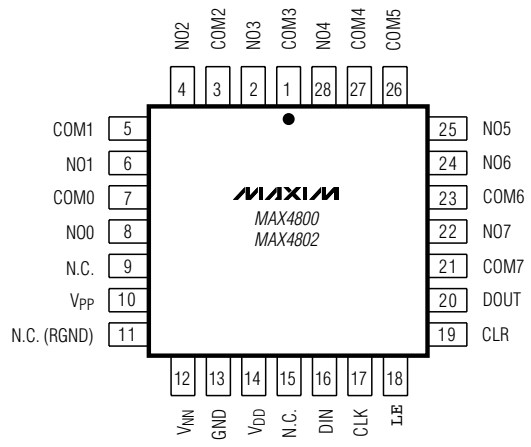
*EXPOSED PADDLE CONNECTED TO V_{NN}

()MAX4802 ONLY



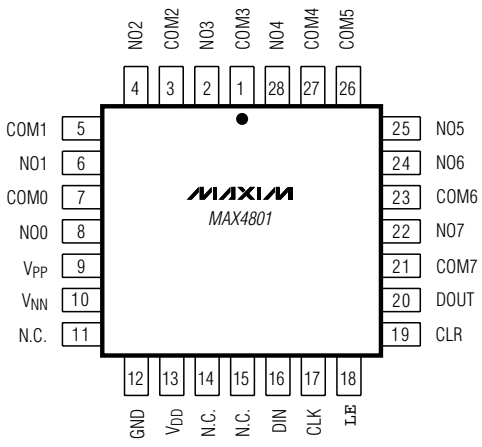
TQFP
7mm x 7mm

()MAX4802 ONLY



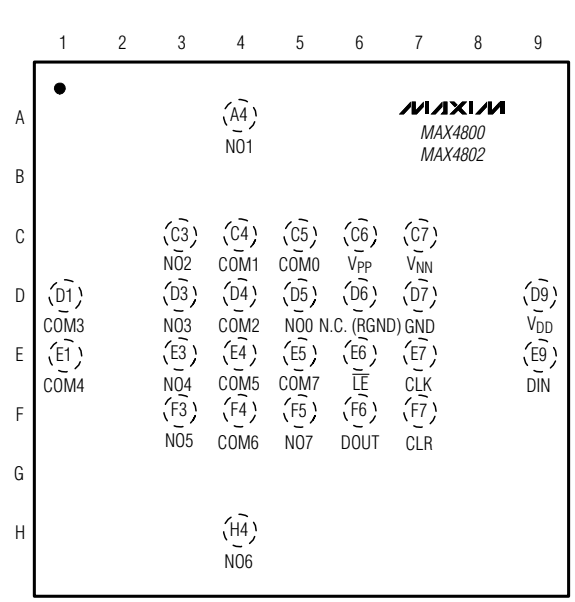
PLCC

()MAX4802 ONLY



PLCC

Pin Configurations (continued)



CSBGA

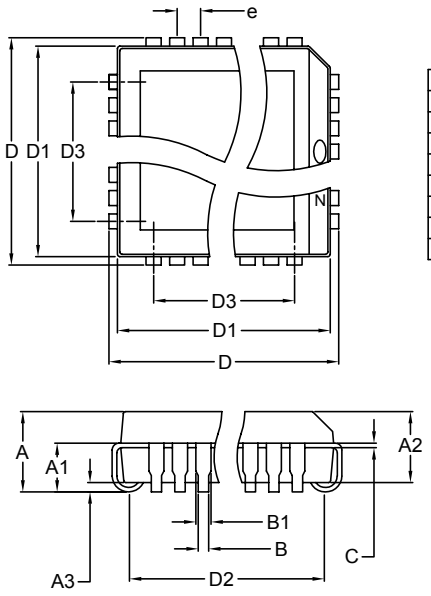
()MAX4802 ONLY

Low-Charge Injection, 8-Channel, High-Voltage Analog Switches

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PLCC.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.20	4.57
A1	0.090	0.120	2.29	3.04
A2	0.145	0.156	3.69	3.96
A3	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
e	0.050		1.27	

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MO047
D	0.385	0.395	9.78	10.03	20	AA
D1	0.350	0.356	8.89	9.04		
D2	0.290	0.330	7.37	8.38		
D3	0.200 REF		5.08 REF			
D	0.485	0.495	12.32	12.57	28	AB
D1	0.450	0.456	11.43	11.58		
D2	0.390	0.430	9.91	10.92		
D3	0.300 REF		7.62 REF			
D	0.685	0.695	17.40	17.65	44	AC
D1	0.650	0.656	16.51	16.66		
D2	0.590	0.630	14.99	16.00		
D3	0.500 REF		12.70 REF			
D	0.785	0.795	19.94	20.19	52	AD
D1	0.750	0.756	19.05	19.20		
D2	0.690	0.730	17.53	18.54		
D3	0.600 REF		15.24 REF			
D	0.985	0.995	25.02	25.27	68	AE
D1	0.950	0.958	24.13	24.33		
D2	0.890	0.930	22.61	23.62		
D3	0.800 REF		20.32 REF			

NOTES:

1. D1 DOES NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .20mm (.008") PER SIDE.
3. LEADS TO BE COPLANAR WITHIN .10mm.
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MO047-XX AS SHOWN IN TABLE.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

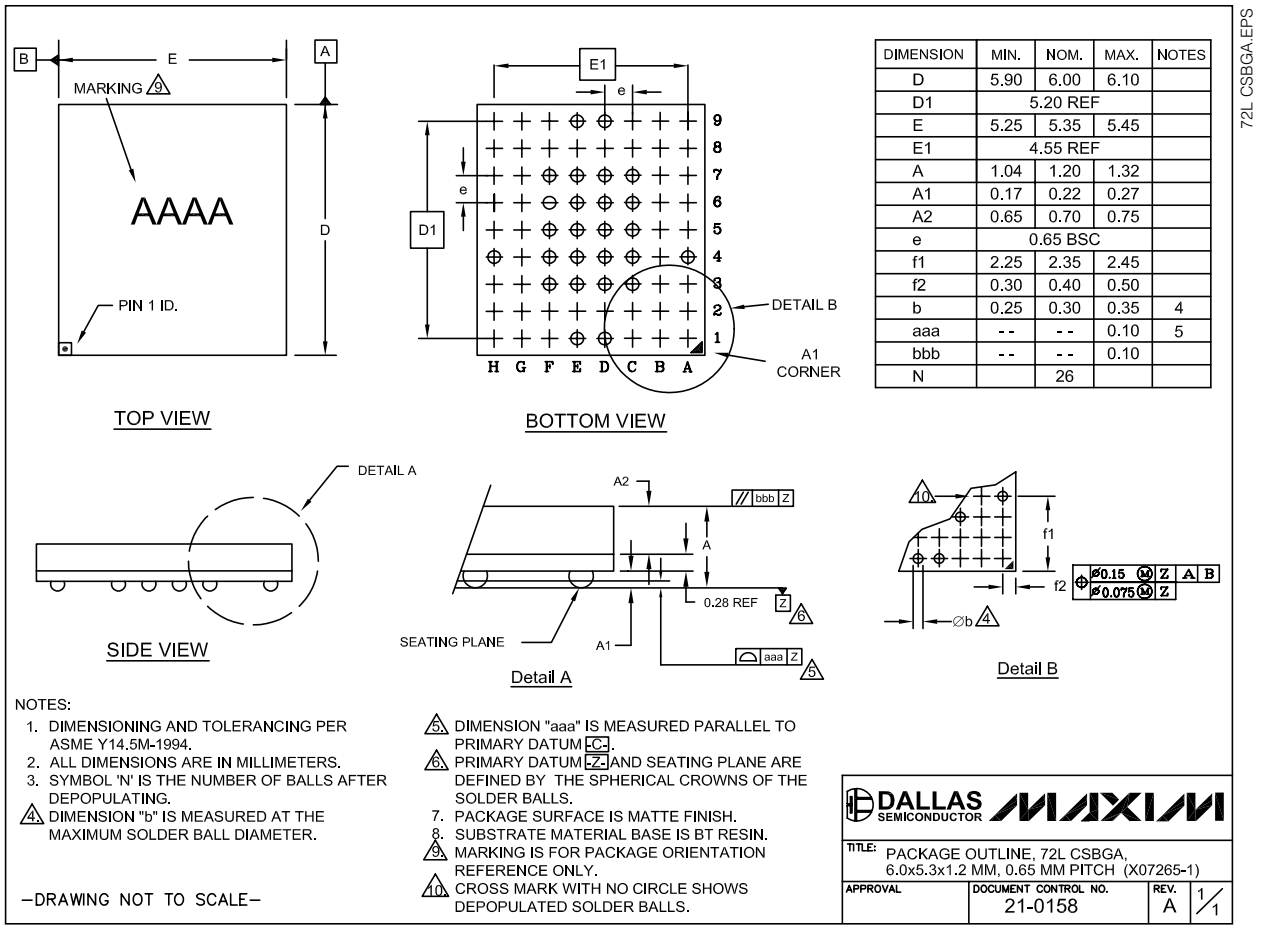
PROPRIETARY INFORMATION

TITLE: FAMILY PACKAGE OUTLINE: 20L, 28L, 44L, 52L, 68L PLCC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0049	D	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



DIMENSION	MIN.	NOM.	MAX.	NOTES
D	5.90	6.00	6.10	
D1		5.20 REF		
E	5.25	5.35	5.45	
E1		4.55 REF		
A	1.04	1.20	1.32	
A1	0.17	0.22	0.27	
A2	0.65	0.70	0.75	
e		0.65 BSC		
f1	2.25	2.35	2.45	
f2	0.30	0.40	0.50	
b	0.25	0.30	0.35	4
aaa	--	--	0.10	5
bbb	--	--	0.10	
N		26		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. SYMBOL 'N' IS THE NUMBER OF BALLS AFTER DEPOPULATING.
4. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER.
5. DIMENSION "aaa" IS MEASURED PARALLEL TO PRIMARY DATUM -C-.
6. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE IS MATTE FINISH.
8. SUBSTRATE MATERIAL BASE IS BT RESIN.
9. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. CROSS MARK WITH NO CIRCLE SHOWS DEPOPULATED SOLDER BALLS.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

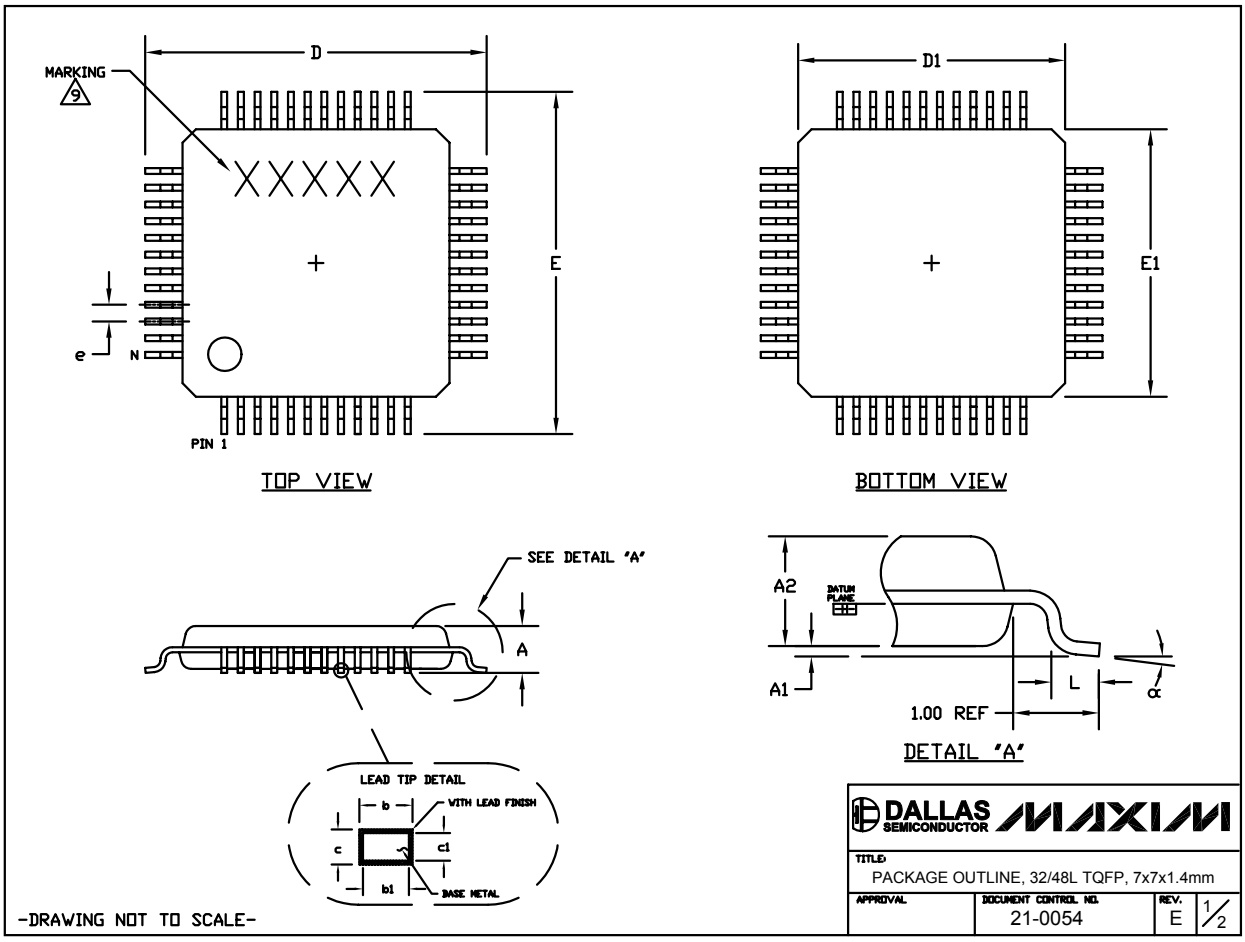
TITLE: PACKAGE OUTLINE, 72L CSBGA, 6.0x5.3x1.2 MM, 0.65 MM PITCH (X07265-1)

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0158	A	1/1

Low-Charge Injection, 8-Channel, High-Voltage Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟H⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. ⚠ MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. NUMBER OF LEADS ARE SHOWN FOR REFERENCE ONLY.

JEDEC VARIATION				
	BBA		BBC	
	MIN.	MAX.	MIN.	MAX.
A	--	1.60	--	1.60
A_1	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D_1	6.90	7.10	6.90	7.10
E	8.90	9.10	8.90	9.10
E_1	6.90	7.10	6.90	7.10
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
b1	0.30	0.40	0.17	0.23
c	0.09	0.20	0.09	0.20
c1	0.09	0.16	0.09	0.16
N	32		48	
α	0°	7°	0°	7°

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

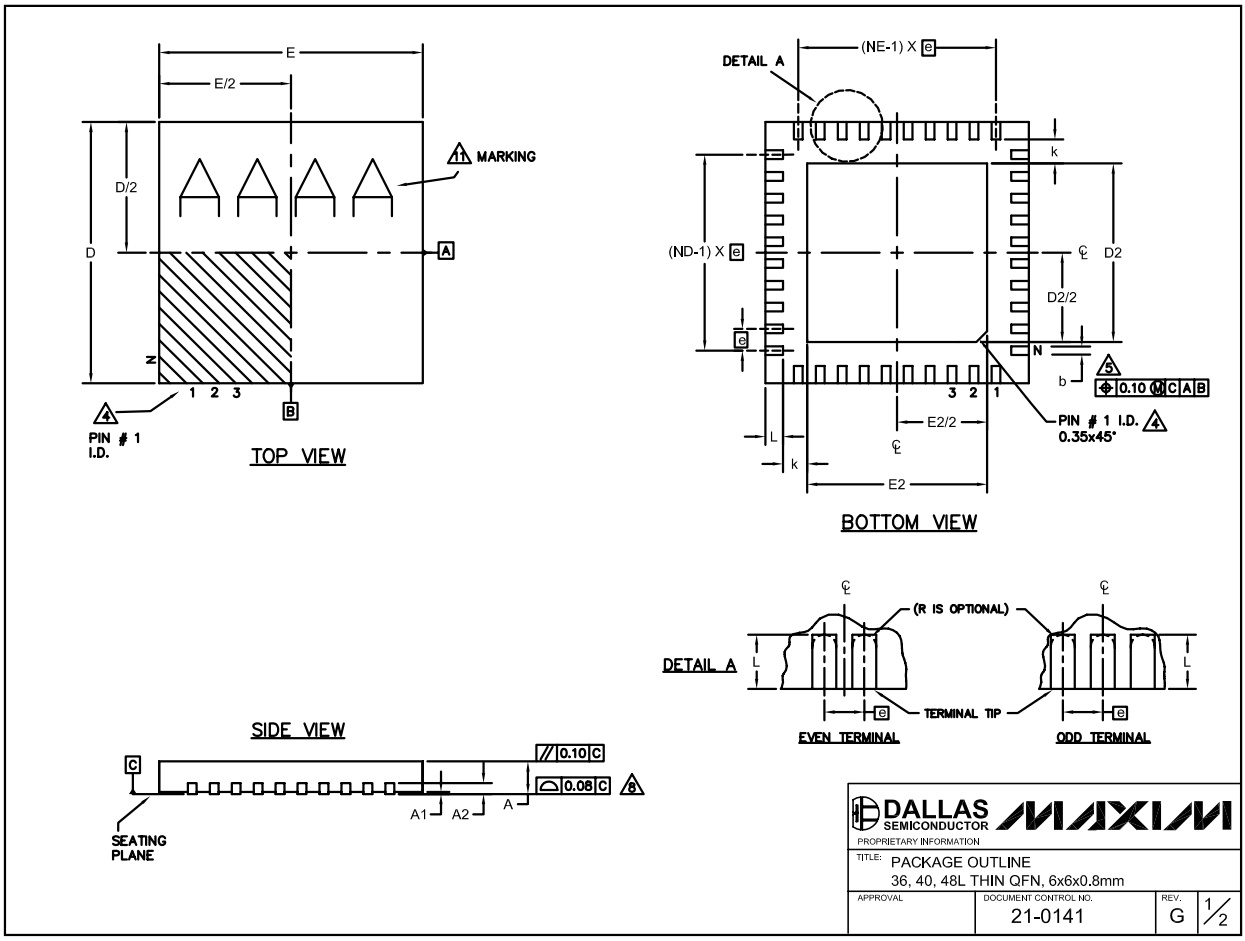
TITLE: PACKAGE OUTLINE, 32/48L TQFP, 7x7x1.4mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0054	E	2/2

Low-Charge Injection, 8-Channel, High-Voltage Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	G	2/2

Revision History

Pages changed at Rev 1: 1, 7, 8, 14, 18, 19, 20, 21

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