

SiGe – Low-Noise Amplifier (1900 MHz)



Description

The TST0951 is a low-noise amplifier (LNA) in SiGe technology. This LNA offers the possibility to apply a gain switching through a control input pin, and provides a power-down mode function for extending the battery operation time.

In low-gain mode, the output drive capability is not reduced, resulting in improved intermodulation performance. The nominal gain is very precise and has max. ± 1.0 dB gain variation over full temperature range and supply-voltage range.

Electrostatic sensitive device.
Observe precautions for handling.



Features

- Input frequency 1800 to 2000 MHz
- Low noise figure at high gain mode (< 3 dB)
- Precise gain (19 dB, ± 1.0 dB)
- Low- / high gain mode
- High gain flatness (± 0.3 dB max.)
- Power-down function
- High reverse isolation (min. -40 dB)
- Small package (TSSO8)

Block Diagram

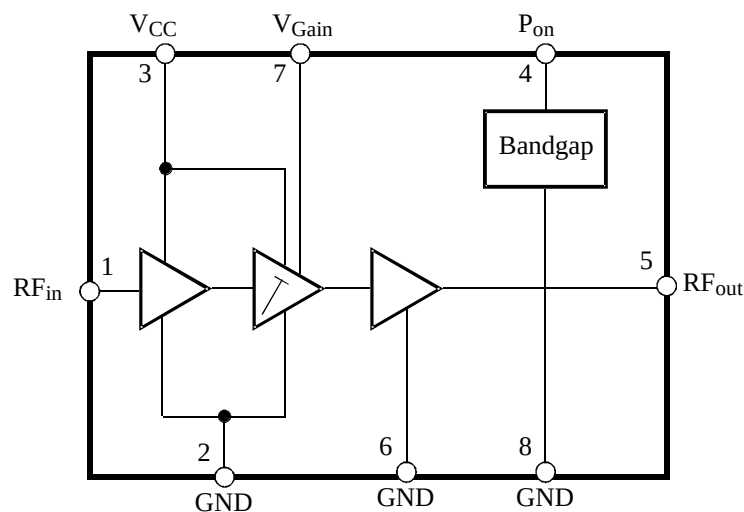


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
TST0951B-MFDG3	TSSO8	Taped and reeled

Pin Description

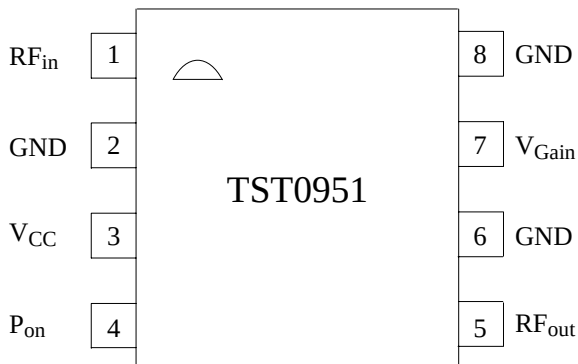


Figure 2. Pinning

Pin	Symbol	Function
1	RF _{in}	RF input
2	GND	Ground
3	V _{CC}	Supply voltage
4	P _{on}	Power-down input
5	RF _{out}	RF output
6	GND	Ground
7	V _{Gain}	Gain switching input
8	GND	Ground

Functional Description

The TST0951 is a very precise amplifier, especially designed for DCS/ PCS telephone applications. The circuit consists of three stages. By attenuating the output signal of the first stage, the complete amplifier gain is reduced and the intermodulation behavior is improved.

Absolute Maximum Ratings

All voltages are referred to GND (Pins 2, 6 and 8)

Parameters	Symbol	Min.	Max.	Unit
Supply voltage Pin 3	V _{CC}	2.7	3.3	V
Junction temperature	T _j	-40	+125	°C
Storage temperature	T _{stg}	-40	+150	°C
Input power Pin 1	RF _{in}	-	-10	dBm
Power-down input Pin 4	P _{on}	0	V _{CC}	V
Gain switching input Pin 7	V _{Gain}	0	V _{CC}	V

Solder Reflow Profile (SMD Packages)

Parameters	Symbol	Value	Unit
Maximum heating rate	T _D	1 to 3	°C/s
Peak temperature in preheat zone	T _{PH}	100 to 140	°C
Duration of time above melting point of solder	t _{MP}	Min. 10 / Max. 130	s
Peak reflow temperature	T _{Peak}	220 to 225	°C
Maximum cooling rate	T _{Peak}	2 to 4	°C/s

Wave Soldering (Through-Hole Packages)

Parameters	Symbol	Value	Unit
Maximum lead temperature (5 s)	T _D	260	°C

Operation Range

All voltages are referred to GND (Pins 2, 6 and 8)

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	2.7	2.8	2.9	V
Ambient temperature	T_{amb}	-20		+70	°C
Input frequency	RF_{in}	1800		2000	MHz

Note for biasing:

Apply first V_{CC} , then P_{on} and V_{Gain} (see absolute maximum ratings)

Electrical Characteristics

Test conditions: $V_{CC} = +2.8$ V, $T_{amb} = +25^{\circ}\text{C}$, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power supply						
Supply voltage	Pin 3	V_{CC}	2.7	2.8	2.9	V
Current consumption						
active mode		I_a		10	12	mA
power-down mode		I_{pd}		50	200	μA
RF input / output						
Input impedance *)	Pin 1	Z_i		50		Ω
Output impedance *)	Pin 5	Z_o		50		Ω
Frequency band		F_{in}	1800		2000	MHz
Nominal gain	Pin 1 to 5	G	18	19	20	dB
Gain attenuation related to nominal gain	Pin 1 to 5	ΔG	17	18	19	dB
Gain flatness	Pin 1 to 5		-0.3		+0.3	dB
Noise figure	Pin 1 to 5			9	20	dB
in low-gain mode		NF			3.0	dB
in high-gain mode		NF				dB
Input VSWR *)	LNA active					
in low-gain mode	Pin 1	VSWR			2:1	
in high-gain mode		VSWR			2:1	
Output VSWR *)	LNA active					
PON = '1'	Pin 5	VSWR			2:1	
LNA inactive						
PON = '0'	Pin 5	VSWR			3:1	
Input 1 dB compression point						
in low-gain mode	Pin 1 to 5		-16			dBm
in high-gain mode			-21			dBm
Input intercept point 3rd order						
in low-gain mode	Pin 1 to 5		-7			dBm
in high-gain mode			-12			dBm
Reverse isolation						
in low-gain mode	Pin 5 to 1		40			dB
in high-gain mode			40			dB
Control function						
Control inputs threshold						
high level	Pins 4 and 7	V_{TH}	$0.97 \times V_{CC}$			V
low level		V_{TH}			$0.03 \times V_{CC}$	V
Leakage current on control inputs low level	Pins 4 and 7	I_l			100	μA

*) with external matching (see application circuit)

Power Down Logic

Level	P _{on}	Power Status
	'0'	Power OFF
	'1'	Power ON

Gain Control Logic

Gain Level	V _{Gain}	Gain
	'0'	Minimum gain
	'1'	Maximum gain

Test Circuit

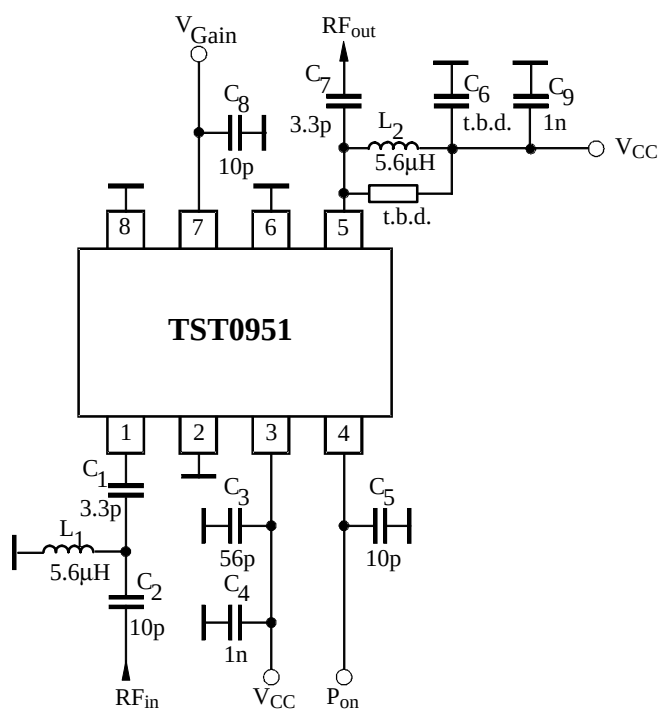
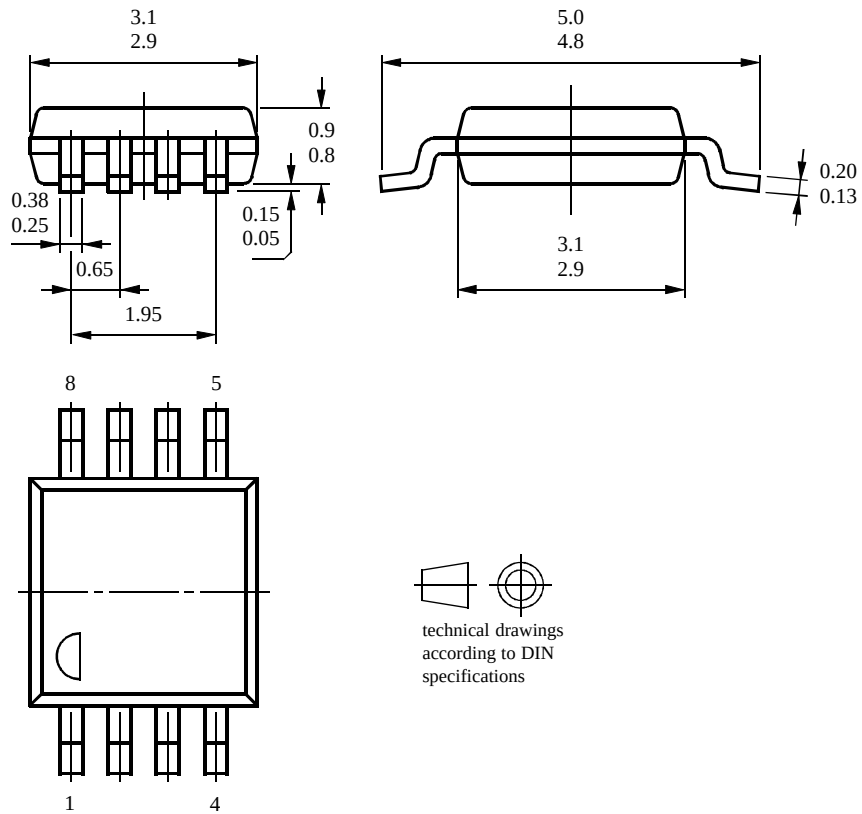


Figure 3. Test circuit

Package Information

Package TSSO8

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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Data sheets can also be retrieved from the Internet: <http://www.temic-semi.com>

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