TOSHIBA CCD LINEAR IMAGE SENSOR CCD(Charge Coupled Device)

# TCD1500C

The TCD1500C is a high sensitive and low dark current 5340-elements linear image sensor. The sensor can be used for facsimile, imagescanner and OCR. The signal preprocessing circuit which is composed of Sample and Hold circuit and Pre-amplifier circuit. The device contains a row of 5340 photodiodes, which provide a 16 lines/mm (400DPI) across a A3 size paper and besides 24 lines/mm (600DPI) across a A4 size paper.



Number of Image Sensing Elements: 5340

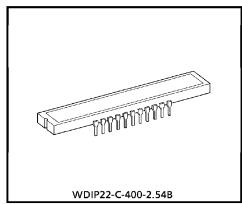
Image Sensing Element Size :  $7\mu m$  by  $7\mu m$  on  $7\mu m$ 

Photo Sensing Region : High sensitive pn photodiode

Clock : 2 phase

Internal Circuit : S/H circuit, Pre-Amplifier circuit

**Package** : 22 pin cerdip



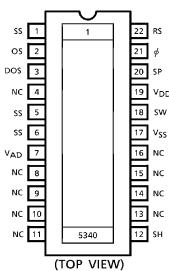
Weight: 5.4g (Typ.)

#### **MAXIMUM RATINGS** (Note 1)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	Vφ		V
Shift Pulse Voltage	V <sub>SH</sub>		٧
Reset Pulse Voltage	V <sub>RS</sub>		V
Sample and Hold Pulse Voltage	V <sub>SP</sub>	-0.3~15	٧
Power Supply Voltage (Analog)	V <sub>AD</sub>		V
Power Supply Voltage (Driver)	V <sub>DD</sub>		٧
Operating Temperature	T <sub>opr</sub>	<b>- 25∼60</b>	°C
Storage Temperature	T <sub>stg</sub>	<b>- 40∼100</b>	°C

(Note 1) All voltage are with respect to SS and VSS terminals (Ground).

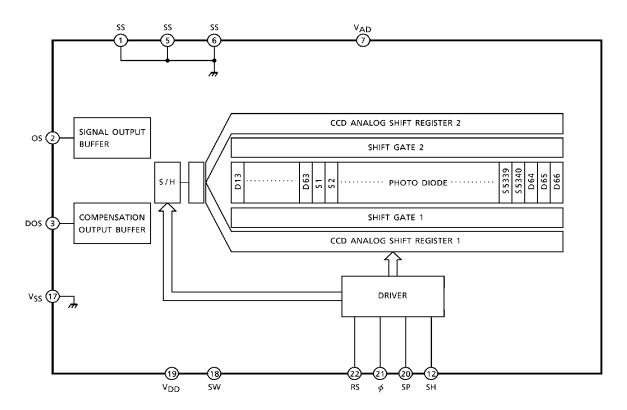
# PIN CONNECTIONS



■ TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

1997-06-30 1/13

#### **CIRCUIT DIAGRAM**



#### **PIN NAMES**

ø	Clock
SH	Shift Gate
RS	Reset Gate
SP	Sample Hold Gate
OS	Signal Output
DOS	Compensation Output
$V_{AD}$	Power (Analog)
$v_{DD}$	Power (Driver)
SS	Ground (Analog)
VSS	Ground (Driver)
SW	Final Clock Select Switch
NC	Non Connection

961001EBA2'

1997-06-30 2/13

The products described in this document are subject to foreign exchange and foreign trade control laws.
The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
The information contained herein is subject to change without notice.

#### **OPTICAL / ELECTRICAL CHARACTERISTICS**

(Ta = 25°C,  $V_{AD}$  = 12V,  $V_{DD}$  = 12V,  $V_{\phi}$  =  $V_{SH}$  =  $V_{RS}$  = 5V (PULSE),  $f_{\phi}$  = 0.5MHz,  $f_{RS}$  = 1MHz,  $t_{INT}$  (INTEGRATION TIME) = 10ms, LIGHT SOURCE = DAYLGIHT FLUORESCENT LAMP)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Sensitivity	R	3.8	4.8	5.8	V / lx·s	
District November 11 15 and	PRNU	_	_	10	%	(Note 2)
Photo Response Non Uniformity	PRNU (3)	_	3	8	mV	(Note 3)
Register Imbalance	RI	_	_	3	%	(Note 4)
Saturation Output Voltage	V <sub>SAT</sub>	1.0	1.5	_	\ \	(Note 5)
Saturation Exposure	SE	0.17	0.3	_	lx∙s	(Note 6)
Dark Signal Voltage	V <sub>DRK</sub>	_	_	2	mV	(Note 7)
Dark Signal Non Uniformity	DSNU	_	_	3	mV	(Note 7)
Analog Current Dissipation	I <sub>AD</sub>	_	_	20	mA	
Driver Current Dissipation	IDD	_	_	10	mA	
Total Transfer Efficiency	TTE	92	_	_	%	
Output Impedance	ZO	_	0.5	1	kΩ	
Dynamic Range	DR	_	1500	_		(Note 8)
DC Signal Output Voltage	Vos	3.5	4.5	6.0	V	(Note 9)
DC Compensation Output Voltage	V <sub>DOS</sub>	3.5	4.5	6.0	٧	(Note 9)
DC Mismatch Voltage	Vos-V <sub>DOS</sub>	_	_	100	mV	

(Note 2) Measured at 50% of SE (Typ.)

Definition of PRNU : PRNU =  $\frac{\Delta \chi}{\overline{\gamma}}$  × 100 (%)

Where  $\overline{\chi}$  is average of total signal outputs and  $\Delta \chi$  is the maximum deviation from  $\overline{\chi}$  under uniform illumination.

- (Note 3) PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (Typ.)
- (Note 4) Measured at 50% of SE (Typ.)

RI is defined as follows:

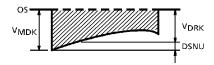
RI = 
$$\frac{\sum_{N=1}^{5339} |\chi_{N} - \chi_{N} + 1|}{5339 \times \overline{\chi}} \times 100 (\%)$$

Where  $\chi n$  and  $\chi n + 1$  are signal outputs of each pixel.  $\overline{\chi}$  is average of total signal outputs.

(Note 5) V<sub>SAT</sub> is defined as minimum saturation output voltage of all effective pixels.

(Note 6) Definition of SE : SE = 
$$\frac{V_{SAT}}{R}$$
 (Ix·s)

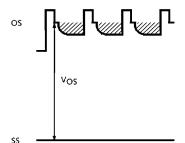
(Note 7)  $V_{DRK}$  is defined as average dark signal voltage of all effective pixels. DSNU is defined as different voltage between  $V_{DRK}$  and  $V_{MDK}$  when  $V_{MDK}$  is maximum dark signal voltage.

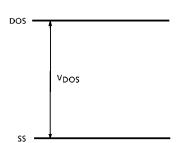


(Note 8) Definition of DR : DR =  $\frac{V_{SAT}}{V_{DRK}}$ 

 $V_{\mbox{\footnotesize{DRK}}}$  is proportional to  $t_{\mbox{\footnotesize{INT}}}$  (Integration Time). So the shorter  $t_{\mbox{\footnotesize{INT}}}$  condition makes wider DR value.

(Note 9) DC signal output voltage and DC compensation output voltage are defined as follows:





### **OPERATING CONDITION**

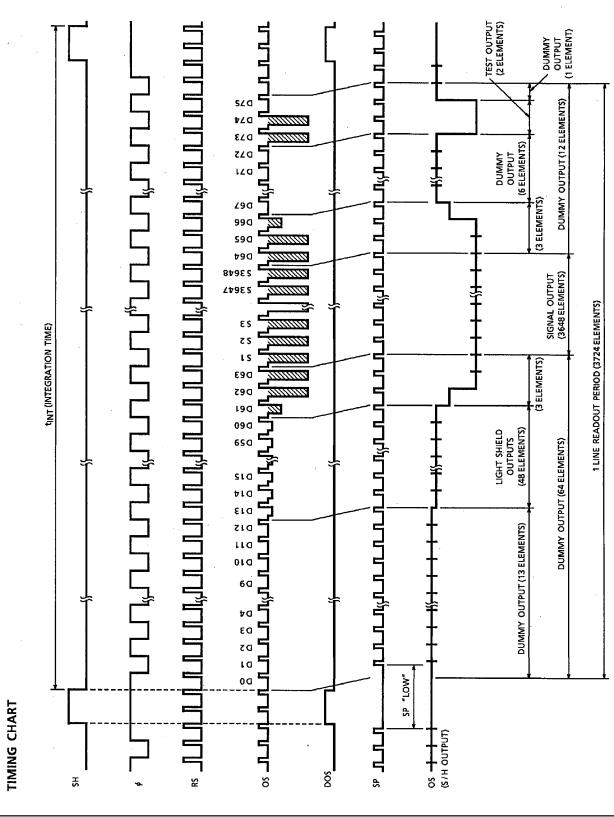
CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Clask Bulsa Valtaga	Clock Pulse Voltage "H"Level	4.5	5.0	5.5	V	
Clock ruise voltage	"L" Level	$V_\phi$	0	_	0.5	'
Shift Bulsa Valtaga	hift Dulco Veltage	4.5	5.0	5.5	V	
Shift Pulse Voltage	"L" Level	$V_{SH}$	0		0.5	
Baset Bules Valtage	"H"Level	V <sub>RS</sub>	4.5	5.0	5.5	V
Reset Pulse Voltage	"L" Level		0		0.5	
Sample and Hold Pulse Voltage	"H"Level	VSP	4.5	5.0	5.5	V
(Note 9)	"L" Level		0	_	0.5	V
Switch Voltage	"H"Level		4.5	5.0	5.5	V
	"L" Level	$V_{SW}$	0	_	0.5	V
Power Supply Voltage (Analog)		$V_{AD}$	11.4	12	13	V
Power Supply Voltage ((Driver)		$V_{DD}$	11	12	13	V

(Note 9) Supply "H" level to SP terminal when sample-and-hold circuitry is not used.

## **CLOCK CHARACTERISTICS** (Ta = 25°C)

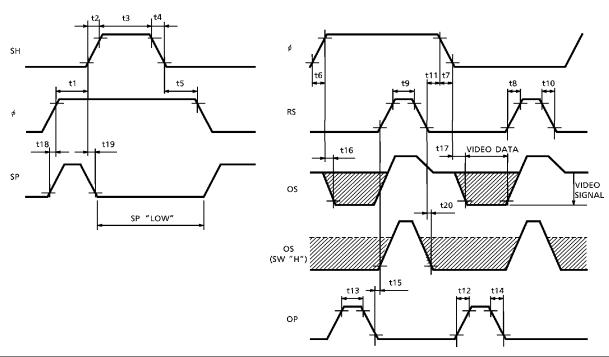
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	f <sub>¢</sub>	_	0.5	4.0	MHz
Reset Pulse Frequency	fRS	_	1	8.0	MHz
Sample and Hold Pulse Frequency	fsp	_	1	8.0	MHz
Clock Capacitance	C <sub>∅</sub>	_	_	10	рF
Final Stage Clock Capacitance	C <sub>\psi</sub>	_	_	10	pF
Shift Gate Capacitance	C <sub>SH</sub>	_	_	10	рF
Sample and Hold Gate Capacitance	C <sub>SP</sub>	_	_	10	pF
Switch Capacitance	C <sub>SW</sub>	_	_	10	pF

1997-06-30 5/13



1997-06-30 6/13

### TIMING REQUIREMENTS

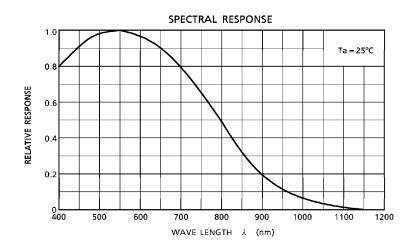


CHARACTERISTIC	SYMBOL	MIN.	TYP. (Note 10)	MAX.	UNIT
Pulse Timing of SH and $\phi$ 1	t1, t5	60 (Note 12)	1000	_	ns
SH Pulse Rise Time, Fall Time	t2, t4	0	50	_	ns
SH Pulse Width	t3	500	1000	_	ns
$\phi$ Rise Time, Fall Time	t6, t7	0	50	_	ns
RS Rise Time, Fall Time	t8, t10	0	20	_	ns
RS Pulse Width	t9	20	250	_	ns
Pulse Timing of $\phi$ and RS	t11	0	100	_	ns
SP Rise Time, Fall Time	t12, t14	10	100	_	ns
SP Pulse Width	t13	20	100	_	ns
Pulse Timing of SP and RS	t15	0	50	_	ns
Video Data Dalay Time (Nata 11)	t16, t17	_	75	90	ns
Video Data Delay Time (Note 11)	t20	_	65	75	ns
Pulse Timing of $\phi$ and SP	t18	0	250	_	ns
Pulse Timing of SH and SP	t19	20	250	_	ns

(Note 10) TYP. is the case of fRS = 1MHz. (Note 11) Load Resistance is 100k  $\Omega_{\star}$ 

(Note 12) MIN. is Ons, when DOS is not used.

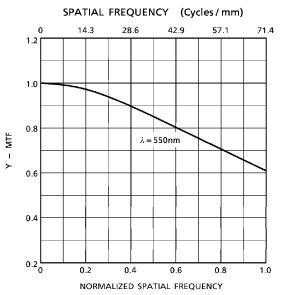
#### **TYPICAL PERFORMANCE CURVES**



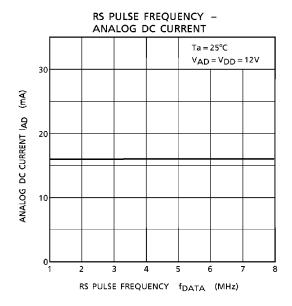
MODULATION TRANSFER FUNCTION OF X-DIRECTION

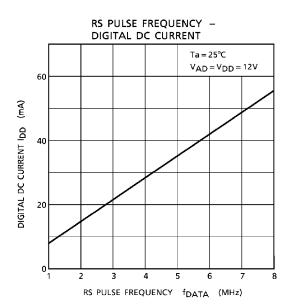
SPATIAL FREQUENCY (Cycles/mm) 14.3 28.6 42.9 57.1 71.4 1.2 1.0 0.8 X - MTF  $\lambda = 550 \text{nm}$ 0.6 0.4 0.2L 0.4 0.6 8.0 1.0 NORMALIZED SPATIAL FREQUENCY

MODULATION TRANSFER FUNCTION OF Y-DIRECTION

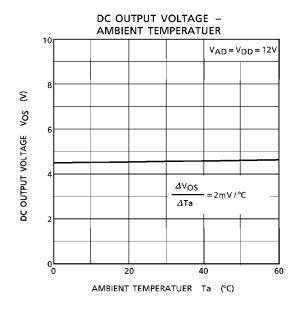


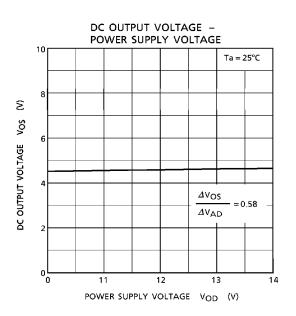
#### TYPICAL PERFORMANCE CURVES (Cont'd)

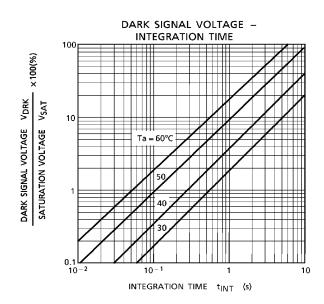




#### TYPICAL PERFORMANCE CURVES (Cont'd)

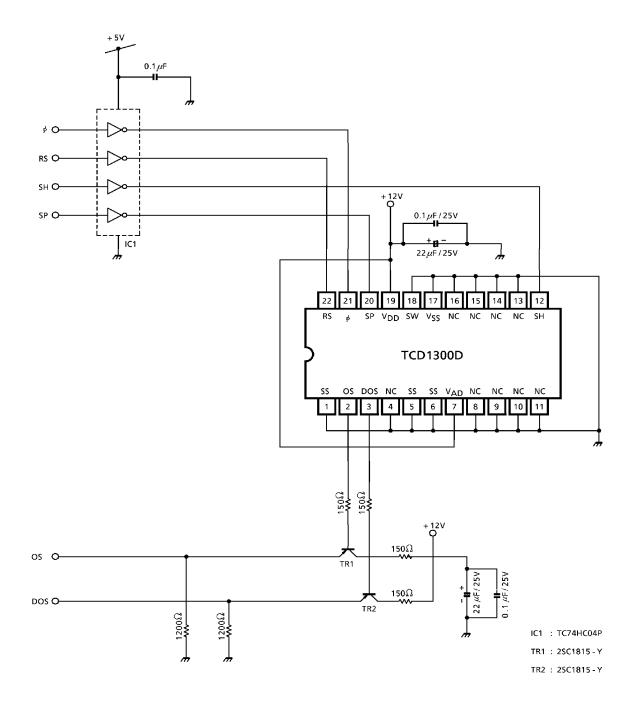






1997-06-30 10/13

#### TYPICAL DRIVE CIRCUIT



1997-06-30 11/13

#### **CAUTION**

#### 1. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N<sub>2</sub>.

Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

#### 2. Electrostatic Breakdown

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

#### 3. Incident Light

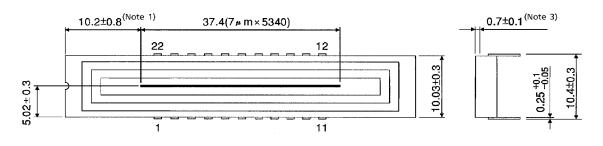
CCD sensor is sensitive to infrared light.

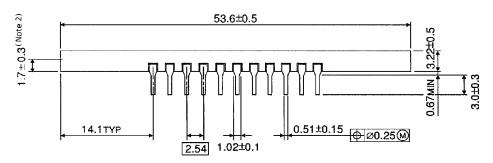
Note that infrared light component degrades resolution and PRNU of CCD sensor.

1997-06-30 12/13

#### **OUTLINE DRAWING**

WDIP22-C-400-2.54B (C) Unit: mm





- (Note 1) No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.
- (Note 2) TOP OF CHIP TO BOTTOM OF PACKAGE.
- (Note 3) GLASS THICKNES (n = 1.5)

Weight: 5.4g (Typ.)