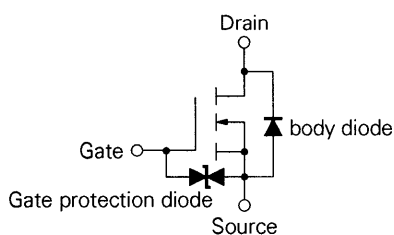
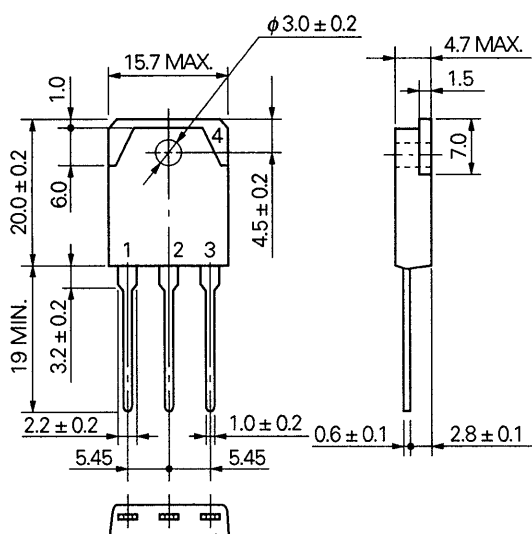


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P1 98.2

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

PACKAGE DIMENSIONS (in millimeters)



1. Gate
2. Drain
3. Source
4. Fin (Drain)

DESCRIPTION

The 2SK1492 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 0.12 \Omega$ MAX. ($V_{GS} = 10 V$, $I_D = 18 A$)
- Low C_{iss} $C_{iss} = 3\ 000$ pF TYP.
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	-55 to +150 °C
Channel Temperature	150 MAX. °C

Maximum Power Dissipation

Total Power Dissipation ($T_a = 25\ ^\circ C$)	140	W
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Maximum Voltages and Currents ($T_a = 25\ ^\circ C$)

V_{DS}	Drain to Source Voltage	250	V
V_{GS}	Gate to Source Voltage	±30	V
$I_{D(DC)}$	Drain Current (DC)	±35	A
$I_{D(pulse)}^*$	Drain Current (pulse)	±140	A

* $PW \leq 10\ \mu s$, Duty Cycle $\leq 1\ \%$

Maximum Avalanche Capability Ratings**

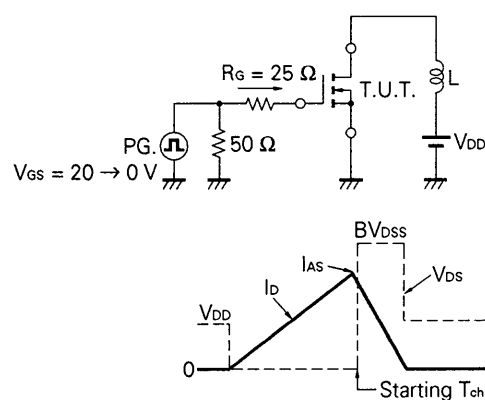
I_{AS}	Single Avalanche Current	52.5	A
E_{AS}	Single Avalanche Energy	2 500	mJ

**Starting $T_{ch} = 25\ ^\circ C$, $R_G = 25\ \Omega$, $V_{GS} = 20 V \rightarrow 0$

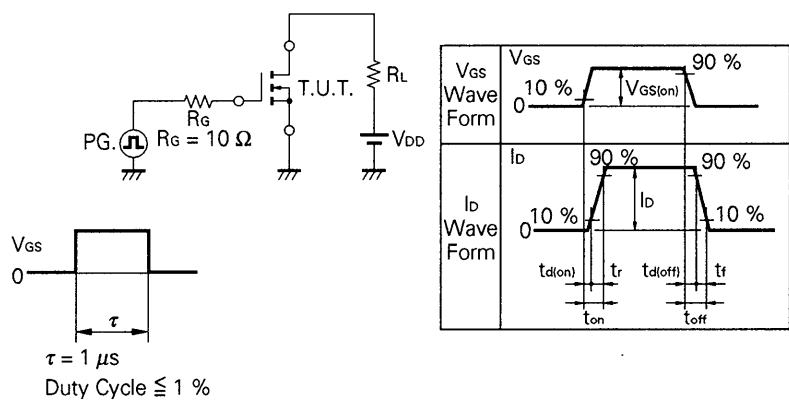
ELECTRICAL CHARACTERISTICS ($T_a = 25\text{ }^{\circ}\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		0.08	0.12	Ω	$V_{GS} = 10\text{ V}$, $I_D = 18\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.5		3.5	V	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	7.0			S	$V_{DS} = 10\text{ V}$, $I_D = 18\text{ A}$
Drain Leakage Current	I_{DSS}			100	μA	$V_{DS} = 250\text{ V}$, $V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 30\text{ V}$, $V_{DS} = 0$
Input Capacitance	C_{iss}		3 000		pF	$V_{DS} = 10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$
Output Capacitance	C_{oss}		1 500		pF	
Reverse Transfer Capacitance	C_{rss}		620		pF	
Turn-On Delay Time	$t_{d(on)}$		50		ns	$V_{GS} = 10\text{ V}$ $V_{DD} = 150\text{ V}$ $I_D = 18\text{ A}$, $R_G = 10\text{ }\Omega$ $R_L = 8.3\text{ }\Omega$
Rise Time	t_r		240		ns	
Turn-Off Delay Time	$t_{d(off)}$		140		ns	
Fall Time	t_f		100		ns	
Total Gate Charge	Q_G		80		nC	$V_{GS} = 10\text{ V}$ $I_D = 35\text{ A}$ $V_{DD} = 200\text{ V}$
Gate to Source Charge	Q_{GS}		17		nC	
Gate to Drain Charge	Q_{GD}		50		nC	
Diode Forward Voltage	$V_{F(S-D)}$		1.0		V	$I_F = 35\text{ A}$, $V_{GS} = 0$
Reverse Recovery Time	t_{rr}		370		ns	$I_F = 35\text{ A}$ $di/dt = 50\text{ A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}		2.8		μC	

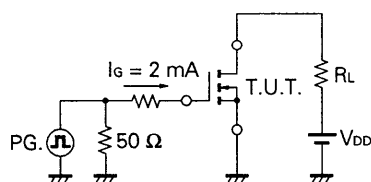
Test Circuit 1: Avalanche Time



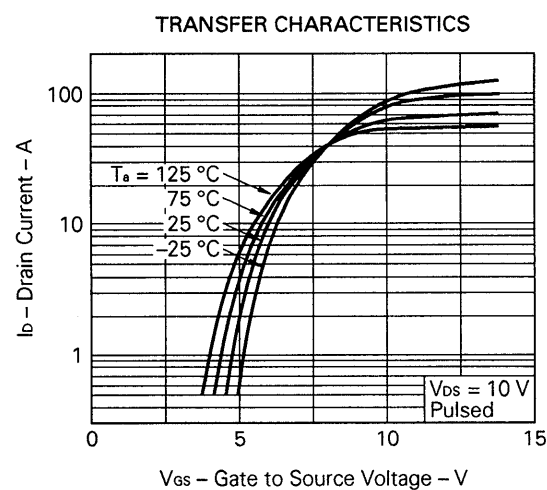
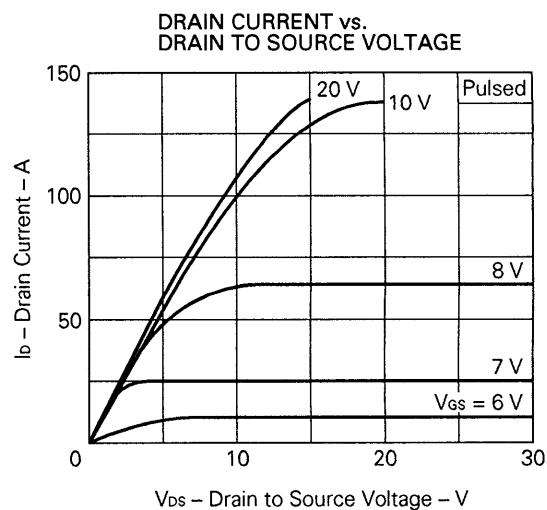
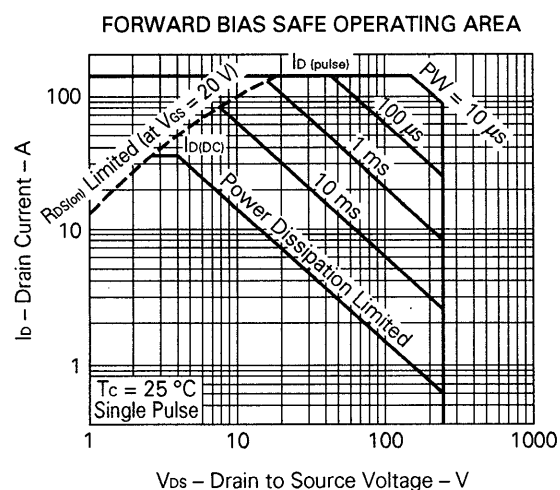
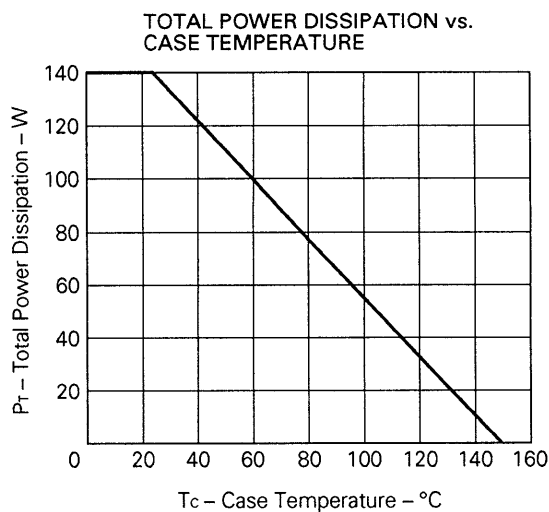
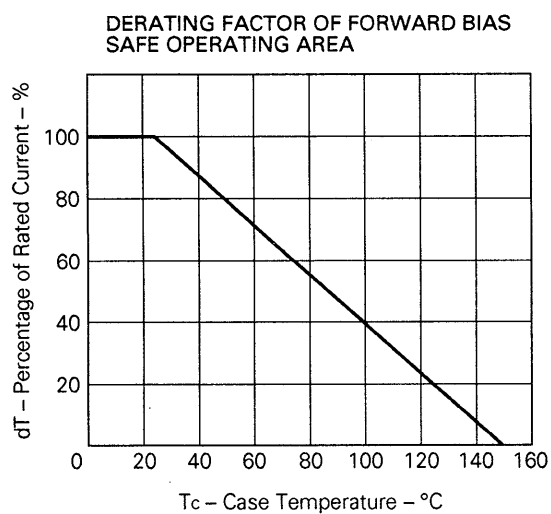
Test Circuit 2: Switching Time



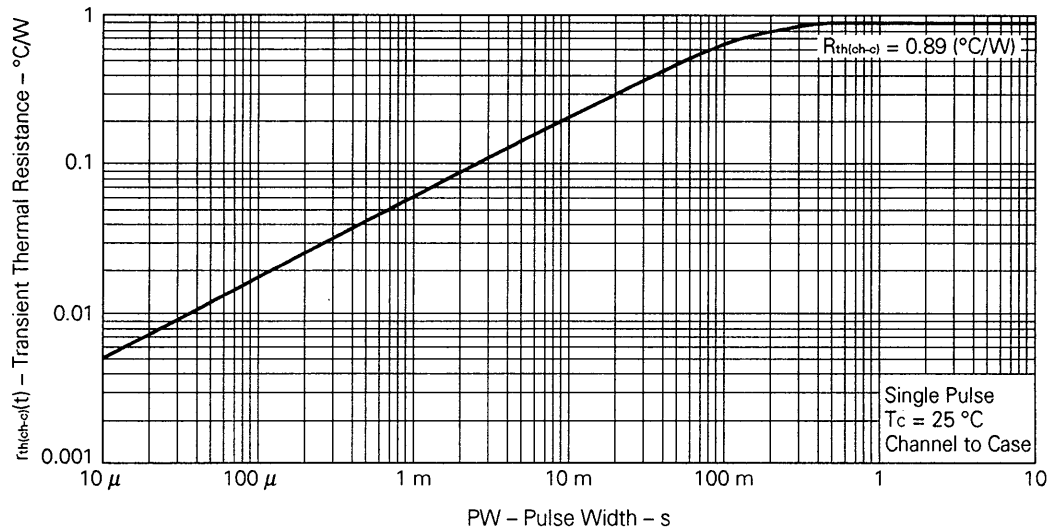
Test Circuit 3: Gate Charge



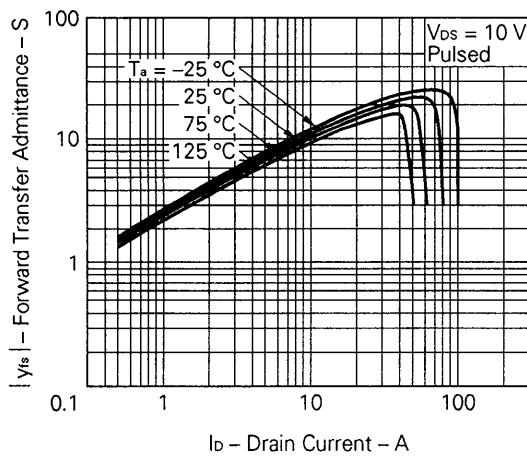
TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)



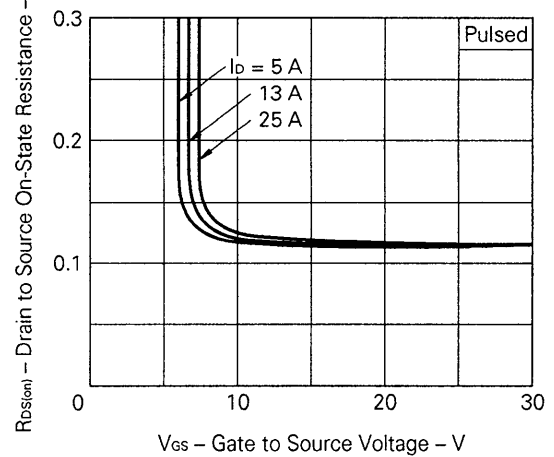
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



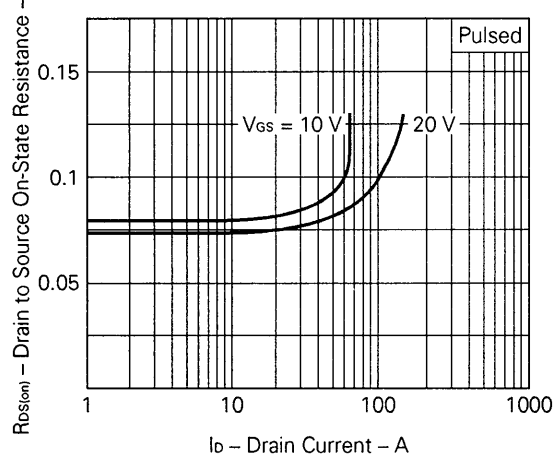
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



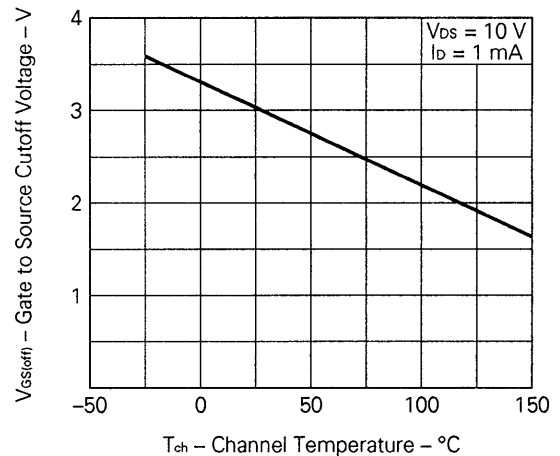
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

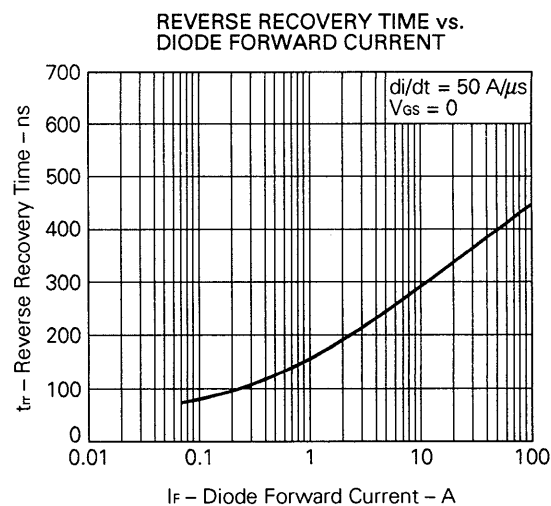
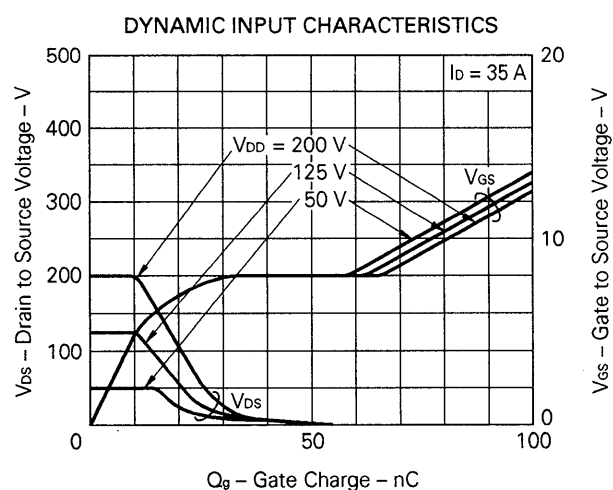
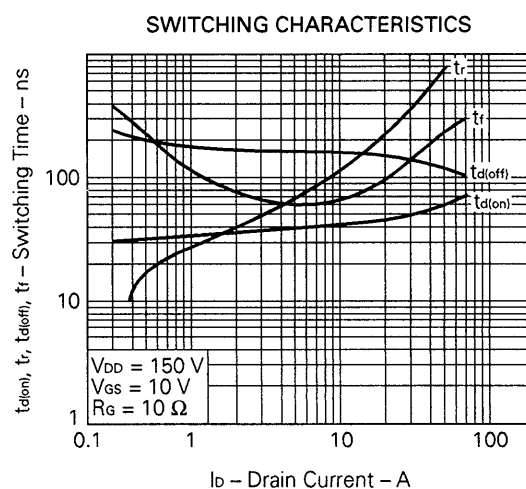
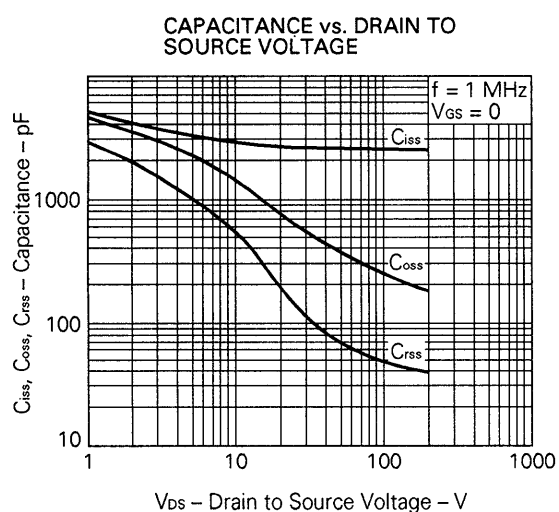
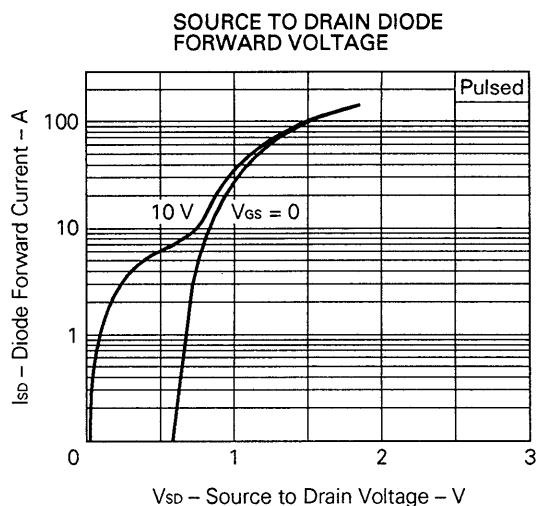
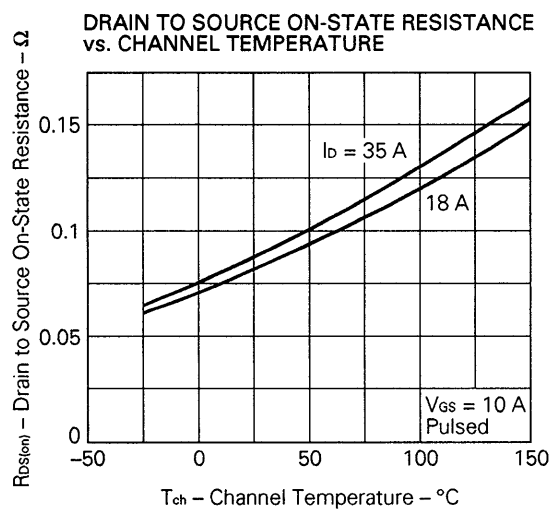


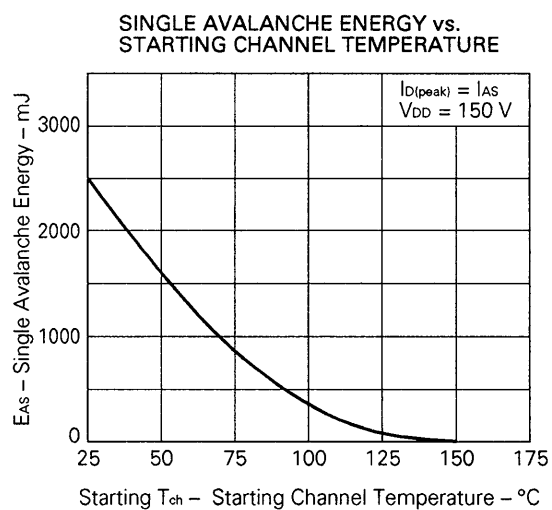
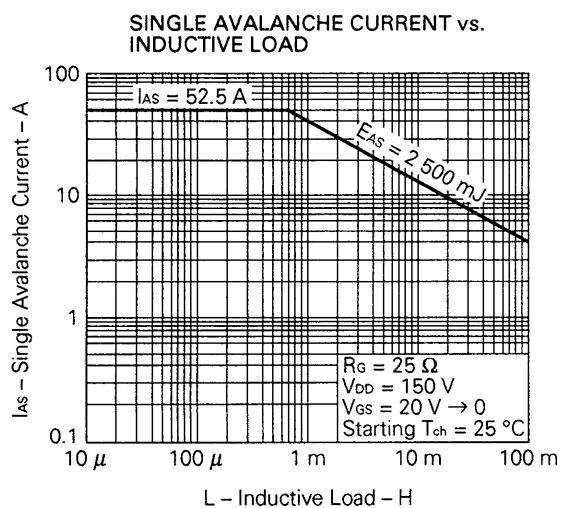
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE







Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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