# STEL-1108
# Data Sheet

# STEL-1108/CR
## 126 MHz BPSK/QPSK
## Digital Modulator

intel

# TABLE OF CONTENTS

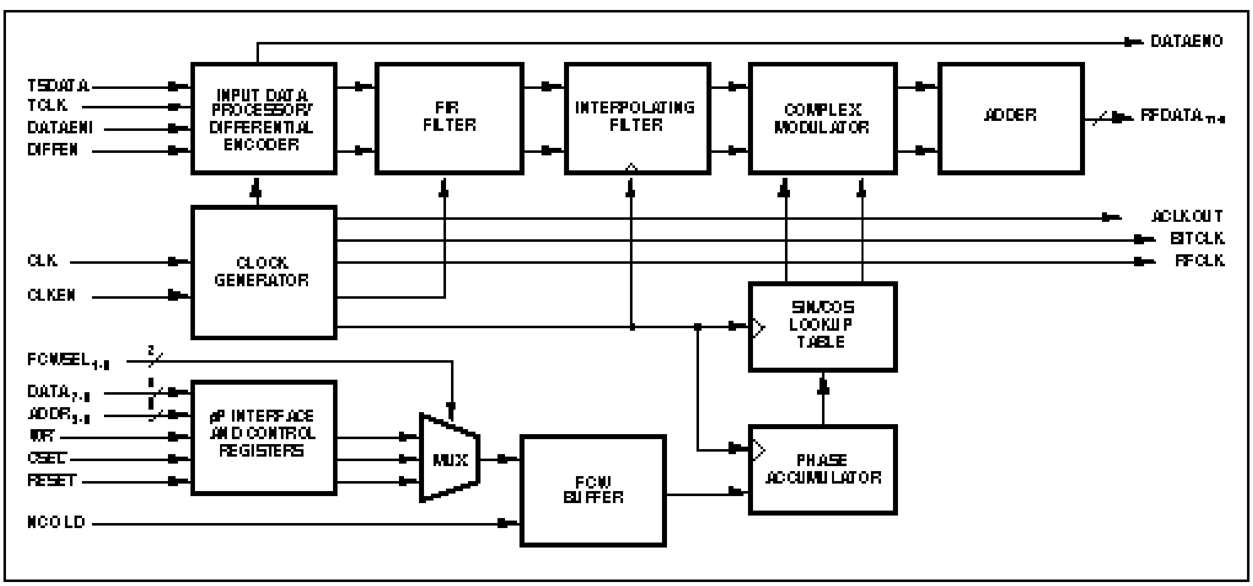
## FEATURES

- Complete BPSK / DBPSK / QPSK / DQPSK modulator in a CMOS ASIC
- Operates at up to 6.3 Mbps in BPSK mode and up to 12.6 Mbps in QPSK mode.
- Programmable over a wide range of data rates
- NCO modulator provides fine frequency resolution
- 126 MHz maximum clock rate generates modulated carrier at frequencies to 50 MHz
- Eliminates most analog circuitry
- Operates in continuous and burst mode
- Selectable 10- or 12-bit outputs
- 32-tap FIR filter for signal shaping before modulation
- 80-Pin MQFP Package

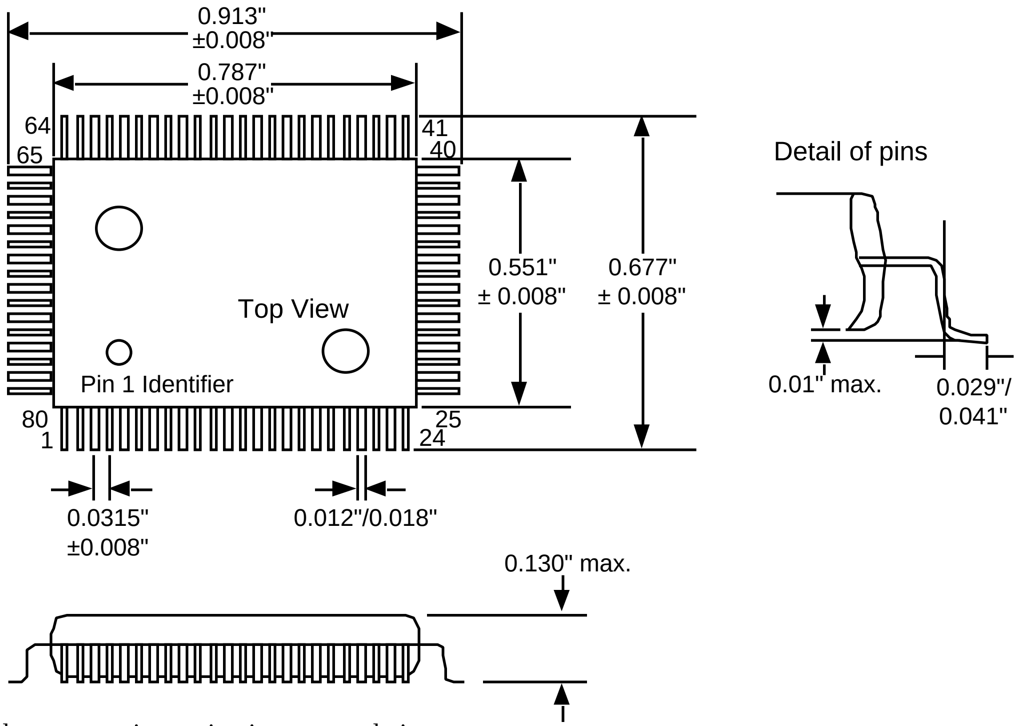
## BENEFITS

- High performance and high reliability with reduced manufacturing costs
- Supports data rates for voice and other applications
- Supports multiple data rate applications
- Rapidly retunable to any frequency in the operating band
- Simplifies upconversion of signal to higher frequencies
- Low cost, small, allows quick prototyping
- Optimizes performance in all modes
- Optimum interfacing to suitable DAC
- Optimum spectral purity of output minimizes external filtering
- Small Footprint, Surface Mount

## BLOCK DIAGRAM



## PACKAGE OUTLINE




Note: Tolerance on pin spacing is not cumulative

WCP 51833.c-8/21/96

Package style: 80-pin MQFP. Thermal coefficient, $\theta$ja = 58° C/W

## PIN CONFIGURATION

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{DD}$ | 17 | TSDATA | 33 | $V_{SS}$ | 49 | $V_{SS}$ | 65 | $\overline{RFCLKD}$ |
| 2 | $DATA_4$ | 18 | DATAENI | 34 | I.C. | 50 | $RFDATA_4$ | 66 | $V_{SS}$ |
| 3 | $DATA_5$ | 19 | TCLK | 35 | I.C. | 51 | $V_{DD}$ | 67 | $\overline{RESET}$ |
| 4 | $DATA_6$ | 20 | $FCWSEL_0$ | 36 | I.C. | 52 | $RFDATA_5$ | 68 | RFCLKD |
| 5 | $DATA_7$ | 21 | $FCWSEL_1$ | 37 | ACLKOUT | 53 | $V_{SS}$ | 69 | $V_{SS}$ |
| 6 | $V_{SS}$ | 22 | I.C. | 38 | $V_{DD}$ | 54 | $RFDATA_6$ | 70 | DIFFEN |
| 7 | $V_{SS}$ | 23 | I.C. | 39 | DATAENO | 55 | $V_{SS}$ | 71 | NCO LD |
| 8 | $ADDR_5$ | 24 | I.C. | 40 | BITCLK | 56 | $RFDATA_7$ | 72 | $\overline{CSEL}$ |
| 9 | $ADDR_4$ | 25 | $V_{DD}$ | 41 | $V_{DD}$ | 57 | $RFDATA_8$ | 73 | $\overline{WR}$ |
| 10 | $ADDR_3$ | 26 | CLKEN | 42 | RFCLK | 58 | $V_{SS}$ | 74 | I.C. |
| 11 | $V_{DD}$ | 27 | $V_{SS}$ | 43 | $V_{SS}$ | 59 | $RFDATA_9$ | 75 | $V_{DD}$ |
| 12 | $ADDR_2$ | 28 | CLK | 44 | $RFDATA_0$ | 60 | $RFDATA_{10}$ | 76 | $DATA_0$ |
| 13 | $ADDR_1$ | 29 | NC | 45 | $RFDATA_1$ | 61 | $V_{SS}$ | 77 | $DATA_1$ |
| 14 | $ADDR_0$ | 30 | $V_{DD}$ | 46 | $V_{SS}$ | 62 | $RFDATA_{11}$ | 78 | $DATA_2$ |
| 15 | $V_{SS}$ | 31 | $5V_{DD}$ | 47 | $RFDATA_2$ | 63 | $V_{DD}$ | 79 | $DATA_3$ |
| 16 | $V_{SS}$ | 32 | N.C. | 48 | $RFDATA_3$ | 64 | $V_{SS}$ | 80 | $V_{SS}$ |

Notes: I.C. denotes Internal Connection. Do not use for vias.

# INTRODUCTION

The STEL-1108 is a BPSK / QPSK modulator in a single ASIC.* It is capable of operating at data rates up to 6.3 Mbps in BPSK mode and 12.6 Mbps in QPSK mode. The STEL-1108 will operate at a clock frequency of up to 126 MHz, allowing it to generate output signals at carrier frequencies up to 50 MHz. The STEL-1108 uses digital FIR filtering to optimally shape the spectrum of the modulating data prior to modulation, thereby optimizing the spectrum of the modulated signal while minimizing the analog filtering required after the modulator. The filters are designed to have a symmetrical (mirror image) polynomial transfer function, thereby making the phase response of the filter linear and eliminating inter symbol interference as a result of group delay distortion. In this way it is possible to change the carrier frequency over a wide range without having to change filters, providing the ability to operate a single system in many channels. Signal level scaling is provided after the FIR filter to allow the maximum dynamic range of the arithmetic to be utilized since the signal levels can be changed over a wide range according to how the device is programmed. To facilitate interfacing the STEL-1108 to a Digital to Analog Converter (DAC) an output clock with programmable delay is provided. In addition, the STEL-1108 is designed to operate from a 3.3 volt power supply; provision is made to allow the device to interface with other logic operating at 5 volts.

See Application Note 125 for example calculations of control register values.

*The STEL-1108 utilizes advanced signal processing techniques which are covered by U.S. Patent Number 5,412,352.

# FUNCTION BLOCKS – DESCRIPTION

## Clock Generator Block

The timing of the STEL-1108 is controlled by the Clock Generator Block. This block generates all the clocks required in the device from the **CLK** input, as well as the output clocks. The divider which determines the bit rate, symbol rate and sampling rate of the FIR filter is programmed by the data "n" written into address $29_H$, with the sampling frequency set to $f_{CLK}/(n+1)$, where n can be from 4 to 255. A second divider is used to generate the auxiliary output clock (ACLKOUT) from the clock input. This divider is controlled by the data, "n", stored in bit 3-0 in address $2A_H$, with the frequency set to $f_{CLK}/(n+1)$, where n can be from 2 to 15. Of all the clock signals generated, only the auxiliary clock continues to run when the clock enable is low. The bit clock output runs at twice the symbol rate, even in BPSK mode.

## Input Data Processor Block

The STEL-1108 is designed to operate as a BPSK, QPSK, DBPSK or DQPSK modulator according to the setting of bit 3 in address $2C_H$ and the **DIFFEN** input. When operating in QPSK mode the input data processor assembles pairs of data bits for each symbol to be modulated. The symbol data can then be differentially encoded in a way which depends on whether the modulation format is to be DBPSK or DQPSK. For DBPSK, the encoding algorithm is straightforward:

output bit(k) = input bit(k)   output bit(k–1),

where   represents the logical EXOR function. For DQPSK, however, the differential encoding algorithm is more complex since there are now sixteen possible new states depending on the four possible previous output states and four possible new input states, as shown in the table below:

| New Input | Previously Encoded $OUT(I, Q)_{k-1}$ | | | |
|---|---|---|---|---|
| $IN(I, Q)_k$ | 0 0 | 0 1 | 1 1 | 1 0 |
| 0 0 | 0 0 | 0 1 | 1 1 | 1 0 |
| 0 1 | 0 1 | 1 1 | 1 0 | 0 0 |
| 1 1 | 1 1 | 1 0 | 0 0 | 0 1 |
| 1 0 | 1 0 | 0 0 | 0 1 | 1 1 |
| | Newly Encoded $OUT(I, Q)_k$ | | | |

## FIR Filter Block

The encoded data is filtered to minimize the sidelobes of its spectrum using a 32-tap, linear phase FIR filter. The 10-bit filter coefficients are completely programmable for any symmetrical (mirror image) polynomial and are stored in the registers at addresses $09_H$ to $28_H$, giving the user full control (apart from the symmetry constraint) of the filter response. The clock (sampling) frequency of the FIR filter is set to be four times the symbol rate. This frequency is determined by the data, "n", written into address $29_H$, with the sampling frequency set to $f_{CLK}/(n+1)$, where n can be from 4 to 255.

## Interpolating Filter Block

The output of the FIR filter is interpolated up to the clock frequency, $f_{CLK}$, in a one, two or three stage interpolating filter. Since the gain of the integrators in the interpolating filter can vary over a wide range, a gain control function is provided at its input to select the significance of the 14-bit outputs of the FIR filter relative to the 24-bit inputs of the interpolating filter. This level shift function is controlled by the data stored in bit 7-4 in address $2A_H$.

## Frequency Control Word Buffer Block

The STEL-1108 incorporates a Numerically Controlled Oscillator (NCO) to synthesize the carrier in the modulator. The frequency of the NCO is programmed by means of the Frequency Control Word (FCW) registers at addresses $00_H$ through $08_H$. The STEL-1108 incorporates provision for three separate FCWs (FCW A, FCW B and FCW C) to be stored in these registers. The modulator frequency can be switched between these values by means of the **FCWSEL$_{1-0}$** inputs. The fourth setting of this 2-bit input selects a zero-frequency value, causing the modulator output to stop instantly at its current phase.

## Phase Accumulator and Sine/Cosine Lookup Table Block

The 24-bit NCO gives a frequency resolution of approximately 6 Hz at a clock frequency of 100 MHz. The 12-bit sine and cosine lookup tables (LUTs) synthesize a carrier with very high spectral purity, typically better than 75 dBc at the digital outputs.

## Complex Modulator Block

The interpolated I and Q data signals are fed into the Complex Modulator Block to be multiplied by the sine and cosine carriers from the Sin / Cos LUT Block.

## Adder Block

The modulated sine and cosine carriers are fed into the Adder Block where they are either added or subtracted together to form the sum:

$$\text{Sum} = \pm I \cdot \cos(\omega t) \pm Q \cdot \sin(\omega t)$$

The signs of the I and Q components can be controlled by the settings of bits 0 and 1 in address $2B_H$, giving complete control over the characteristics of the RF signal generated.

# INPUT SIGNAL DESCRIPTIONS

## $\overline{\text{RESET}}$ (Pin 67)

**Reset.** **$\overline{\text{RESET}}$** is the master reset of the STEL-1108 and clears or presets all registers when it is set low. Setting **$\overline{\text{RESET}}$** high enables operation of the circuitry. After the STEL-1108 is powered up, it is necessary to assert the **$\overline{\text{RESET}}$** pin low for greater than 100 nS prior to configuring the chip.

## CLK (Pin 28)

**Master Clock.** **CLK** is the master clock of all the blocks. Its frequency must be an integer multiple of four times the data rate used (i.e., an integer multiple of the FIR Filter sampling rate) so that the programmable binary divider in the Clock Generator Block can generate the bit clock from the **CLK** signal.

## CLKEN (Pin 26)

**Clock Enable.** **CLKEN** provides a gate to control the master clock. Setting **CLKEN** low will disable all functions in the STEL-1108 (except for the auxiliary clock output) by stopping the clock internally, thereby reducing the power consumption almost to the static level. Setting **CLKEN** high enables normal operation. When bit 7 is set high in address $2C_H$, the STEL-1108 will be configured to operate with an externally provided data clock, **TCLK**. When **CLKEN** is set high **BITCLK** will be resynchronized to the first rising edge of **TCLK** after the rising edge of **CLKEN**.

***CAUTION: CLKEN must be held low continuously while programming addresses $2A_H$ and $2B_H$. Failure to do so will cause the interpolator to lock up, requiring the STEL-1108 to be reset before normal operation resumes.***

## $\overline{\text{WR}}$ (Pin 73)

**Write.** **$\overline{\text{WR}}$** is used to control the writing of data to the **DATA$_{7-0}$** bus. When **$\overline{\text{WR}}$** is set low the register selected by the **ADDR$_{5-0}$** lines will become transparent and the data on the **DATA$_{7-0}$** bus will be latched in when **$\overline{\text{WR}}$** goes high again.

## DATA$_{7-0}$ (Pins 2 - 5, 76 - 79)

**Data Bus.** **DATA$_{7-0}$** is an 8-bit microprocessor interface bus that provides access to all internal mode control register inputs for programming. **DATA$_{7-0}$** is used in conjunction with **$\overline{\text{WR}}$** and **ADDR$_{5-0}$** to write the information into the control and coefficient registers.

## ADDR$_{5-0}$ (Pins 8 - 10, 12 - 14)

**Address Bus.** **ADDR$_{5-0}$** is a 6-bit address bus that selects the mode control register location into which the information provided on the **DATA$_{7-0}$** bus will be written. **ADDR$_{5-0}$** is used in conjunction with **$\overline{\text{WR}}$** and **DATA$_{7-0}$** to write the information into the control and coefficient registers.

## $\overline{\text{CSEL}}$ (Pin 72)

**Chip Select.** **$\overline{\text{CSEL}}$** is provided to enable or disable the microprocessor operation of the STEL-1108. When **$\overline{\text{CSEL}}$** is set high all write operations are disabled. When **$\overline{\text{CSEL}}$** is set low the data bus become active and write operations are enabled.

## NCO LD (Pin 71)

**NCO Load** Input. The frequency control word selected by the **FCWSEL$_{1-0}$** inputs will be loaded into the NCO on the rising edge of **NCO LD**. This function is also executed automatically each time the **DATAENI** input is set high. There is a pipeline delay of 16 **CLK** cycles from the rising edges of both **NCO LD** and **DATAENI** to the point where the NCO outputs are multiplied by the modulating signal in the Modulator Block. There is a further pipeline delay of 11 **CLK** cycles to the output pins, making a total of 27 **CLK** cycles from the load command to the output.

## FCWSEL$_{1-0}$ (Pins 20, 21)

**F**requency **C**ontrol **W**ord **Sel**ect. **FCWSEL$_{1-0}$** is a 2-bit input that permits the selection of one of four frequency control words for the NCO. In this way the NCO can be rapidly switched between these four frequencies without having to reload the FCW data in the FCW registers. The FCW is selected as follows:

| **FCWSEL$_{1-0}$** | FCW data register / addresses |
|---|---|
| 00 | FCW 'A' |
| 01 | FCW 'B' |
| 10 | FCW 'C' |
| 11 | FCW = 0 (zero frequency) |

Whenever **FCWSEL$_{1-0}$** is changed the NCO frequency will change after the NCO is reloaded with a rising edge on either the **NCO LD** or the **DATAENI** inputs.. When **FCWSEL$_{1-0}$** = 11 the FCW data is unconditionally set to $00\ 00\ 00\ 00_H$, setting the NCO to zero frequency. When this occurs the NCO output will remain at its current phase value until **FCWSEL$_{1-0}$** is changed and the NCO is reloaded.

## DATAENI (Pin 18)

**Data Enable Input.** The **DATAENI** input is used to signify the beginning and end of a burst of data. It should be set high before the first (when the STEL-1108 is configured for BPSK modulation by setting bit 3 in address $2C_H$ high) or second (when the STEL-1108 is configured for QPSK modulation by setting bit 3 in address $2C_H$ low) falling edge of **BITCLK** (the edge on which the Q-channel bit is loaded in the QPSK mode) of each burst and set low again after the last falling edge of **BITCLK** of each burst. **DATAENO** will go high after the first two symbol periods of eachburst. At this time the NCO will be reloaded according to the current setting of **FCWSEL$_{1-0}$**.

### DIFFEN (Pin 70)

**Dif**ferential **En**code enable Input. When **DIFFEN** is set low the data will be transmitted without any differential encoding. When this pin is set high the data will be differentially encoded before modulation and transmission as follows:

DBPSK modulation (bit 3 in address $2C_H$ set high):

The data will be differentially encoded starting with the bit entering the **TSDATA** input during the symbol in which **DIFFEN** goes high. This bit will be differentially encoded relative to a logic zero, regardless of the value of the previous bit. The differential encoding algorithms:

output bit(k) = input bit(k)     output bit(k–1)

where     represents the logical XOR function.

DQPSK modulation (bit 3 in address $2C_H$ set low):

The data will be differentially encoded starting with the bit pair entering the **TSDATA** input during the symbol in which **DIFFEN** goes high. The bits in that symbol will be differentially encoded relative to a 00 symbol, regardless of the value of the previous symbol. The differential encoding algorithm is shown in the table below:

| New Input | Previously Encoded $OUT(I, Q)_{k-1}$ | | | |
|---|---|---|---|---|
| $IN(I, Q)_k$ | 0 0 | 0 1 | 1 1 | 1 0 |
| 0 0 | 0 0 | 0 1 | 1 1 | 1 0 |
| 0 1 | 0 1 | 1 1 | 1 0 | 0 0 |
| 1 1 | 1 1 | 1 0 | 0 0 | 0 1 |
| 1 0 | 1 0 | 0 0 | 0 1 | 1 1 |
| | Newly Encoded $OUT(I, Q)_k$ | | | |

### TSDATA (Pin 17)

Transmit Serial Data Input. The data to be transmitted is input at this pin. When bit 7 is set low in address $2C_H$, the data is latched in on the falling edges of the **BITCLK** output. When this bit is set high the data is latched in on the rising edges of the **TCLK** input.

### TCLK (Pin 19)

**T**ransmit **Cl**oc**k** Input. The STEL-1108 is designed to operate either in a slave mode, when an external bit clock is required, or in a master mode, when it provides its own clock, according to the setting of bit 7 in address $2C_H$. Although the **TSDATA** signal is sampled internally on the falling edges of the internally generated **BITCLK** signal, a synchronizing circuit is provided to allow the use of the external data clock, **TCLK**, by setting bit 7 high in address $2C_H$. The **TCLK** input must be set to the correct frequency in relation to the **CLK** input, i.e., its frequency must be the same as the bit rate. In this mode the clock generator will free-run until the first rising edge on **TCLK** and will then synchronize **BITCLK** to this edge to allow **TCLK** to be used as the data input clock. The falling edges of **BITCLK** will occur n+4 cycles of **CLK** after the rising edges of **TCLK**, where n is the value of the data stored in the Sampling Rate Control Register at address $29_H$. The data will then be latched in on the rising edges of **TCLK** before being re-sampled internally with **BITCLK**. In the event that the mutual synchronization of the clocks is lost, the clock generator can be made to resynchronize itself to **TCLK** by setting bit 0 in address $2E_H$ high and then low again. **BITCLK** will be resynchronized to the first rising edge of **TCLK** after bit 0 is set low.

### $5V_{DD}$ (Pin 31)

To allow the STEL-1108 to be operated with drive circuits operating from conventional +5 volt logic levels the input buffers are powered from a separate power supply pin called $5V_{DD}$. This pin should be connected to the supply from which the drive circuits are powered. If the drive circuits operate from the same supply voltage as the STEL-1108 then $5V_{DD}$ and $V_{DD}$ (+3.3 volts) should be connected together.

# OUTPUT SIGNAL DESCRIPTIONS

## $RFDATA_{11\text{-}0}$ (Pins 44, 45, 47, 48, 50, 52, 54, 56, 57, 59, 60, 62)

**RF** Output **Data**. The 12 MSBs of the internal 15-bit sum of the I·cos and Q·sin products are brought out as **$RFDATA_{11\text{-}0}$**. In some applications it may be desirable to use a 10-bit DAC with the STEL-1108. In this case the two MSBs, **$RFDATA_{11\text{-}10}$**, can be disabled by setting bit 3 high in address $2B_H$. The signal should then be scaled after the FIR filter so that the peak amplitude of the output is no more than 10 bits and the DAC connected to pins **$RFDATA_{9\text{-}0}$**.

## DATAENO (Pin 39)

**Data En**able **O**utput. **DATAENO** is a modified replica of the **DATAENI** input. It will be set high two symbols after **DATAENI** goes high and it will be set low eleven symbols after **DATAENI** goes low. In this way, **DATAENO** indicates the entire activity period of the **$RFDATA_{11\text{-}0}$** output during the burst.

## BITCLK (Pin 40)

**Bit Clock Output. BITCLK** is a 50% duty cycle clock at twice the symbol rate, which is determined by the value of the data stored in the Sampling Rate Control Register at address $29_H$. If an external transmit data clock is not available, **BITCLK** can be used as the clock in QPSK mode (divide by 2 externally for BPSK mode). When bit 7 in address $2C_H$ is set high the **TSDATA** signal is first sampled internally on the rising edges of the **TCLK** signal The falling edges of **BITCLK** will then occur n+4 cycles of **CLK** after the rising edges of **TCLK**, where n is the value of the data stored in the Sampling Rate Control Register at address $29_H$. When bit 7 in address $2C_H$ is set low the **TSDATA** signal will be sampled directly on the falling edges of **BITCLK**.

## RFCLK (Pin 42)

The **RFCLK** output is a replica of the input clock signal, **CLK**. It is intended to be used to strobe the DAC connected to the **$RFDATA_{11\text{-}0}$** output. To cater for different DAC characteristics and requirements it is possible to set the actual timing of **RFCLK** by means of bits 6-5 in address $2C_H$, as shown in the following table:

| Bits 6-5 | RFCLK Delay (TYP) |
|---|---|
| 0 0 | 5 nsec |
| 0 1 | 7 nsec |
| 1 0 | 9 nsec |
| 1 1 | Disabled |

Setting 11 disables the **RFCLK** output, making it possible to turn off the DAC output in this way. Please refer to the timing diagrams for further details.

## $\overline{RFCLKD}$, RFCLKD (Pins 65, 68)

The **$\overline{RFCLKD}$ and RFCLKD** outputs are delayed replicas of the output clock signal, **RFCLK**. They are not normally used and are not shown in the block diagram.

## ACLKOUT (Pin 37)

**Auxiliary Clock O**utput. **CLK** is divided by a factor of 3 to 16 to generate the **ACLKOUT** signal. The division factor is determined by the data stored in bits 3-0 of address $2A_H$. The frequency is then set to the frequency of **CLK**/(n+1), where n is the value stored in address $2A_H$ and must range from 2 to 15. In all cases, **ACLKOUT** will be high for two cycles of **CLK** and low for (n–1) cycles of **CLK**.

# MODE CONTROL REGISTERS - WRITE ADDRESSES

## Addresses $00_H$ - $08_H$: NCO Frequency Control Words

The internal Carrier NCO is driven by a frequency control word that is stored in the FCW registers. The nine 8-bit registers at addresses $00_H$ through $08_H$ are used to store the three 24-bit frequency control words FCW 'A', FCW 'B' and FCW 'C' as shown in Table 1. The LSB of each byte is stored in bit 0 of each register.

| Address | FCW Data |
|---|---|
| $00_H$ | FCW 'A', bits 7-0 |
| $01_H$ | FCW 'A', bits 15-8 |
| $02_H$ | FCW 'A', bits 23-16 |
| $03_H$ | FCW 'B', bits 7-0 |
| $04_H$ | FCW 'B', bits 15-8 |
| $05_H$ | FCW 'B', bits 23-16 |
| $06_H$ | FCW 'C', bits 7-0 |
| $07_H$ | FCW 'C', bits 15-8 |
| $08_H$ | FCW 'C', bits 23-16 |

Table 1. Carrier NCO FCW Storage

The frequency of the NCO will be:

$$f_{CARR} = \frac{f_{CLK} \cdot FCW}{2^{24}}$$

where:

$f_{CLK}$ is the frequency of the **CLK** input.

and FCW is the FCW data stored in addresses $00_H$ through $08_H$ as selected by the setting of the **FCWSEL$_{1-0}$** inputs. When **FCWSEL$_{1-0}$** is set to 11 the frequency of the NCO is set to zero.

## Addresses $09_H$ - $28_H$: FIR Filter Coefficients

The coefficients of the FIR filter are stored in addresses $09_H$ - $28_H$, using two addresses for each 10-bit coefficient as shown in Table 2. The LSB of each byte is stored in bit 0 of each register, so that bits 9-8 of each coefficient are stored in bits 1-0 of the corresponding register. The coefficients are stored as Two's Complement numbers in the range –512 to +511 (200H to 1FFH).

| Address | FCW Data |
|---|---|
| $09_H$ | Taps 0 and 31, bits 7-0 |
| $0A_H$ | Taps 0 and 31, bits 9-8 |
| $0B_H$ | Taps 1 and 30, bits 7-0 |
| $0C_H$ | Taps 1 and 30, bits 9-8 |
| … | … |
| … | … |
| $25_H$ | Taps 14 and 17, bits 7-0 |
| $26_H$ | Taps 14 and 17, bits 9-8 |
| $27_H$ | Taps 15 and 16, bits 7-0 |
| $28_H$ | Taps 15 and 16, bits 9-8 |

Table 2. FIR Filter Coefficient Storage

The filter is always constrained to have symmetrical coefficients, resulting in a linear phase response. This allows each coefficient to stored once for two taps, as shown in the table.

## Address $29_H$: Sampling Rate, Symbol Rate and Bit Rate Control

The timing of the STEL-1108 is controlled by the Clock Generator Block. This block generates all the clocks required in the device from the **CLK** input, as well as the output clocks. The divider which determines the bit rate, symbol rate and sampling rate of the FIR filter is programmed by the data written into address $29_H$, with the sampling frequency ranging from $f_{CLK}/5$ to $f_{CLK}/256$. The sampling rate is then set to the frequency of **CLK**/(n+1), where n is the value stored in address $29_H$ and must range from 4 to 255, unless n is a multiple of 16. If n is a multiple of 16 the sampling rate will be set to the frequency of **CLK**/(n+17) In all cases this is further divided by 2 to generate **BITCLK**. Note that at **CLK** frequencies below approximately 64 MHz it is also permissible to set the sampling rate to 3, giving a sampling frequency of $f_{CLK}/4$.

## Address $2A_H$:

***CAUTION: CLKEN must be held low continuously while programming address $2A_H$. Failure to do so will cause the interpolator to lock up, requiring the STEL-1108 to be reset before normal operation resumes.***

### Bits 0 through 3 -- Auxiliary Clock Rate Control

The timing of the **ACLKOUT** signal is controlled by the Clock Generator Block. The divider which determines the frequency of **ACLKOUT** is programmed by the data written into bits 3-0 in address $2A_H$, with the frequency ranging from $f_{CLK}/3$ to $f_{CLK}/16$. The frequency is then set to the frequency of **CLK**/(n+1), where n is the value stored in address $2A_H$ and the valid range is 2 to 15. If n is set to 1 the **ACLKOUT** output will remain set high, thereby disabling this function. If the **ACLKOUT** signal is not required, it is recommended that it be set in this mode to conserve power consumption.

### Bits 4 through 7 -- Interpolation Filter Input Gain Control

Since the gain of the integrators in the interpolation filter can vary over a wide range, a gain control function is provided at its input to select the significance of the 14-bit outputs of the FIR filter relative to the 24-bit inputs of the interpolation filter. This function is controlled by the data stored in bit 7-4 in address $2A_H$, as shown in Table 3:

| Bits 7-4 | Input signal level of Interpolation Filter |
|---|---|
| $0_H$ | Bits 13-0 Lowest Gain |
| $1_H$ | Bits 14-1 |
| ..... | .... |
| ..... | .... |
| $7_H$ | Bits 20-7 |
| $8_H$ | Bits 21-8 Highest Gain |

Table 3. Interpolation Filter Signal Level Control

### Address $2B_H$:

***CAUTION: CLKEN must be held low continuously while programming address $2B_H$. Failure to do so will cause the interpolator to lock up, requiring the STEL-1108 to be reset before normal operation resumes.***

### Bits 1 - 0 -- Invert I/Q Channels

The I channel signal is multiplied by the cosine output from the NCO and the Q channel Signal is multiplied by the sine output prior to being added together. Bits 0 and 1 in address $2B_H$ allow the two products to be inverted prior to the addition, as shown in Table 4:

| Bits 1-0 | Output of Adder Block |
|---|---|
| 0 0 | Sum = $I \cdot \cos(\omega t) + Q \cdot \sin(\omega t)$ |
| 0 1 | Sum = $-I \cdot \cos(\omega t) + Q \cdot \sin(\omega t)$ |
| 1 0 | Sum = $I \cdot \cos(\omega t) - Q \cdot \sin(\omega t)$ |
| 1 1 | Sum = $-I \cdot \cos(\omega t) - Q \cdot \sin(\omega t)$ |

Table 4. Signal Inversion Control

This capability gives complete flexibility to the control of the output signal.

### Bit 2 -- Test Mode

Bit 2 in address $2B_H$ sets the STEL-1108 into a test mode and should always be set low during normal operation.

### Bit 3 -- Disable Output MSBs

The STEL-1108 generates a 12-bit output signal $OUT_{11-0}$ and is designed to be used with a 12-bit DAC. In some applications it may be desirable to use a 10-bit DAC; in this case the output signal level should be set so that the 2 MSBs of the output, $OUT_{11-10}$, are unused. These two bits can then be disabled to reduce power consumption by setting bit 3 high in address $2B_H$. Care should be taken when this feature is used since no overflow protection is provided.

### Bits 5 - 4 -- Interpolation Filter Bypass Control

Bits 4 and 5 in address $2B_H$ determine the number of stages of interpolation used in the Interpolation Filter Block. Three cascaded sections of interpolation are provided and up to two of these can be bypassed according to the settings of bits 4 and 5, as shown in Table 5:

| Bits 5-4 | Number of Interpolations selected |
|---|---|
| 0 0 | 3 |
| 0 1 | 2 |
| 1 0 | 2 |
| 1 1 | 1 |

Table 5. Interpolation Filter Bypass Control

### Bits 7 - 6 -- Test Mode

Bits 6 and 7 in address $2B_H$ set the STEL-1108 into a test mode and should always be set low.

## Address $2C_H$:

### Bit 0 -- Test Mode

Bit 0 in address $2C_H$ sets the STEL-1108 into a test mode and should always be set low during normal operation.

### Bit 1 -- FIR Filter Bypass Control

The FIR filters in the STEL-1108 can be bypassed by setting bit 1 high in address $2C_H$.

### Bit 2 -- Test Mode

Bit 2 in address $2C_H$ sets the STEL-1108 into a test mode and should always be set low during normal operation.

### Bit 3 -- BPSK Select

The STEL-1108 is capable of operating as either a BPSK or a QPSK modulator according to the setting of bit 0 in address $2C_H$. Setting this bit low puts the device into the QPSK mode, generating the output signal:

$$RFOUT = \pm I \cdot \cos(\omega t) \pm Q \cdot \sin(\omega t)$$

Setting this bit high puts the device into the BPSK mode, generating the output signal:

$$RFOUT = \pm I \cdot \cos(\omega t)$$

In this case many of the circuits in the Q channel signal path are disabled to conserve power.

### Bit 4 -- Test Mode

Bit 4 in address $2C_H$ sets the STEL-1108 into a test mode and should normally be set low. Setting this bit high complements the frequency control word.

### Bits 6 - 5 -- RFCLK Delay Control

Bits 5 and 6 in address $2C_H$ control the delay or phase of the RFCLK output, as shown in Table 6:

| Bits 6-5 | RFCLK Delay (TYP) |
|---|---|
| 0 0 | 5 nsec |
| 0 1 | 7 nsec |
| 1 0 | 9 nsec |
| 1 1 | Disabled |

Table 6. RFCLK Delay Control

### Bit 7 -- External Transmit Clock Select

The STEL-1108 is designed to operate either in a slave mode, when an external bit clock is required, or in a master mode, when it provides its own clock, according to the setting of bit 7 in address $2C_H$. Although the **TSDATA** signal is sampled internally on the falling edges of the internally generated **BITCLK** signal, a synchronizing circuit is provided to allow the use of the external data clock, **TCLK**, by setting bit 7 high in address $2C_H$. The **TCLK** input must be set to the correct frequency in relation to the **CLK** input, i.e., its frequency must be the same as the bit rate. In this mode the clock generator will free-run until the first rising edge on **TCLK** and will then synchronize **BITCLK** to this edge to allow **TCLK** to be used as the data input clock. The data will then be latched in on the rising edges of **TCLK** before being re-sampled internally with **BITCLK**. In the event that the mutual synchronization of the clocks is lost, the clock generator can be made to resynchronize itself to **TCLK** by setting bit 0 in address $2E_H$ high and then low again. **BITCLK** will be resynchronized to the first rising edge of **TCLK** after bit 0 is set low. When bit 7 is set low in address $2C_H$ the **TSDATA** signal will be sampled directly by the falling edges of **BITCLK**.

## Address $2D_H$:

### Bit 0 -- PN Data Mode

The STEL-1108 incorporates a pseudo random number (PN) generator, primarily for test purposes. When bit 0 is set high in address $2D_H$ the PN generator will be connected to the data path in place of the normal input data at the **TSDATA** input. When this bit is set low the device will operate in the normal mode, transmitting the input data.

### Bit 1 -- PN Code Select

When bit 0 is set high in address $2D_H$ the STEL-1108 PN generator will be connected to the data path in place of the normal input data at the **TSDATA** input. Two different PN codes can be selected, according the setting of bit 1 in address $2D_H$. When this bit is set low the code will be (10,3) and when it is set high the code will be (23,18). The latter code is the same as that used in a TTC FIREBERD 6000 BER test set, allowing the system to be tested without a second FIREBERD at the transmit site when the transmitter and receiver are located at different sites.

### Bit 2 -- Offset Binary Select

The output signal **$RFOUT_{11-0}$** can be in either two's complement or offset binary format , according to the setting of bit 2 in address $2D_H$. Setting this bit high selects two's complement and setting it low selects offset binary, as shown in Table 7:

| Signal level | **$RFOUT_{11-0}$** Bit 2 = 1 (2's Comp) | Bit 2 = 0 (O. Bin) |
|---|---|---|
| Max. + | $7FF_H$ (12-bit mode) | $FFF_H$ |
| Zero | $000_H$ | $800_H$ |
| Max. – | $800_H$ (12-bit mode) | $000_H$ |

Table 7. **$RFOUT_{11-0}$** Signal Formats

### Bits 7 - 3 -- Not Used

### Address $2E_H$

### Bit 0 -- Bit Clock Sync Control

When bit 7 is set high in address $2C_H$, the STEL-1108 will be configured to operate with an externally provided data clock, **TCLK**. The internally generated **BITCLK** will be synchronized to the first rising edge of this clock. In the event that the mutual synchronization of the clocks is lost, the clock generator can be made to resynchronize itself to **TCLK** by setting bit 0 in address $2E_H$ high and then low again. **BITCLK** will be resynchronized to the first rising edge of **TCLK** after bit 0 is set low.

## DECIMAL, HEX AND BINARY ADDRESS EQUIVALENTS

| Dec. | Hex. | Binary | Dec. | Hex. | Binary | Dec. | Hex. | Binary |
|---|---|---|---|---|---|---|---|---|
| 0 | $00_H$ | 000000 | 16 | $10_H$ | 010000 | 32 | $20_H$ | 100000 |
| 1 | $01_H$ | 000001 | 17 | $11_H$ | 010001 | 33 | $21_H$ | 100001 |
| 2 | $02_H$ | 000010 | 18 | $12_H$ | 010010 | 34 | $22_H$ | 100010 |
| 3 | $03_H$ | 000011 | 19 | $13_H$ | 010011 | 35 | $23_H$ | 100011 |
| 4 | $04_H$ | 000100 | 20 | $14_H$ | 010100 | 36 | $24_H$ | 100100 |
| 5 | $05_H$ | 000101 | 21 | $15_H$ | 010101 | 37 | $25_H$ | 100101 |
| 6 | $06_H$ | 000110 | 22 | $16_H$ | 010110 | 38 | $26_H$ | 100110 |
| 7 | $07_H$ | 000111 | 23 | $17_H$ | 010111 | 39 | $27_H$ | 100111 |
| 8 | $08_H$ | 001000 | 24 | $18_H$ | 011000 | 40 | $28_H$ | 101000 |
| 9 | $09_H$ | 001001 | 25 | $19_H$ | 011001 | 41 | $29_H$ | 101001 |
| 10 | $0A_H$ | 001010 | 26 | $1A_H$ | 011010 | 42 | $2A_H$ | 101010 |
| 11 | $0B_H$ | 001011 | 27 | $1B_H$ | 011011 | 43 | $2B_H$ | 101011 |
| 12 | $0C_H$ | 001100 | 28 | $1C_H$ | 011100 | 44 | $2C_H$ | 101100 |
| 13 | $0D_H$ | 001101 | 29 | $1D_H$ | 011101 | 45 | $2D_H$ | 101101 |
| 14 | $0E_H$ | 001110 | 30 | $1E_H$ | 011110 | 46 | $2E_H$ | 101110 |
| 15 | $0F_H$ | 001111 | 31 | $1F_H$ | 011111 | | | |

## REGISTER SUMMARY - WRITE ADDRESSES

| Address | Contents | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| $00\text{-}02_H$ | NCO Frequency Control Word ‘A’ (24 bits) | | | | | | | |
| $03\text{-}05_H$ | NCO Frequency Control Word ‘B’ (24 bits) | | | | | | | |
| $06\text{-}08_H$ | NCO Frequency Control Word ‘C’ (24 bits) | | | | | | | |
| $09\text{-}28_H$ | FIR Filter Coefficients | | | | | | | |
| $29_H$ | Sampling Rate, Symbol Rate and Bit Rate Control | | | | | | | |
| $2A_H$ | Interpolation Filter Input Gain Control | | | | Auxiliary Clock Rate Control | | | |
| $2B_H$ | Set to zero | | Int. Filt. Bypass Control | | Dis. MSBs | Set to zero | Invert I/Q Channels | |
| $2C_H$ | Ext. Tx Clock Sel. | **RFCLK** Control | | Set to zero | BPSK Select | Set to zero | FIR Bypass Control | Set to zero |
| $2D_H$ | | | | | | Offset Bin. Select | PN Code Select | PN Data Mode |
| $2E_H$ | | | | | | | | Bit Clock Sync Cont. |

**EXAMPLE SOFTWARE INITIALIZATION SEQUENCE**

1. **Disable the clock by setting pin 26 (CLKEN) low**
2. **Reset the STEL-1108 by pulsing pin 67 (RESETB) low (this clears all internal registers)**
3. **Write to all 47 registers**
4. **Enable the clock by setting pin 26 (CLKEN) high**
5. **Force the internal NCO to load the new frequency register data by pulsing pin 71 (NCO LD) high**

# ELECTRICAL CHARACTERISTICS

## ABSOLUTE MAXIMUM RATINGS

***Warning**: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to $V_{SS}$.*

| Symbol | Parameter | Range | Units |
|---|---|---|---|
| $T_{stg}$ | Storage Temperature | –40 to +125 | °C |
| $V_{DDmax}$ | Supply voltage on $V_{DD}$ | –0.3 to + 7 | volts |
| $V_{I(max)}$ | Input voltage | –0.3 to 5$V_{DD}$+0.3 | volts |
| $I_i$ | DC input current | ± 30 | mA |
| $P_{Diss\ (max)}$ | Power dissipation, CLKEN = 1 | 690 | mW |
| $P_{Diss\ (max)}$ | Power dissipation, CLKEN = 0 | 50 | mW |

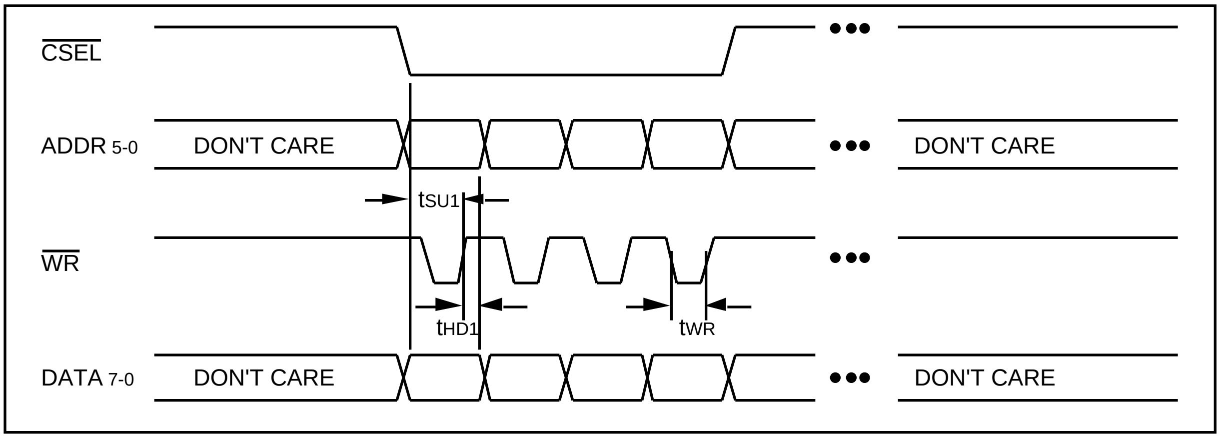
## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Range | Units |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage | +3.3 ± 10% | volts |
| $T_a$ | Operating Temperature (Ambient) | –40 to +85 | °C |

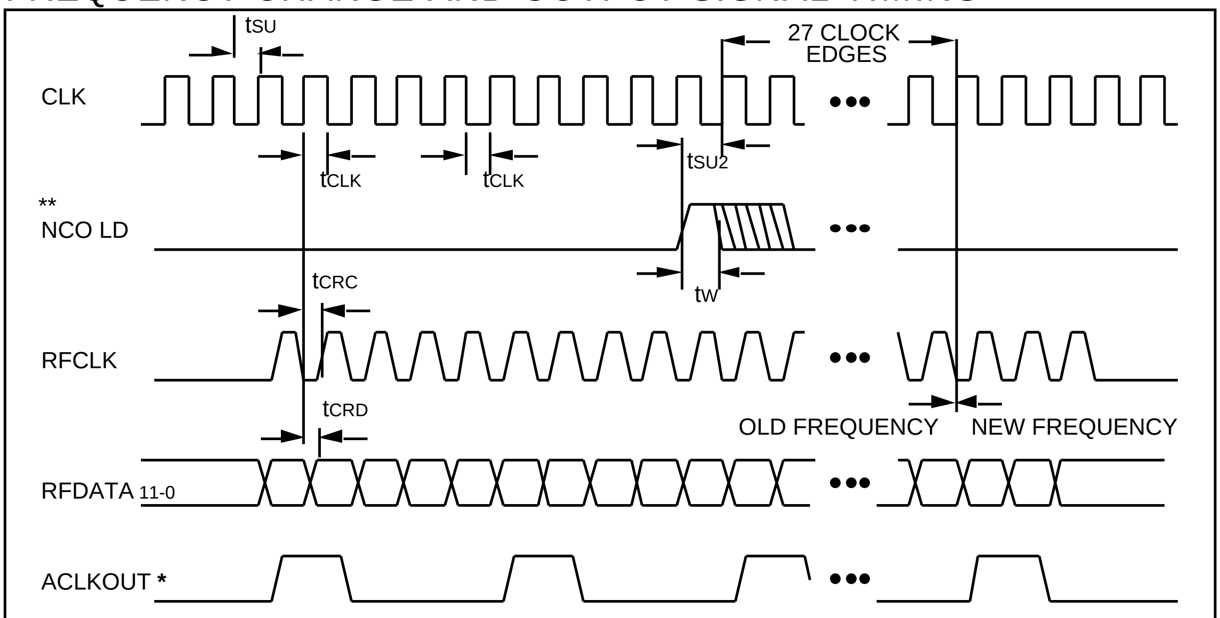
## D.C. CHARACTERISTICS Operating Conditions: $V_{DD}$ = 3.3 V ±10%, $V_{SS}$ = 0 V, $T_a$ = –40° to 85° C

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_{DDQ}$ | Supply Current, Quiescent | | | 1.0 | mA | Static, no clock |
| $I_{DD}$ | Supply Current, Operational | | 2.2 | | mA / MHz | $f_{CLK}$ = 126 MHz |
| $V_{IH(min)}$ | Clock High Level Input Voltage | 2.0 | | | volts | **CLK**, Logic '1' |
| $V_{IL(max)}$ | Clock Low Level Input Voltage | | | 0.8 | volts | **CLK**, Logic '0' |
| $V_{IH(min)}$ | High Level Input Voltage | 2.0 | | | volts | Other inputs, Logic '1' |
| $V_{IL(max)}$ | Low Level Input Voltage | | | 0.8 | volts | Other inputs, Logic '0' |
| $I_{IH}$ | High Level Input Current | | | 10 | µA | $V_{IN}$ = 5$V_{DD}$ |
| $I_{IL}$ | Low Level Input Current | | | –10 | µA | $V_{IN}$ = $V_{SS}$ |
| $V_{OH(min)}$ | High Level Output Voltage | 2.4 | 3.0 | $V_{DD}$ | volts | $I_O$ = –4.0 mA, RFDATA, RFCLK |
| $V_{OL(max)}$ | Low Level Output Voltage | | 0.2 | 0.4 | volts | $I_O$ = + 4.0 mA, RFDATA, RFCLK |
| $V_{OH(min)}$ | High Level Output Voltage | 2.4 | 3.0 | $V_{DD}$ | volts | $I_O$ = –2.0 mA, All other outputs |
| $V_{OL(max)}$ | Low Level Output Voltage | | 0.2 | 0.4 | volts | $I_O$ = +2.0 mA, All other outputs |
| $I_{OS}$ | Output Short Circuit Current | 20 | 65 | 130 | mA | $V_{OUT}$ = $V_{DD}$, $V_{DD}$ = max |
| $C_{IN}$ | Input Capacitance | | 2 | | pF | All inputs |
| $C_{OUT}$ | Output Capacitance | | 4 | 10 | pF | All outputs |

## REGISTER WRITE TIMING



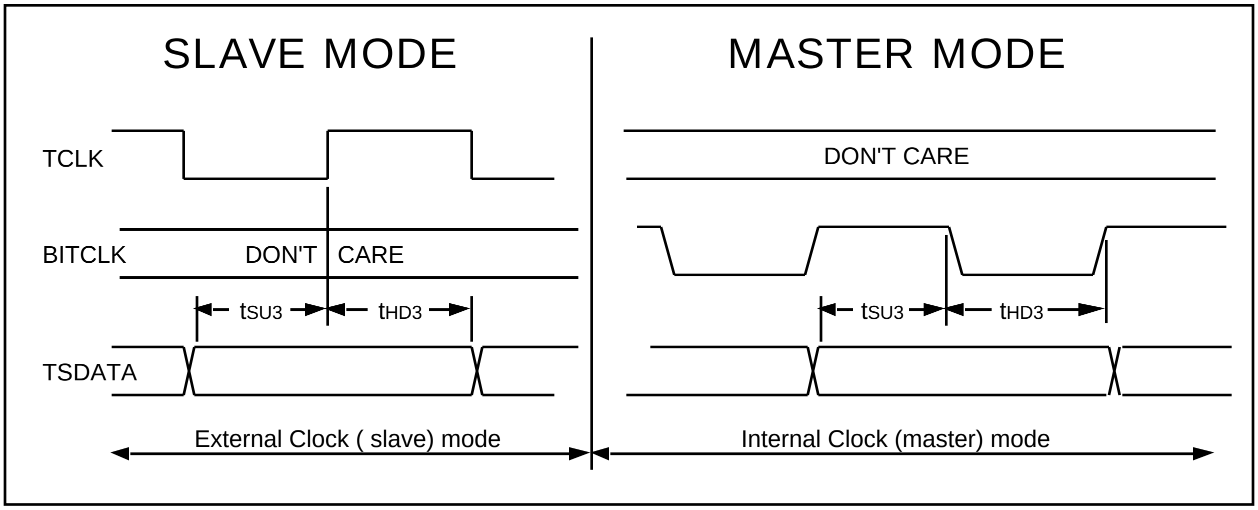

## FREQUENCY CHANGE AND OUTPUT SIGNAL TIMING

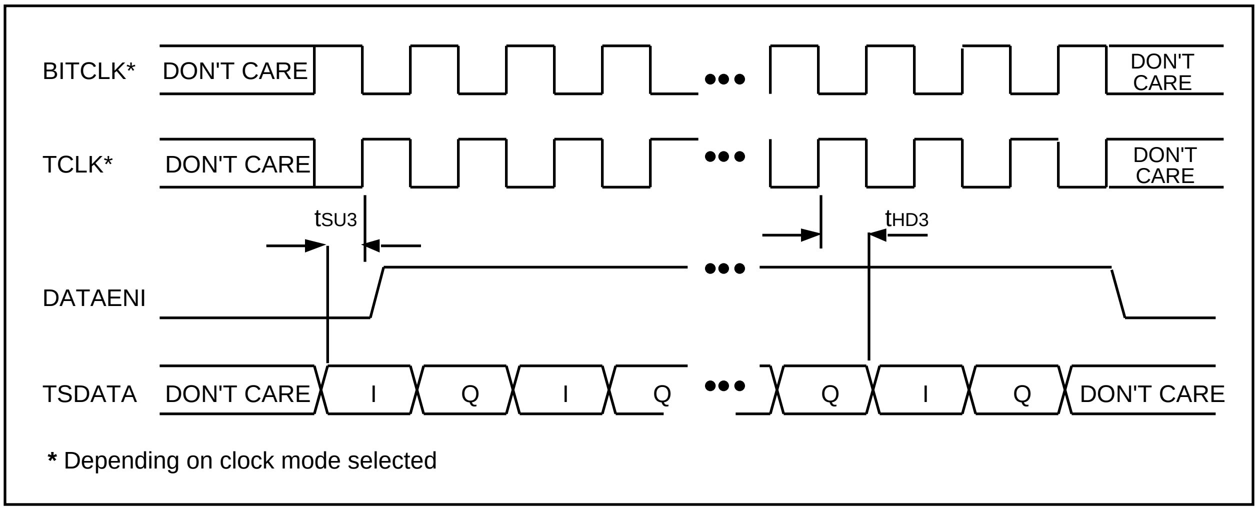



* Shown for ÷5 case (n = 4)
**Insert NCOLD when CLKEN is "HIGH."

TCP 52113.c 9/6/96

## INPUT DATA AND CLOCK TIMING




TCP 52111.c 11/25/96

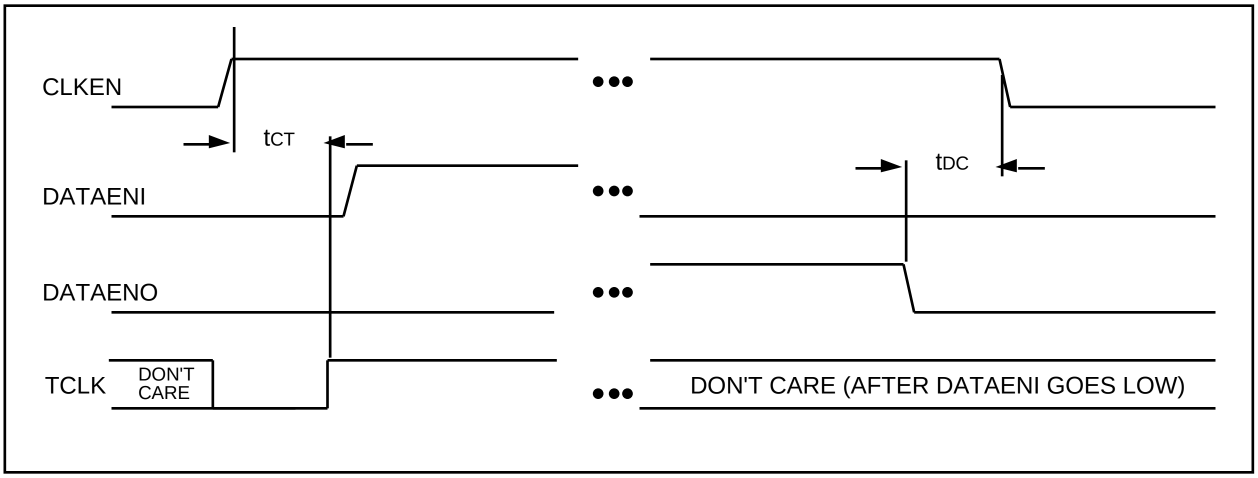
A.C. CHARACTERISTICS

Operating Conditions: $V_{DD}$ = 3.3 V ±10%, $V_{SS}$ = 0 V, $T_a$ = –40° to 85° C,

| Symbol | Parameter | Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| $f_{CLK}$ | **CLK** Frequency | | 126 | MHz | See Note |
| $t_{CLK}$ | **CLK** Pulse width, High or Low | 2 | | nsec. | |
| $t_{WR}$ | $\overline{\textbf{WR}}$ Pulse width | 10 | | nsec. | |
| $t_{SU1}$ | **DATA**$_{7-0}$, **ADDR**$_{5-0}$, $\overline{\textbf{CSEL}}$ to $\overline{\textbf{WR}}$ setup | 5 | | nsec. | |
| $t_{HD1}$ | **DATA**$_{7-0}$, **ADDR**$_{5-0}$, $\overline{\textbf{CSEL}}$ to $\overline{\textbf{WR}}$ hold | 5 | | nsec. | |
| $t_W$ | **NCO LD** Pulse width | 10 | | nsec. | |
| $t_{CRC}$ | **CLK** to **RFCLK** delay, bits 6-5 in Address $2C_H$ | 5* | 9* | nsec. | Load = 10 pF |
| $t_{CRD}$ | **CLK** to **RFDATA**$_{11-0}$ delay | | 12 | nsec. | Load = 10 pF |
| $t_{SU3}$ | **TSDATA** to **TCLK** or **BITCLK** setup | 2.5 | | nsec. | |
| $t_{HD3}$ | **TSDATA** to **TCLK** or **BITCLK** hold | 2.5 | | nsec. | |

***These are the minimum and maximum nominal values programmable.**

## INPUT DATA AND CLOCK TIMING



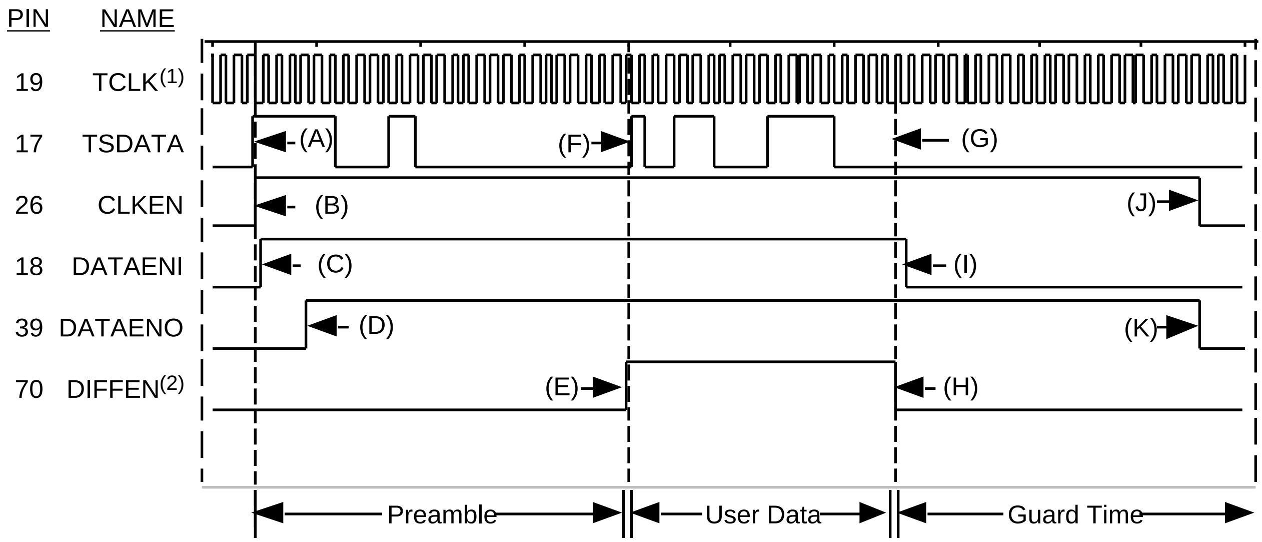

TCP 52112.c 11/25/96

## A.C. CHARACTERISTICS

Operating Conditions: $V_{DD}$ = 3.3 V ±10%, $V_{SS}$ = 0 V, $T_a$ = –40° to 85° C,

| Symbol | Parameter | Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| $t_{CT}$ | **CLKEN** to **TCLK** setup | 2 | | cycles | of **CLK** |
| $t_{DC}$ | **DATAENO** to **CLKEN** hold | 0 | | cycles | of **CLK** |

## BURST TIMING (Slave Mode): FULL VIEW




TCP 52032.c 8/22/96

NOTES:

(1) All input signals shown are derived from TCLK. Each edge is delayed from a TCLK edge by typically 6 to 18 nsec. DATAENO does not depend on TCLK but its edges are synchronized to TCLK. TCLK itself can be turned off after DATAENI goes low.

(2) If the preamble is not encoded the same as the user data, the DIFFEN control can be toggled in mid transmission as shown. Otherwise, the DIFFEN control can be held high or low depending on encoding desired.

(A) First data bit transition on falling edge of TCLK (first of 14 preamble symbols). The data will be valid on the next rising edge of TCLK.

(B) CLKEN rises on the same edge of TCLK that the data starts on. CLKEN is allowed to rise any time earlier than shown.

(C) DATAENI rises on the first rising edge of TCLK (middle of the first preamble bit).

(D) DATAENO rises on the falling edge of TCLK (at the end of the second symbol).

(E) DIFFEN rises on the rising edge of TCLK immediately preceding the first user data bit.

(F) User data bits are clocked by the falling edge of TCLK and must be valid during the next rising edge of TCLK.

(G) End of user data. Note that the data is allowed to go away immediately after it is latched in by the rising of TCLK which occurs in the middle of the last user data bit.

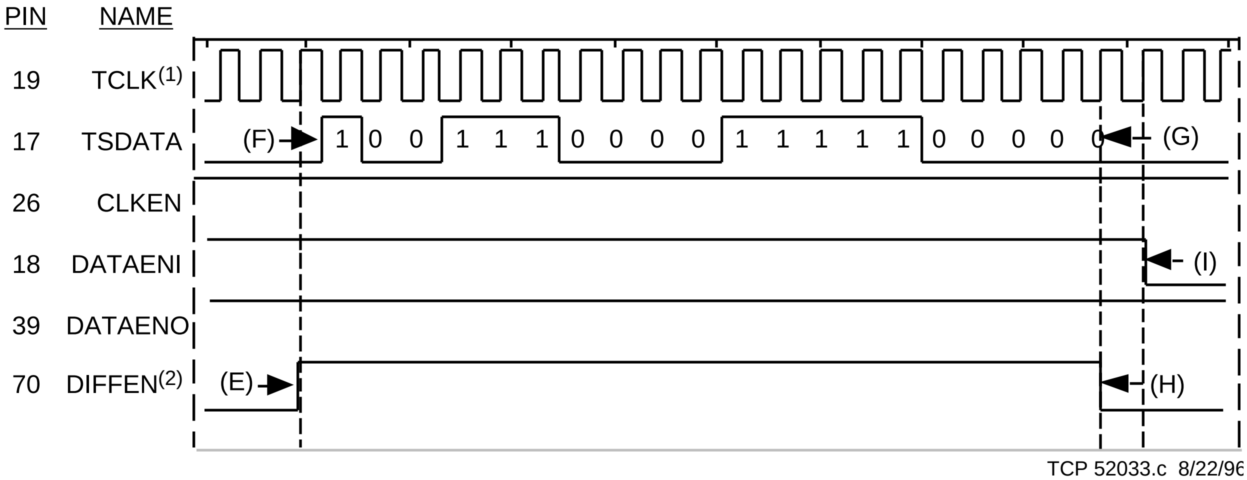
H) DIFFEN goes low on rising edge of TCLK (middle of last user data bit).

(I) DATAENI goes low on rising edge of TCLK (on the cycle of TCLK *after* the last user data bit).

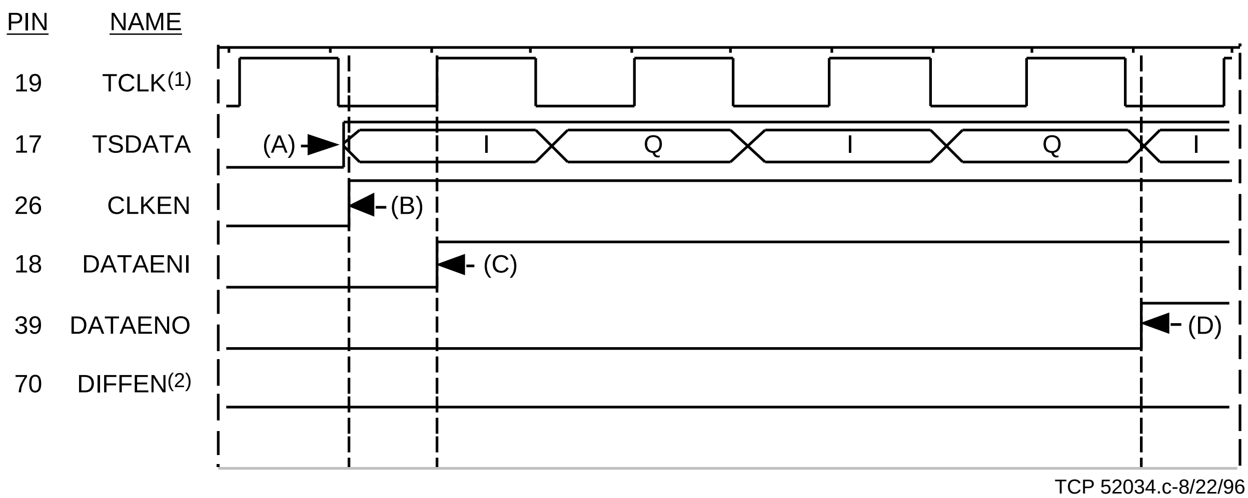
(J) CLKEN must stay high until any time on or after the point where DATAENO goes low.

(K) DATAENO stays high for a period of time about 11 symbols long after DATAENI goes low.

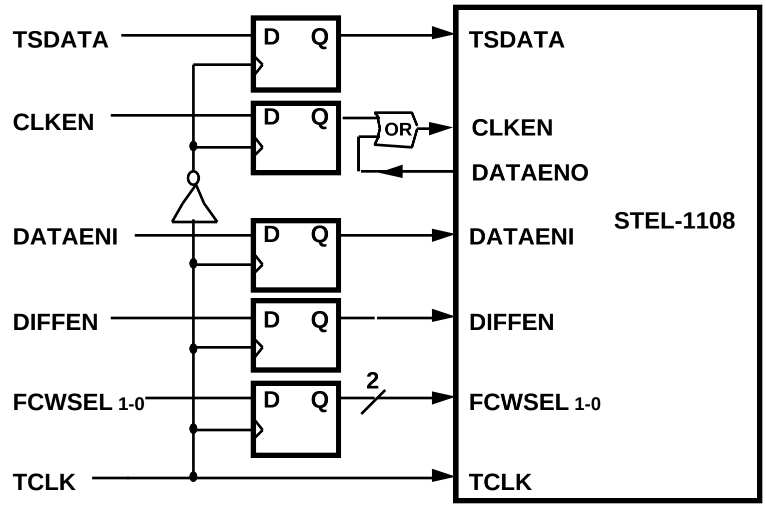
## BURST MODE TIMING: USER BURST DATA INPUT DETAIL




## BURST MODE TIMING: PREAMBLE START DETAIL

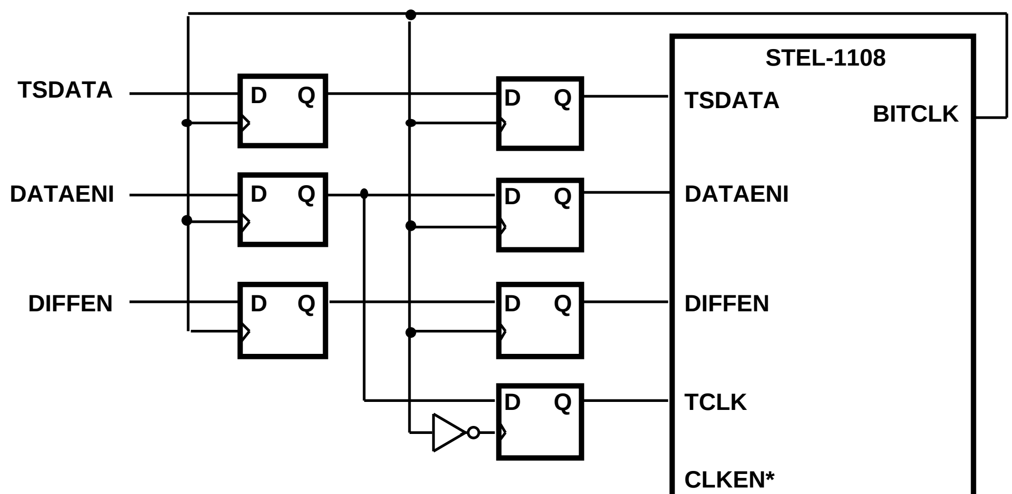


## RECOMMENDED INTERFACE CIRCUIT (Slave Mode)




TCP 52118.c 8/16/96

## RECOMMENDED INTERFACE CIRCUIT (Master Mode)




*CLKEN may be turned off between bursts to conserve power as long as it is turned on at least three cycles of BITCLK before TSDATA arrives and kept on until after DATAENO goes low. Note that the BITCLK output goes inactive whenever CLKEN is low.

TCP 52115.c 9/6/96

## SYNCHRONIZING THE 1108 BIT CLOCK (Master Mode)

1) With TCLK Low

2) Preset the bit clock sync circuit by either

   A) cycling clock enable from low to high
   B) cycling software bit 0 in address $2E_H$ from zero to one and back to zero

3) Bit clock will be in sync after first rising edge of TCLK

4) To keep I/Q bits synchronized with symbol boundaries, either have an integer number of symbols (i.e. an even # of bit clocks) between bursts, or resynchronize at the beginning of each burst.

*For Further Information Call or Write*

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