MicroStar BGA™ Packaging Reference Guide

Literature Number: SSYZ015A
Second Edition – September 1999

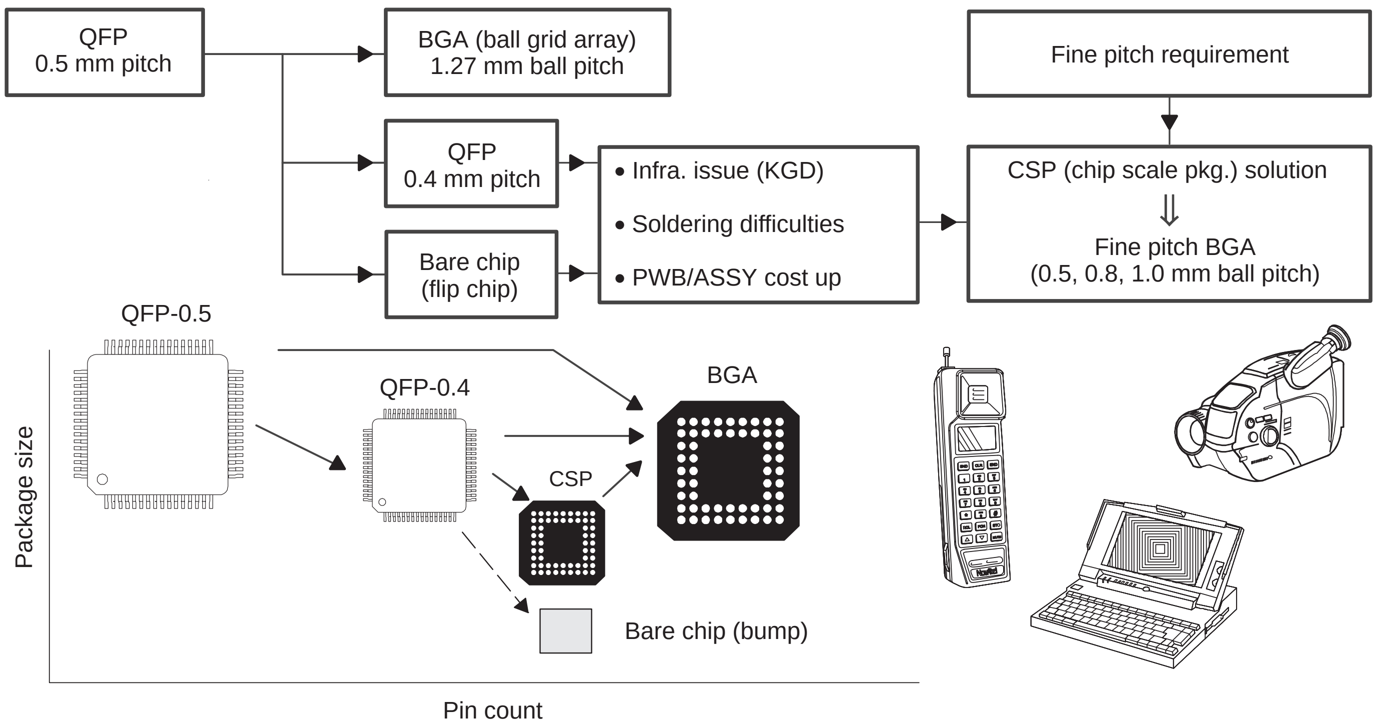
Texas Instruments

Introduction

The parallel pursuit of cost reduction and miniaturization in recent years has given rise to an increasing emphasis on very small integrated circuit (IC) package solutions. This is particularly evident in consumer-based end equipment using digital signal processor (DSP) solutions such as wireless telephones, laptop computers, and hard-disk drives. Despite the formal definition, packages with an area similar in size to the IC they encapsulate are loosely referred to as chip scale packages (CSPs). Figure 1 illustrates this trend.

Figure 1. Packaging Trends

Package trend (customer requirement)

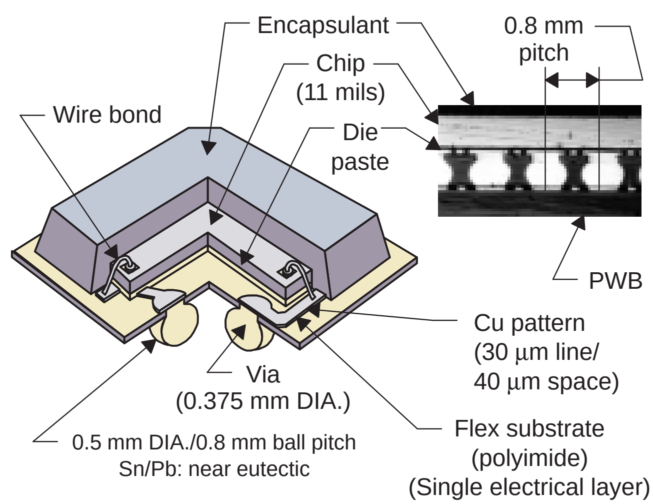


Chip scale packages are in many ways an ideal solution to the cost reduction and miniaturization requirements. They offer enormous area reductions in comparison to quad flat packages (QFPs) and have increasing potential to do so without adding to system-level cost. In the best case, CSPs compete today on a cost-per-terminal basis with QFPs. For example, various CSPs from Texas Instruments (TI™) are now available at cost parity with thin QFPs.

Texas Instruments produces a polyimide film-based family of CSPs called MicroStar BGA™. Like most other CSPs, MicroStar BGAs use solder alloy balls as the interconnect between the package substrate and the board on which the package is soldered. The MicroStar BGA family comes in a range of solder ball pitch (0.5 mm, 0.8 mm, and 1.0 mm). Currently, TI's most popular packages are 64- and 144-ball packages. Figure 2 shows the structure of TI's MicroStar BGA package.

Figure 2. Structure of TI's MicroStar BGA

Conforms to JEDEC Outlines: MO-192 and MO-205-A



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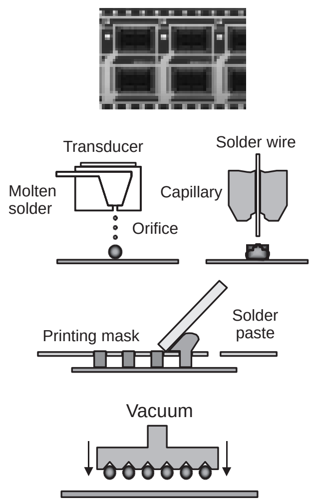
Texas Instruments addressed several key issues in package assembly in order to produce a CSP that is not only physically and mechanically stable but cost-effective for a wide variety of applications. Figure 3 demonstrates how MicroStar BGAs resolve reliability and cost issues. An overall view of the flow used to produce TI MicroStar BGA packages is shown in Figure 4. The process for solder ball attachment is shown in Figure 5.

Figure 3. MicroStar BGA Package Assembly Issues

Substrate selection	– Ceramic – Glass-epoxy – Polyimide†
Interconnection	– Bump (flip chip) – Wire bond†
Solder ball form	– Solder jet – Stud bump – Paste print – Pick and place†
Encapsulation	– Potting – Transfer mold†



†These are the processes used by TI.

Figure 4. MicroStar BGA Package Assembly Flow

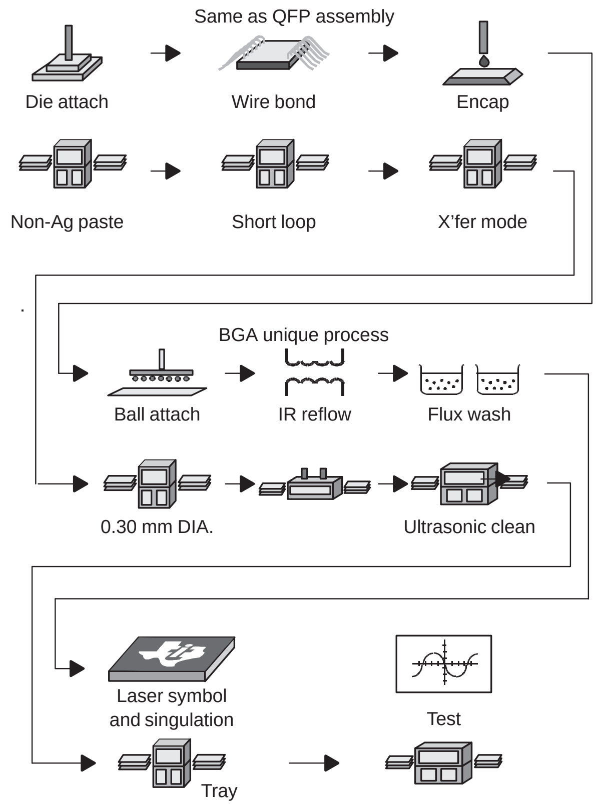
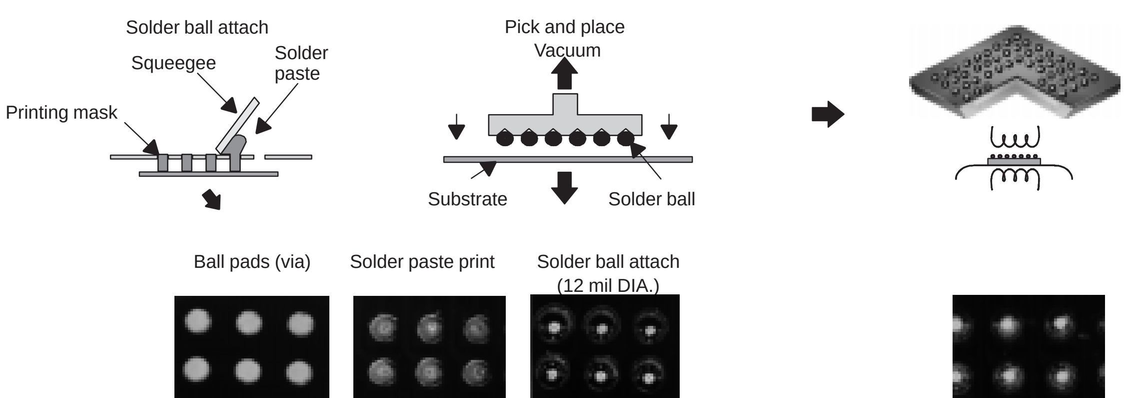
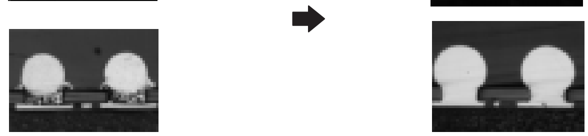


Figure 5. Solder Ball Attachment



Solder ball shear tests

SS	Fail	Ave. Reading
125	0	668 g
125	0	734 g



144GGU, 0.8-mm pitch, 0.5 mm DIA. ball TI spec. is 400 g min

Texas Instruments has qualified many product lines using the MicroStar BGA packages, and has now shipped more than 70 million production units. This guide is designed to give you technical background on MicroStar BGA packages as well as how they can be used to build advanced board layouts.

If you would like more information on using reliable and cost-effective MicroStar BGA packaging in your design, please contact your local TI field sales office.

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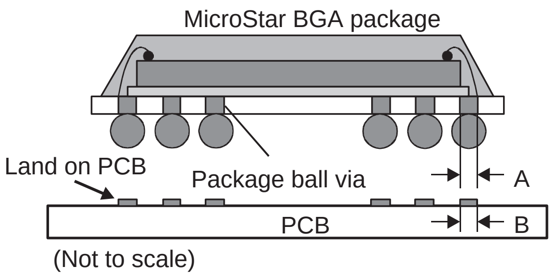
PCB Design Considerations

Solder Land Areas

Design of both the MicroStar BGA itself and the printed circuit board (PCB) are important in achieving good manufacturability and optimum reliability. In particular, the diameters of the package vias and the board lands are critical. While the actual sizes of these dimensions are important, their ratio is more critical. Figure 6 illustrates the package via-to-PCB configuration and Figure 7 illustrates why this ratio is critical.

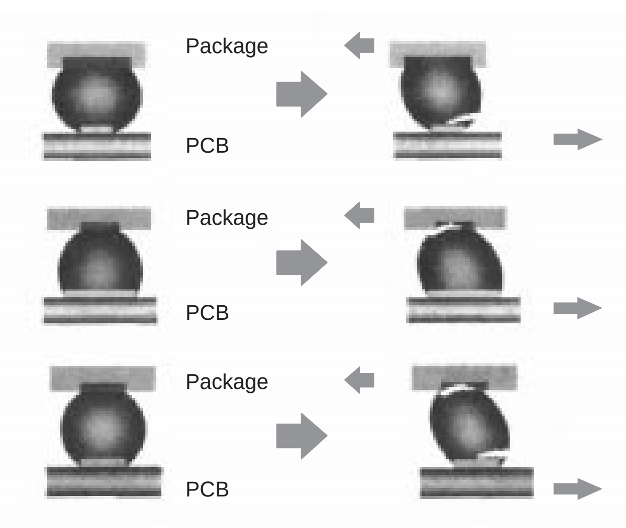
Figure 6. Package Via to Board Land Area Configuration



A = Via diameter on package
B = Land diameter on PCB

Ratio A/B should equal 1.0 for optimum reliability.

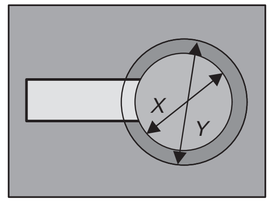
Figure 7. Effects of Via-to-Land Ratios



In the top view of Figure 7, the package via is larger than the PCB via, and the solder ball is prone to crack prematurely at the PCB interface. In the middle view, the PCB via is larger than the package via, which leads to cracks at the package surface. In the bottom view, where the ratio is almost 1:1, the stresses are equalized and neither site is more susceptible to cracking than the other.

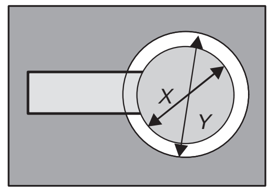
Solder lands on the PCB are generally simple round pads. Solder lands are either solder-mask-defined or non-solder-mask-defined.

Figure 8. Optimum Land Configurations



Solder-mask-defined Land

Ball Pitch	X DIA.	Y DIA.
0.5 mm	(In development)	
0.8 mm	0.38 mm	0.48 mm
1.00 mm	0.45 mm	0.55 mm



Non-solder-mask-defined Land

Ball Pitch	X DIA.	Y DIA.
0.5 mm	(In development)	
0.8 mm	0.35 mm	0.50 mm
1.0 mm	0.4 mm	0.55 mm

Solder-mask-defined (SMD) land. With this method, the copper pad is made larger than the desired land area, and the opening size is defined by the opening in the solder mask material. The advantages normally associated with this technique include more closely controlled size and better copper adhesion to the laminate. Better size control is the result of photoimaging the stencils for masks. The chief disadvantage of this method is that the larger copper spot can make routing more difficult.

Non-solder-mask-defined (NSMD) land. Here, the land area is etched inside the solder mask area. While the size control is dependent on copper etching and is not as accurate as the solder mask method, the overall pattern registration is dependent on the copper artwork, which is quite accurate. The tradeoff is between accurate dot placement and accurate dot size.

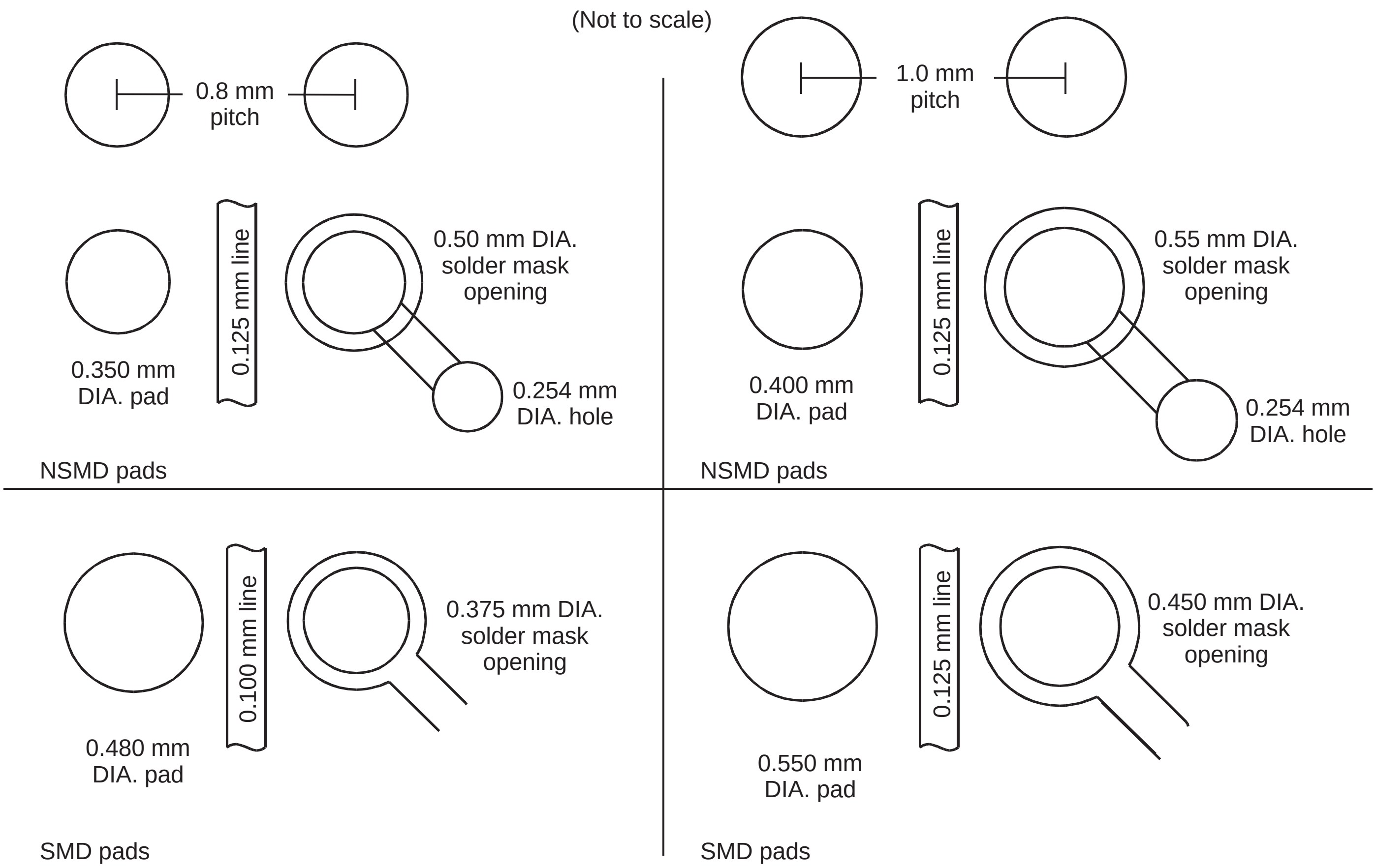
See Figure 8 for an example of optimum land diameters and configurations for a common MicroStar BGA pitch.

Conductor Width/Spacing

Many of today’s circuit board layouts are based on at most a 100-µm conductor line width and 200-µm spacing. To route between 0.8-mm-pitch balls, given a clearance of roughly 380 µm between ball lands, only one signal can be routed between ball pads. The 380-µm ball spacing is worst case and is calculated by assuming the diameter of the solder ball land is 410 µm.

Figure 9 presents some design considerations based on commonly used PCB design rules. Conventionally, the pads are connected by wide copper traces to other devices or to plated through holes (PTH). As a rule, the mounting pads must be isolated from the PTH. Placing the PTH interstitially to the land pads often achieves this.

Figure 9. PCB Design Considerations (Conventional)



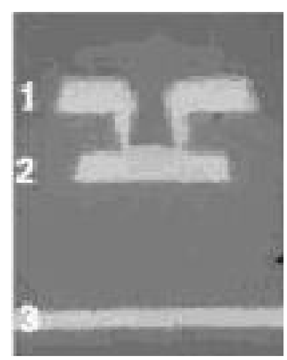
High-Density Routing Techniques

A challenge when designing with CSP packages is that as available space contracts, the space available for signal fanout also decreases. By using a few high-density routing techniques, the PCB designer can minimize many of these design and manufacturing challenges. This section focuses on TI designators GGU (144-pin) and GGW (176-pin) packages. Both packages have 0.8-mm pitch, but each is distinctly different in array style. The GGW ball array has wide channels in the four corners, providing the inner balls with space for routing and V_{CC} connectivity. Mechanical drawings of these MicroStar BGA packages can be found in Appendix B. The GGU package has a solid four-row array configuration which can cause difficulties when routing inner rows on two-layer boards.

Via Density

Via density, as mentioned earlier, can be a limiting factor when designing high-density boards. Via density is defined as the number of vias in a particular board area. Using smaller vias increases the routability of the board by requiring less board space and increasing via density. The invention of the microvia, shown in Figure 10, has solved many of the problems associated with via density.

Figure 10. Microvia Structure



Microvias are often created using a laser to penetrate the first few layers of dielectric. The laser can penetrate a 4-mil-thick dielectric layer, creating the 4-µm microvia shown in Figure 10. The layout designer can now route to the first internal board layer. Two layers (each 4 mils thick) can be laser-drilled, creating a 200-µm microvia diameter. In this case, routing to the first two internal layers is possible.

The number of board layers increases as board chip density and functional pin count increase. As an example, the TMS320VC549GGU digital signal processor (DSP) is in a 144-GGU package and uses 32 balls for power and ground. Routing of roughly

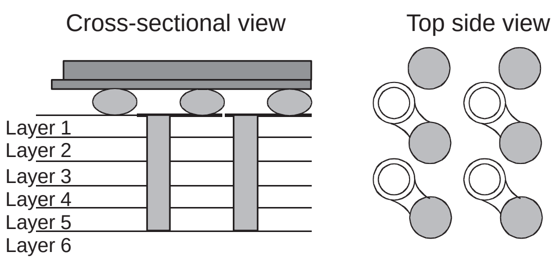
112 signals can be accomplished on three layers. The power and ground planes increase the board to five layers. The sixth layer can be used on the bottom side to place discrete components. Furthermore, by increasing the board layer stack-up to eight layers, high-density applications are possible with only 10 to 15 mils between the chips.

Conventional PCB Design

The relatively large via density on the package periphery, mentioned earlier, is caused by limited options when routing the signal from the ball. To reduce or eliminate the via density problem on the periphery of the package, designers can build the PCB vertically from the BGA pad through the internal layers of the board, as shown in Figure 11. By working vertically and mechanical drilling 250-µm vias between the pads on the board and the internal layers, designers can create a "pick-and-choose" method. They can pick the layer and choose the route. A "dog bone" method is used to connect the through-hole via and the pad.

This method requires a very small mechanical drill to create the necessary number of 144 or 176 vias for one package. Although this method is the least expensive, a disadvantage is that the vias go through the board, creating a matrix of vias on the bottom side of the board.

Figure 11. "Dog Bone Via" Structure



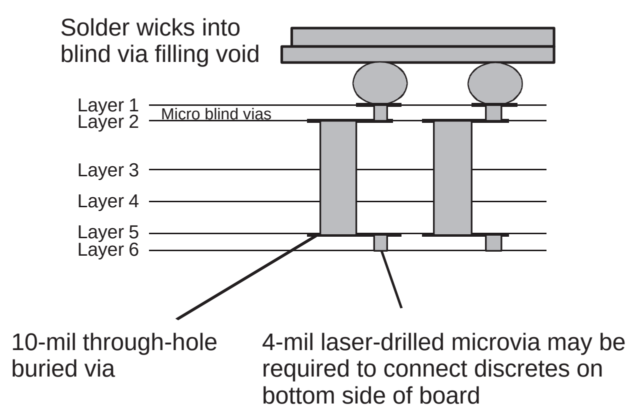
Advanced Design Methods

Another option is to use a combination of blind and buried vias. Blind vias connect either the top or bottom side of the board to inner layers. Buried vias usually connect only the inner layers. Figure 12 illustrates this method using 4-mil laser-drilled microvias in the center of the pads and burying the dog bone on layer 2.

Since the buried via does not extend through the underside of the board, the designer can use another set of laser-drilled blind microvias, if needed, to connect the bypass capacitors and other discrete components to the bottom side.

More information on these advanced techniques is available by contacting your local TI field sales office.

Figure 12. Buried Vias



2
Reliability

Daisy-Chained Units

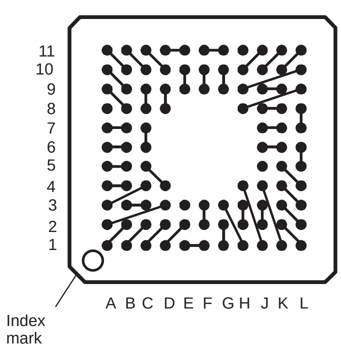
Daisy-chained units are used to gain experience in the handling and mounting of CSPs, for board-reliability testing, to check PCB electrical layouts, and to confirm the accuracy of the mounting equipment. To facilitate this, Texas Instruments offers daisy-chained units in all production MicroStar BGA packages.

Each daisy-chained pinout differs slightly depending on package layout. An example is shown in Figure 13. Daisy-chained packages are wired to provide a continuous path through the package for easy testing. TI issues a net list for each package, which correlates each ball position with a corresponding wire pad number. The daisy-chained net list is a special case of the general net list shown in Figure 14. Package net lists and daisy-chained net lists for all production packages are included in Appendix B.

A PCB layout for a 144-GGU daisy-chained package is shown in Figure 15. When a daisy-chained package is assembled on the PCB, a complete circuit is formed, which allows continuity testing. The circuit includes the solder balls, the metal pattern on the die, the bond wires, and the PCB traces. The entire package or only a quadrant can be interconnected and tested. A diagram of the test configuration is shown in Figure 16.

Figure 13. Daisy-Chained Pinout List

100GGT Top View



A1	–	B2	L1	–	K2	L11	–	K10	A11	–	B10
B1	–	C2	L2	–	K3	K11	–	J10	A10	–	B9
C1	–	D2	L3	–	K4	J11	–	H10	A9	–	B8
D1	–	E2	L4	–	K5	G9	–	G10	B7	–	A7
F3	–	F2	J6	–	K6	F9	–	F10	C7	–	C6
E1	–	F1	L5	–	L6	G11	–	F11	B6	–	A6
G1	–	G2	L7	–	L8	E11	–	D11	B5	–	A5
G3	–	H1	K7	–	J7	E10	–	E9	C5	–	D4
H2	–	H3	K8	–	J8	D10	–	C11	A4	–	B4
H4	–	J1	L9	–	H8	D9	–	D8	C4	–	A3
J2	–	J3	K9	–	J9	C10	–	B11	B3	–	C3
K1	–	J4	L10	–	H9	C9	–	C8	A2	–	D3

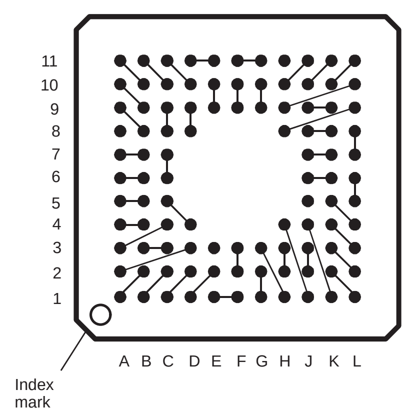
NC – E3, J5, H11, A8

Reliability Data

Reliability is one of the first questions designers ask about any new packaging technology. They want to know how well the package will survive handling and assembly operation, and how long it will last on the board. The elements of package reliability and system reliability, while related, focus on different material properties and characteristics and are tested by different methods.

Figure 14. General Net List

100GGT Top View



PIN#		BALL#	PIN#		BALL#	PIN#		BALL#	PIN#		BALL#
1	–	A1	26	–	L1	51	–	L11	76	–	A11
2	–	B2	27	–	K2	52	–	K10	77	–	B10
3	–	B1	28	–	L2	53	–	K11	78	–	A10
4	–	C2	29	–	K3	54	–	J10	79	–	B9
5	–	C1	30	–	L3	55	–	J11	80	–	A9
6	–	D2	31	–	K4	56	–	H10	81	–	B8
7	–	E3	32	–	J5	57	–	H11	82	–	A8
8	–	D1	33	–	L4	58	–	G9	83	–	B7
9	–	E2	34	–	K5	59	–	G10	84	–	A7
10	–	F3	35	–	J6	60	–	F9	85	–	C7
11	–	F2	36	–	K6	61	–	F10	86	–	C6
12	–	E1	37	–	L5	62	–	G11	87	–	B6
13	–	F1	38	–	L6	63	–	F11	88	–	A6
14	–	G1	39	–	L7	64	–	E11	89	–	B5
15	–	G2	40	–	L8	65	–	D11	90	–	A5
16	–	G3	41	–	K7	66	–	E10	91	–	C5
17	–	H1	42	–	J7	67	–	E9	92	–	D4
18	–	H2	43	–	K8	68	–	D10	93	–	A4
19	–	H3	44	–	J8	69	–	C11	94	–	B4
20	–	H4	45	–	L9	70	–	D9	95	–	C4
21	–	J1	46	–	H8	71	–	D8	96	–	A3
22	–	J2	47	–	K9	72	–	C10	97	–	B3
23	–	J3	48	–	J9	73	–	B11	98	–	C3
24	–	K1	49	–	L10	74	–	C9	99	–	A2
25	–	J4	50	–	H9	75	–	C8	100	–	D3

Figure 15. PCB Layout for Daisy-Chained Unit

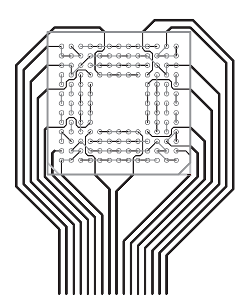
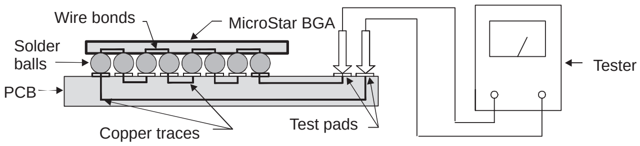


Figure 16. Daisy-Chain Test Configuration



Package reliability focuses on materials of construction, thermal flows, material adherence/delamination issues, resistance to high temperatures, moisture resistance and ball/stitch bond reliability. Thorough engineering of the package is performed to prevent delamination caused by the interaction of the substrate material and the mold compound.

TI subjects each MicroStar BGA to rigorous qualification testing before the package is released to production. These tests are summarized in Table 1. All samples used in these tests are preconditioned according to Joint Electronic Device Committee (JEDEC) A113 at various levels. Typical data is presented in Table 2. MicroStar BGA packages have proven robust and reliable.

Board-level reliability (BLR) issues generally focus on the complex interaction of various materials under the influence of heat generated by the operation of electronic devices. Not only is there a complex thermal situation caused by multiple heat sources, but there are cyclical strains due to expansion mismatches, warping and transient conditions, non-linear material properties, and solder fatigue behavior influenced by geometry, metallurgy, stress relaxation phenomenon, and cycle conditions. In addition to material issues, board and package design can influence reliability. Thermal management from a system level is critical for optimum reliability, and thermal cycling tests are generally used to predict behavior and reliability. Many of these are used in conjunction with solder fatigue life models using a modified Coffin-Manson strain range-fatigue life plots.

Table 1. Package-Level Reliability Tests†

Test Environments	Conditions	Read Points
HAST	85RH/85°C	600 hrs. 1000 hrs.
Autoclave	121°C, 15 psig	96 hrs. 240 hrs.
Temp. Cycle	–55/125°C –65/150°C‡	500 cycles 750 cycles 1000 cycles
Thermal Shock	–65/150°C‡ –55/125°C	200 cycles 500 cycles 750 cycles 1000 cycles
HTOL	125°C, Op. voltage	500 hrs. 600 hrs. 1000 hrs.
HTOL‡	140°C, Op. voltage	500 hrs.
HTOL‡	155°C, Op. voltage	240 hrs.
Bake‡	150°C 170°C	600 hrs. 1000 hrs. 420 hrs.
HAST‡	130°C	96 hrs.

† All samples used in these tests are preconditioned according to Joint Electronic Device Committee (JEDEC) A113 at various levels.
‡ Optional tests. One or more of them may be added to meet customer requirements.

Table 2. Package-Level Reliability Test Results

		Package Types					
	Leads	64	80	144		196	
	Body (mm)	8 x 8	10 x 10	12 x 12		15 x 15	
	Device	MSP	ASP	DSP		DSP	
	Die (mm)	5.3 x 5.8	7.5 x 7.5	9.3 x 9.5			
	Level	4	2	2a	4	3	
Test Environment		**Failures/Sample Size**					
Autoclave	(240 hrs.)	0/70	0/78	0/77	0/77	0/77	
T/C, –55/125°C	(1000 cycles)	0/116	0/78	0/77	0/77	0/76	
T/S, –65/150°C	(500 cycles)		0/78				
	(750 cycles)			0/77			
	(1000 cycles)	0/116			0/77	0/77	
HAST, 85°C/85%RH	(1000 hrs.)					0/78	
	(1250 hrs.)	0/115		0/77			
150°C Storage	(600 hrs.)	0/43			0/77	0/77	0/77
	(1000 hrs.)		0/78				
HTOL	(1000 hrs.)	0/116					

In addition to device/package testing, board-level reliability testing has been extensively performed on the MicroStar BGA packages. Various types of daisy-chained packages were assembled to special boards shown in Figure 17. Electrical measurements were made in the initial state and then at intervals after temperature cycles were run. The overall test conditions are shown in Figure 18. A summary of a wide range of board-level reliability is shown in Table 3. This data includes testing by TI and by end manufacturers.

Table 4 summarizes conclusions from the testing. Two important conclusions are that the PCB pad size needs to match the via size, and that solder paste is needed for attachment to give optimal reliability.

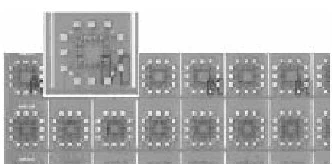
Figure 17. Board-Level Reliability Test Boards

Board Material FR-4

Structure: Two external metal layers
Traces: 1oz cu design rule 100 µm (4 mils) width, 100 µm (4 mils) space
Paste: Eutectic (SENJU 63-330F-21-10.5)
Paste thickness: 0.15 µm
Board thickness: 31 mils

Reflow profile: 225°C max, time above 200°C is 50 sec, time above 150°C is 240 sec
Screen opening: match land pad diameter
Precondition: Level 3

TI-Houston test board



TI-HIJI test board

Reliability Calculations

Another important aspect of predicting how a package will perform in any given application is reliability modeling. Thermal, electrical, and thermomechanical modeling, verified by experimental results, provide insight into system behavior, shorten package

Figure 18. Board-Level Reliability Test Data

Test condition: Open short @25°C, 10% resistance change or 200 Ω
Sample size: Greater or equal to 32
Temperature cycle range: –40°C to 125°C
Sampling rate: Every 100 cycles, up to first failure; every 50 cycles thereafter up to 1000 cycles; every 100 cycles between 1000 to 1500 cycles; every 250 cycles between 1500 to 2500 cycles; Test stopping point min (2500 cycles, 50% failures)

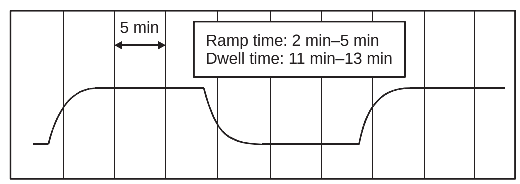


Table 3. Board-Level Reliability Summary

Conditions (With Solder Paste)						Failures/Sample Size						
						Requirements			Extended Range			
Package	TI Mfg Site Test Site	Body (mm)	Pitch (mm)	Die (mm)	Temp. Cycle (°C)	500	800 (Cycles)	1000	1100	1200	1300 (Cycles)	1500
GGU 144 balls	TI HIJI TI HIJI	12 x 12	0.8	8.8 x 8.8	–40/125	0/85	0/85	0/85	4/85	5/77	5/72	15/39
GGU 144 balls	TI Philippines TI HIJI	12 x 12	0.8	8.8 x 8.8	–40/125	0/36	0/36	0/36	0/36	0/36	0/36	1/35
GGF 100 balls	TI HIJI TI HIJI	10 x 10	0.5	6.6 x 6.6	–25/125	0/32	0/32	0/32	0/32	0/32	0/16	6/16
GHC 196 balls	TI TIPI TI Hou	15 x 15	1.0	8.8 x 8.8	–40/125	0/62	0/62	0/62	0/62	0/62	0/62	4/62
GGU 144 balls	TI Philippines Customer A	12 x 12	0.8	8.8 x 8.8	–40/100	0/180	0/180	0/180	0/180	–	–	–
GGW 176 balls	TI HIJI Customer B	15 x 15	0.8	6.6 x 6.6	–25/125	0/35	0/35	0/35	0/35	0/35	0/35	1/35
GGM 80 balls	TI HIJI Customer C	10 x 10	0.8	5.0 x 5.0	–40/125	0/12	0/12	0/12	–	–	–	0/10

Table 4. Summary of Significant BLR Improvements

Condition	Improved BLR ⇒		
Die size	Larger	⇒	Smaller
Die edge	Over balls	⇒	Within ball matrix
Ball count	Smaller	⇒	Larger
Ball size	Smaller	⇒	Larger
PCB pad size	Over/undersized	⇒	Matches package via (for NSMD ~90% of via)
Solder paste	None or insufficient	⇒	Thickness 0.15 nom. (type matches reflow)

development time, predict system lifetimes, and provide an important analytical tool. In applications such as BGAs, where the interconnections are made through solder balls, the useful life of the package is, in most cases, dependent on the useful life of the solder itself. This is an area that has been studied extensively, and very accurate models for predicting both solder behavior and interpreting accelerated life testing exist.

The current methodology employed at Texas Instruments includes both extensive model refinement and constant experimental verification. For a given package, a detailed 2D Finite Element Model (FEM) is constructed. This model will be used to carry out 2D plain strain elastoplastic analysis to predict areas of high stress. These models also account for the thermal variation of material properties, such as Modulus of Elasticity, Coefficient of Thermal Expansion, and Poisson's Ratio as a function of temperature. These allow the FEM to calculate the thermomechanical plastic strains in the solder joints for a given thermal loading.

The combination of Finite Element Analysis (FEA), accurate thermal property information, and advanced statistical methods allows prediction of the number of cycles to failure for various probability levels. Using the assumption that cyclic fatigue lifetime follows a Weibull distribution, various probability levels can be calculated. For these calculations, the Weibull shape parameter used is $\beta = 4$, which is based on experimental data calibration. It is also consistent with available experimental data found in the literature for leadless packages. This then results in the following equation:

$$Nf(x\%) = Nf(50\%)[\ln(1–0.01x)/\ln(0.5)]1/\beta$$

Using this equation, and using the plastic strain εp in combination with the S-N curves, the data below is an example of the accuracy possible with this method:

Sample Finite Element Simulation and Life Prediction:
144 GGU @ T/C: –40/125°C

{Model}→ εp = 0.353% on the outmost joint
→ Nf(50%)= 4434 cycles

→ Nf(1%) = 1539 cycles

{BLR Testing}→ –40/125°C (10 min/10 min)
→ Nf(1%) = 1657 cycles

Modeling is most useful in exploring changes in materials, designs and process parameters without the need to build experimental units. For example, modeling was used to study the effects of changes in board thickness and pad size. Table 5 shows the simulated effects of pad size and board thickness on the fatigue life of a 144-GGU package.

Table 5. Effects of Pad Size and Board Thickness on Fatigue Life

Example1: Effects of pad size on fatigue life

- Package: 144 GGU
- Die: 8.8 x 8.8 x 0.279 mm
- Board: FR-4 board 52 mils thick

Pad Dia. (mils)	Pad Standoff (mm)	Solder Center Dia. (mm)	Plastic Strain (%)	Nf (1%) (cycles to failure)	Difference
12	0.3847	0.4908	0.4400	998	0.88x
13	0.3689	0.4951	0.4127	1134	1
14	0.3523	0.5005	0.3908	1263	1.11x
15	0.3350	0.5060	0.3741	1377	1.21x

Example 2: Effects of board thickness on fatigue life

- Package: 144 GGU
- Die: 8.8 x 8.8 x 0.279 mm
- Board: FR-4
- Pad Size: 13 mils

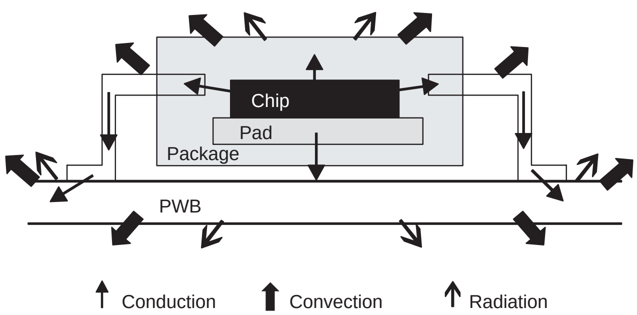
Board Thickness (mils)	Plastic Strain (%)	Nf (1%) (cycles to failure)	Difference
50	0.4095	1152	1
31	0.393	1249	1.08x

Package Characteristics

Texas Instruments has extensive package characterization capabilities, including an electrical measurements lab with TDR/LRC (Time Domain Reflectometer/inductance resistance capacitance) and network analysis capabilities, a thermal measurements lab with JEDEC standard test conditions up to 1000 watts, and extensive electrical, thermal, and mechanical modeling capability. Modeling was implemented at TI starting in 1984. Stress analysis is done with the Ansys Analysis tool, which provides full linear, nonlinear, 2D and 3D capabilities for solder reliability, package warpage, and stress analysis studies. An internally developed tool (PACED™) is used for electrical modeling that gives 2.5D and full 3D capability for LRC models, transmission lines, lossy dielectrics, and SPICE deck outputs. The thermal modeling tool was also internally developed (ThermCAL™) and it provides full 3D automatic mesh generation for most packages. Complex geometries, transient analysis, and anisotropic materials can be modeled with it. With these capabilities, a full range of modeling from device level through system level can be provided. Package modeling is used to predict package performance at the design stage, to provide a package development tool, to aid qualification by similarity, and is used as a failure analysis tool.

Figure 19. Thermal Modeling Process

Heat-Transfer Paths



(TQFP shown for illustration purposes)

- **Model's three heat-transfer mechanisms:**
  - Conduction
  - Convection
  - Radiation
- **Method:**
  - Define solid
  - Mesh solid
  - Solve large number of simultaneous equations relating each defined mesh point to each other
- **Sources of error:**
  - Convection coefficients
  - Material properties
  - Solid definition inaccuracies

Thermal Modeling

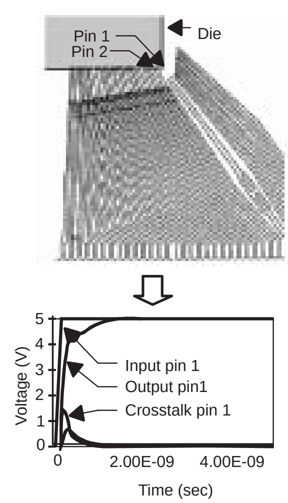
Figure 19 outlines the thermal modeling process. Data for each package is included in Appendix B.

Electrical Modeling

Figure 20 outlines the electrical modeling process. Data for each package is included in Appendix B.

Figure 20. Electrical Modeling Process

- Calculates inductances, capacitances, resistances, transmission line characteristics of package geometries
- Uses as loads for circuit simulation
- Process
  - Select solution algroithms for problem domain
  - Identify package structures to be modeled
  - Generate spice deck of package parameters
  - Simulate impact on driver output waveforms
  - Calculate ground/power bounce



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3

Surface-Mounting MicroStar BGA Packages

Surface-mount technology (SMT) has evolved over the past decade from an art into a science with the development of design guidelines and rules. While these guidelines are specific enough to incorporate many shared conclusions, they are general enough to allow flexibility in board layouts, solder pastes, stencils, fixturing, and reflow profiles. From experience, most assembly operations have found MicroStar BGA packages to be robust, manufacturing-friendly packages that fit easily within existing processes and profiles. In addition, they do not require special handling. However, as ball pitch becomes smaller, layout methodology and placement accuracy become more critical. Below is a review of the more important aspects of surface-mounted CSPs. The suggestions provided may aid in efficient, cost-effective production.

Design for Manufacturability (DFM)

A well-designed board that follows the basic surface-mount technology considerations greatly improves the cost, cycle time, and quality of the end product. Board design should comprehend the SMT-automated equipment used for assembly, including minimum and maximum dimensional limits and placement accuracy. Many board shapes can be accommodated, but the front of the board should have a straight and square edge to help machine sensors detect it. While odd-shaped or small boards can be assembled, they require panelization or special tooling to process in-line. The more irregular the board—non-rectangular with no cutouts—the more expensive the assembly cost.

Fiducials (the optical alignment targets that align the module to the automated equipment) should allow vision-assisted equipment to accommodate the shrink and stretch of the raw board during processing. They also define the coordinate system for all automated equipment, such as printing and pick-and-place. The following guidelines may be helpful:

- Automated equipment requires a minimum of two and preferably three fiducials.
- A wide range of fiducial shapes and sizes can be used. Among the most useful is a circle 1.6 mm in diameter with an annulus of 3.175/3.71 mm. The outer ring is optional, but no other feature may be within 0.76 mm of the fiducial.
- The most useful placement for the fiducials is an L configuration, which is orthogonal to optimize the stretch/shrink algorithms. When possible, the lower left fiducial should be the design origin (coordinate 0,0).
- All components should be within 101.6 mm of a fiducial to guarantee placement accuracy. For large boards or panels, a fourth fiducial should be added.

If the edges of the boards are to be used for conveyer transfer, a cleared zone of at least 3.17 mm should be allowed. Normally, the longest edges of the board are used for this purpose, and the actual width is dependent on equipment capability. While no component lands or fiducials can be in this area, breakaway tabs may be.

Interpackage spacing is a key aspect of DFM, and the question of how close you can safely put components to each other is a critical one. The following component layout considerations are recommendations based on TI experience:

- There should be a minimum of 0.508 mm between land areas of adjacent components to reduce the risk of shorting.
- The recommended minimum spacing between SMD discrete component bodies is equal to the height of the tallest component. This allows for a 45° soldering angle in case manual work is needed.
- Polarization symbols need to be provided for discrete SMDs (diodes, capacitors, etc.) next to the positive pin.
- Pin-1 indicators or features are needed to determine the keying of SMD components.
- Space between lands (under components) on the backside discrete components should be a minimum of 0.33 mm. No open vias may be in this space.
- The direction of backside discretes for wave solder should be perpendicular to the direction through the wave.
- Do not put SMT components on the bottom side that exceed 200 grams per square inch of contact area with the board.
- If space permits, symbolize all reference designators within the land pattern of the respective components.
- It is preferable to have all components oriented in well-ordered columns and rows.
- Group similar components together whenever possible.
- Room for testing needs to be allowed.

Solder Paste

TI recommends the use of paste when mounting MicroStar BGAs. The use of paste offers the following advantages:

- It acts as a flux to aid wetting of the solder ball to the PCB land.
- The adhesive properties of the paste will hold the component in place during reflow.

- It helps compensate for minor variations in the planarity of the solder balls.
- Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give an optimum joint.

Paste selection is normally driven by overall system assembly requirements. In general, the “no clean” compositions are preferred due to the difficulty in cleaning under the mounted component. Most assembly operations have found that no changes in existing pastes are required by the addition of MicroStar BGA, but due to the large variety of board designs and tolerances, it is not possible to say this will be true for any specific application.

Nearly as critical as paste selection is stencil design. A proactive approach to stencil design can pay large dividends in assembly yields and lower costs. In general, MicroStar BGA packages are special cases of BGA packages, and the general design guidelines for BGA package assembly applies to them as well. There are some excellent papers on BGA assembly, so only a brief overview of issues especially important to MicroStar BGA packages will be presented here.

The typical stencil hole diameter should be the same size as the land area, and 125- to 150-µm-thick stencils have been found to give the best results. Good release and a consistent amount of solder paste and shapes are critical, especially as ball pitches decrease. The use of metal squeegee blades, or at the very least, high durometer polyblades, is important in achieving this. Paste viscosity and consistency during screening are some variables that require close control.

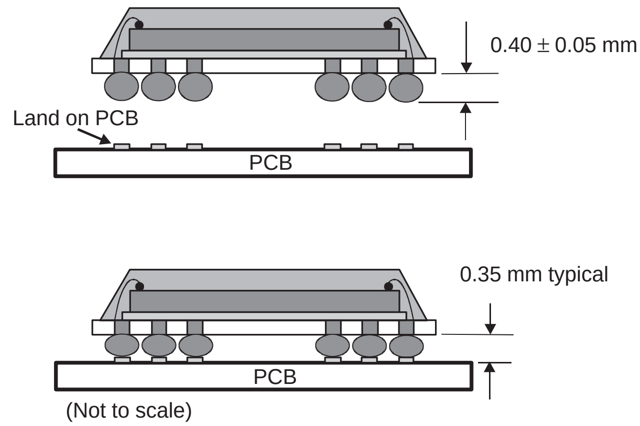
Solder Ball Collapse

In order to produce the optimum solder joint, it is important to understand the amount of collapse of the solder balls, and the overall shape of the joint. These are a function of:

- The diameter of the package solder ball via.
- The volume and type of paste screened onto the PCB.
- The diameter of the PCB land.
- The board assembly reflow conditions.
- The weight of the package.

The original ball height on the package for a typical 0.8-mm-pitch package is 0.40 mm. After the package is mounted, this typically drops to 0.35 mm, as illustrated in Figure 21.

Figure 21. Solder Ball Collapse



Controlling the collapse, and thus defining the package standoff, is critical to obtaining the optimum joint reliability. Generally, a larger standoff gives better solder joint fatigue strength, but this should not be achieved by reducing the board land diameter. Reducing the land diameter will increase the standoff, but will also reduce the minimum cross-section area of the joint. This, in turn, will increase the maximum shear force at the PCB side of the solder joint. Thus, a reduction of land diameter will normally result in a worse fatigue life, and should be avoided unless all the consequences are well understood.

Reflow

Solder reflow conditions are the next critical step in the mounting process. During reflow, the solvent in the solder paste evaporates, the flux cleans the metal surfaces, the solder particles melt, wetting of the surfaces takes place by wicking of molten solder, the solder balls collapse, and finally solidification of the solder into a strong metallurgical bond completes the process. The desired end result is a uniform solder structure strongly bonded to both the PCB and the package with small or no voids and a smooth, even fillet at both ends. Conversely, when all the steps do not carefully fit together, voids, gaps, uneven joint thickness, discontinuities, and insufficient fillet can occur. While the exact cycle used depends on the reflow system and paste composition, there are several key points all successful cycles have in common.

The first of these is a warm-up period sufficient to safely evaporate the solvent. This can be done with a pre-heat or a bake, or, more commonly, a hold in the cycle at evaporation temperatures. If there is less solvent in the paste (such as in a high-viscosity, high-metal-content paste), then the hold can be shorter. However, when the hold is not long enough to get all of the solvent out or too fast to allow it to evaporate, many negative things happen. These range from solder-particle splatter to trapped gases, which can cause voids and embrittlement. A significant number of reliability problems with solder joints can be solved with the warm-up step, so it needs careful attention.

The second key point that successful reflow cycles have in common is uniform heating across the package and the board. Uneven solder thickness and non-uniform solder joints may be an indicator that the profile needs adjustment. There can also be a problem when different sized components are reflowed at the same time. Care needs to be taken when profiling an oven to be sure that the indicated temperatures are representative of what the most difficult to reflow parts are seeing. These problems are more pronounced with some reflow methods, such as infrared (IR) reflow, than with others, such as forced hot-air convection.

Finally, successful reflow cycles strike a balance among temperature, timing, and length of cycle. Mistiming may lead to excessive fluxing activation, oxidation, excessive voiding, or even damage to the package. Heating the paste too hot too fast before it melts can also dry the paste, which leads to poor wetting. Process development is needed to optimize reflow profiles for each solder paste/flux combination.

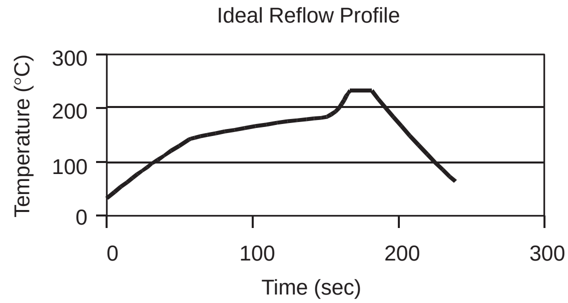
The profile shown in Figure 22 is an ideal one for use in a forced-air-convection furnace, which is the most highly recommended type. The best results have been found in a nitrogen atmosphere.

The guidelines upon which this profile is based, also shown in Figure 22, are general. Modification to the ideal reflow profile will be driven by the interplay of solder-paste particle size and flux percentage with process variables such as heating rates, peak temperatures, board construction factors and atmosphere. These modifications are dependent upon specific applications.

It should be noted that while they are more rugged than most CSP-type packages, many MicroStar BGA packages are still slightly moisture-sensitive at the time of printing of this Reference Guide. The time out of a dry environment should be controlled according to the label on the packing material. This will prevent moisture absorption problems with the package such as “popcorning,” or delamination.

Figure 22. Ideal Reflow Profile

RT to 140°C:	60–90 sec
140°C to 180°C:	60–120 sec
Time above 183°C:	60–150 sec
Peak temperature:	220°C ± 5°C
Time within 5°C peak temperature:	10–20 sec
Ramp-down rate:	6°C/sec maximum



Note: This is an ideal profile, and actual conditions obtained in any specific reflow oven will vary. This profile is based on convection or RF plus forced convection heating.

Other concerns with BGA packages are those caused by a PCB bowing or twisting during reflow. As PCBs get thinner, these problems will become more significant. Potential problems from these effects will show up as open pins, hourglass solder joints, or solder discontinuities. Proper support of the PCB through the furnace, balancing the tab attachments to a panel, and, in worst cases, using a weight to stiffen the PCB can help prevent this. In general, the small size of CSPs create fewer problems than standard BGAs. It is also true that BGAs generally have fewer problems than leaded components.

Inspection

MicroStar BGA packages have been designed to be consistent with very high-yield assembly processes. Because of their relatively light weight, MicroStar BGA packages tend to self-align during reflow. Since the pitch of the ball pattern is large compared to that of fine-pitch leaded packages, solder bridging is rarely encountered. It is recommended that a high-quality solder joint assembly process be developed using the various inspection and analytical techniques, such as cross-sectioning. Once a quality process has been developed, detailed inspection should not be necessary. Visual methods, while obviously limited, can offer valuable clues to the general stability of the process. Electrical checks can confirm interconnection. Both transmission X-rays and laminographic X-rays have proven to be useful nondestructive tools, if desired.

4

Packing and Shipping

MicroStar BGAs are shipped in either of two packing methods:

- Trays
- Tape and reel

Trays

Thermally resistant plastic trays are currently used to ship the majority of the packages. Each family of parts with the same package outline has its own individually designed tray. The trays are designed to be used with pick-and-place machines. Figure 23 gives typical tray details, and Table 6 shows the number of units per tray.

Figure 24 shows the packing method used to ship trays. Before the trays are sealed in the aluminum-lined plastic bag, they are baked in accordance with the requirements for dry-packing at the appropriate level.

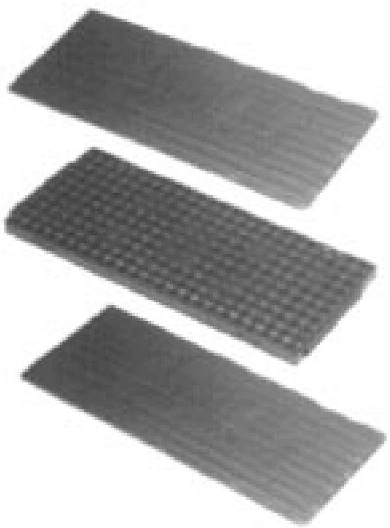
Figure 23. Shipping Tray Detail

Table 6. Number of Units per Shipping Tray

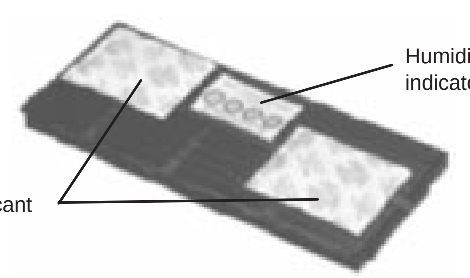
Body Size (mm)	Package Code	Matrix	Units/ Tray	Units/ Box
16 x 16	GZY, GHK	6 x 15	90	450
15 x 15	GGW,GHC	6 x 15	90	450
13 x 13	GHG, GHJ, GHV	8 x 20	160	800
12 x 12	GZG, GGB	8 x 20	160	800
11 x 11	GGT	8 x 20	160	800
10 x 10	GGF, GHZ, GGM	8 x 25	200	1000
8 x 8	GGV, GJJ	9 x 25	225	1125
9 x 13	GFZ, GHB, GHN	10 x 18	180	900

Figure 24. Packing Method for Trays

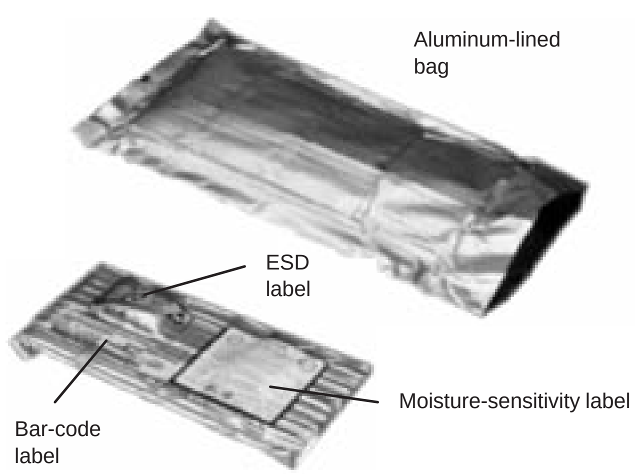
1. Arrange the stack of trays to be packed with a tray pad on top and bottom.



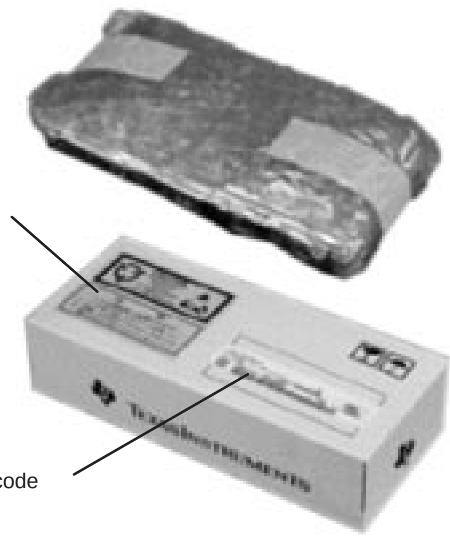
2. Strap the tray stack and pads together with four straps—three crosswise and one lengthwise. Then place the desiccants and the humidity indicator on top.



3. Place the lot inside the aluminum-lined bag and vacuum-seal it. Place the necessary labels on the sealed bag.



4. Wrap and tape bubble pack around the bag for a snug fit in the inner carton. Place the necessary labels on the inner carton.



5. Add bubble pack around the inner carton for a snug fit in the skidboard liner.

6. Place four foam corner spacers on the folded skidboard liner before placing it in the outer carton. An enhanced skidboard liner, which eliminates the need for foam corner spacers, may be used. Seal outer carton and apply necessary labels.

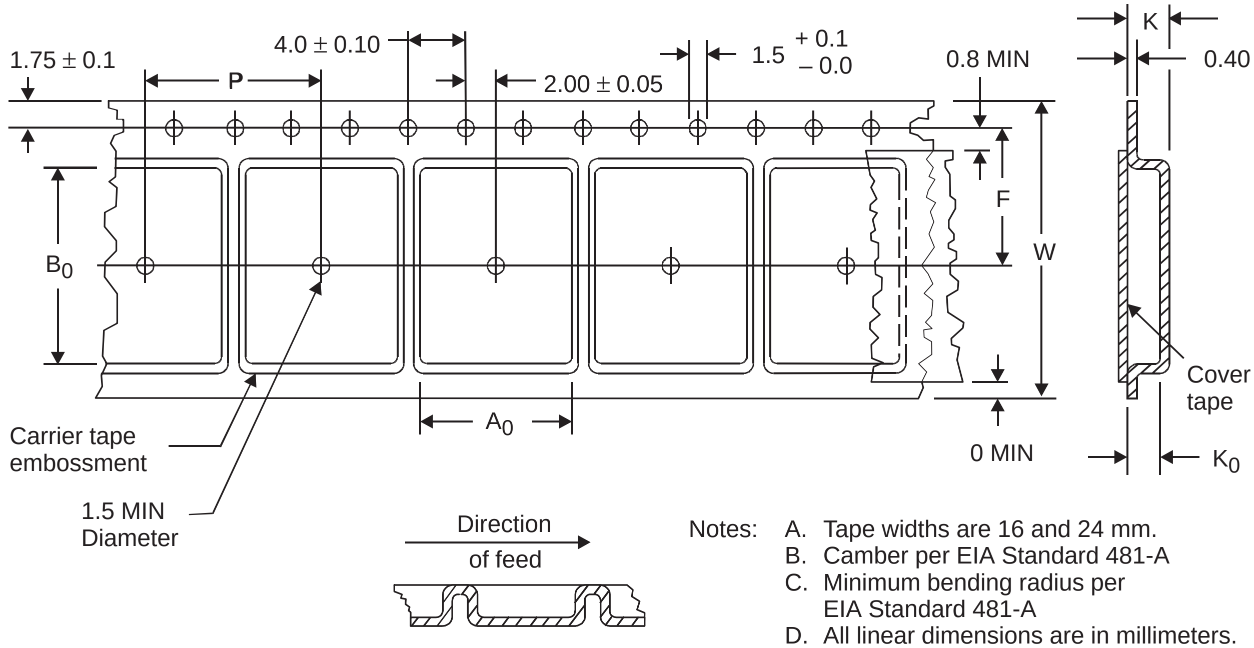
Tape-and-Reel Packing Method

The embossed tape-and-reel method is generally preferred by automatic pick-and-place machines. This will be the standard way MicroStar BGA packages will be shipped. Trays will remain an option for those customers who prefer them. The tape is made from an antistatic/conductive material. The cover tape, which peels back during use, is heat-sealed to the carrier tape to keep the devices in their cavities during shipping and handling. The tape-and-reel packaging used by Texas Instruments is in full compliance with EIA Standard 481-A, “Taping of Surface-Mount Components for Automatic Placement.” The static-inhibiting materials used in the carrier-tape manufacturing provides device protection from static damage, while the rigid, dust-free polystyrene reels provide mechanical protection and clean-room compatibility with dereeling equipment currently available on most high-speed automated placement systems.

Tape Format

Typical tape format is shown in Figure 25. The variables used in Figure 25 and Table 7 are defined as follows: W is the tape width; P is the pocket pitch; A_0 is the pocket width; B_0 is the pocket length; K_0 is the pocket depth; K is the maximum tape depth; and F is the distance between the drive hole and the centerline of the pocket.

Figure 25. Single Sprocket Tape Dimensions



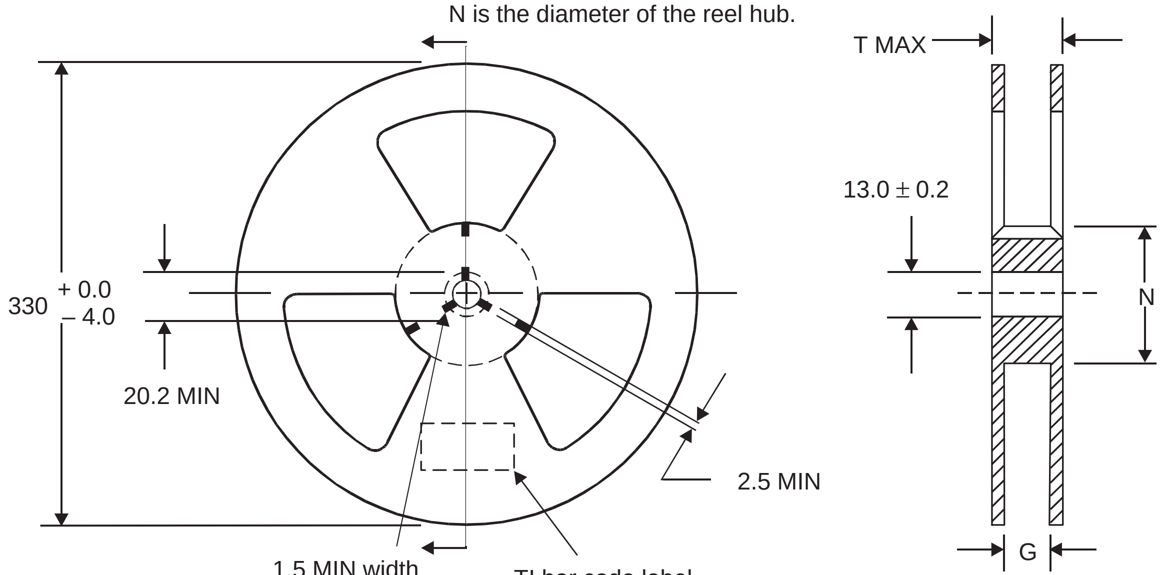
Notes: A. Tape widths are 16 and 24 mm.
B. Camber per EIA Standard 481-A
C. Minimum bending radius per EIA Standard 481-A
D. All linear dimensions are in millimeters.

Table 7. Tape Dimensions†

Tape Width (W)	Pocket Pitch (P)	Pocket Width (A_0)	Pocket Length (B_0)	Pocket Depth (K_0)	Max. Tape Depth (K)	Centerline to Drive Hole (F)	Package Size
16	12	8.2	8.2	1.7	2.0	7.5	8 x 8
24	16	10.2	10.2	1.7	2.0	11.5	10 x 10
24	16	11.35	11.35	1.9	2.2	11.5	11 x 11
24	16	12.4	12.4	1.9	2.2	11.5	12 x 12
24	20	15.25	15.25	2.2	2.5	11.5	15 x 15

† All dimensions are in millimeters.

Figure 26. Reel Dimensions



Note A: All linear dimensions are in millimeters.

Table 8. Reel Dimensions†

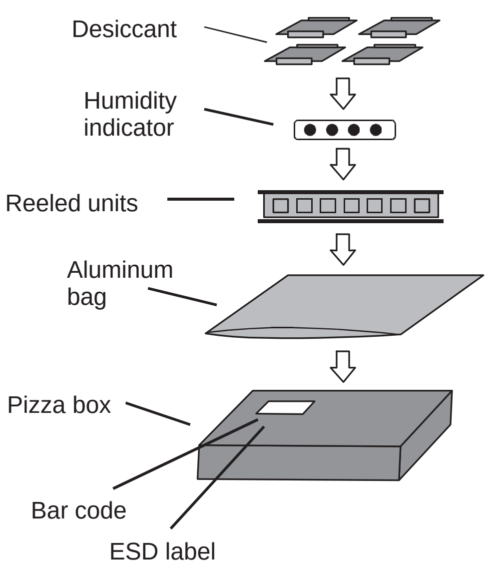
Tape Width (G)	Reel Hub Diameter (N)	Reel Total Thickness (T MAX)	Parts per Reel
16	100	28	1000
24	100	28	1000

† All dimensions are in millimeters.

The reels are shown in Figure 26. In this figure, G is the width of the tape, N is the diameter of the hub, and T is the total reel thickness.

After the parts are loaded into the reel, each individual reel is packed in its own “pizza” box for shipping, as shown in Figure 27.

Figure 27. Tape-and-Reel Packing



Device Insertion

Devices are inserted toward the outer periphery of the tape by placing the side with the device name face up and the side with the balls attached face down. The pin-1 indicator is placed in the top right-hand corner of the pocket, next to the sprocket holes.

Packaging Method

For reels, once the taping has been completed, the end of the leader is fixed onto the reel with tape. The product name, lot number, quantity, and date code are recorded on the reel and the cardboard box used for tape delivery. Each reel is separately packed in a cardboard box for delivery.

Trays are packed with five loaded trays and one empty tray on top for support and to keep packages secure. The stack is secured with stable plastic straps and sealed in a moisture-proof bag.

Customer-specific bar code labels can be added under request or general purchasing specification.

Moisture-sensitive packages are baked before packing and are packed within 8 hours of coming out of the oven. Both the tape-and-reel and the tray moisture-proof bags are sealed and marked with appropriate labeling warning that the packages inside the bags are dry-packed and giving the level of moisture sensitivity.

5
Sockets

The Design Challenge

The fine pitch of MicroStar BGA packages makes socketing a special challenge. Mechanical, thermal, and electrical issues must be accommodated by the socket designer. CSP packaging is at the cutting edge of package design and it appears that it is being adopted faster than any other previous package technology. Standards are only now beginning to be established. TI fully supports these efforts, and all MicroStar BGA outlines are being engineered to fit within JEDEC standards where they exist. For instance, all 0.8-mm-pitch packages fit within JEDEC MO205. While these standards detail the pitch and I/O placement, they do allow wide latitude for overall body size variation. The size of a specific package within the TI MicroStar BGA family is based on the package construction, and is independent of die size. Thus, a range of die sizes and I/Os within a family will have the same package dimensions. Each different family has a specific I/O pitch and array. For maximum socket versatility, an adapter or "personalizer" can be customized for each application, allowing a single-socket body to be used with many packages. This feature is especially useful in the early days as the technology is being developed and adopted and the total volume required is small.

Contacting the Ball

A number of different approaches for contacting the solder ball are shown schematically in Figure 28. The pinch style contact has been used extensively for contacting solder balls in conventional BGAs. A benefit of the pinch style is that the socket does not have to push down on the package to provide the necessary contact force to penetrate the oxide film on the solder balls. The issues in utilizing this approach for pitches below 1.27 mm involve:

1. Miniaturizing the contact
2. Developing injection-molding tooling for the pitch
3. Developing cost-effective manufacturing procedures for handling and assembling the fragile contact

For pitches of 0.75 mm and above, Texas Instruments has designed a pinch contact that satisfies all of these requirements. Further information on the availability of these sockets can be obtained from your local TI Field Sales representative.

The contact is designed to grip the solder ball with a pinching action. This not only provides electrical contact to the solder ball but also helps retain the package in the socket. The contact is shown in Figure 29. The contact is stamped and formed from a 0.12-mm-thick strip of CDA 172, the high-yield-strength beryllium copper alloy. This alloy is used for spring applications that are exposed to high stresses and temperatures because of its excellent stress relaxation performance and formability.

Figure 28. Approaches for Contacting the Solder Ball

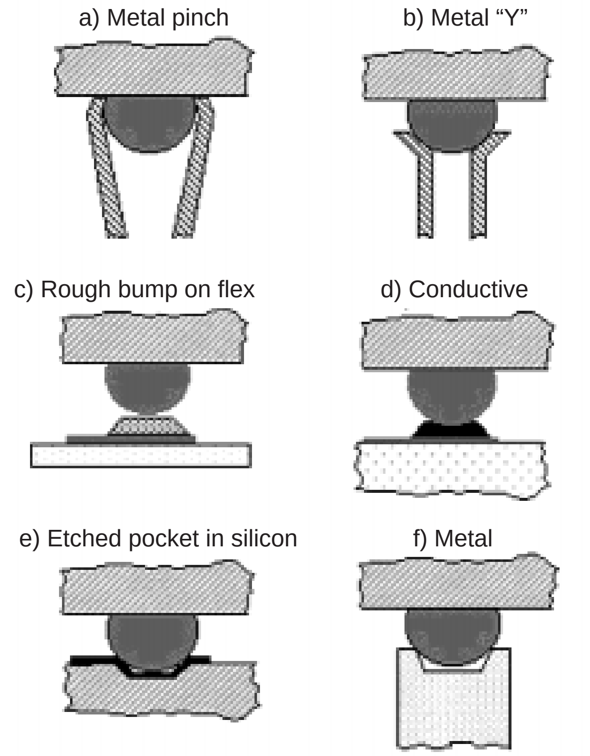
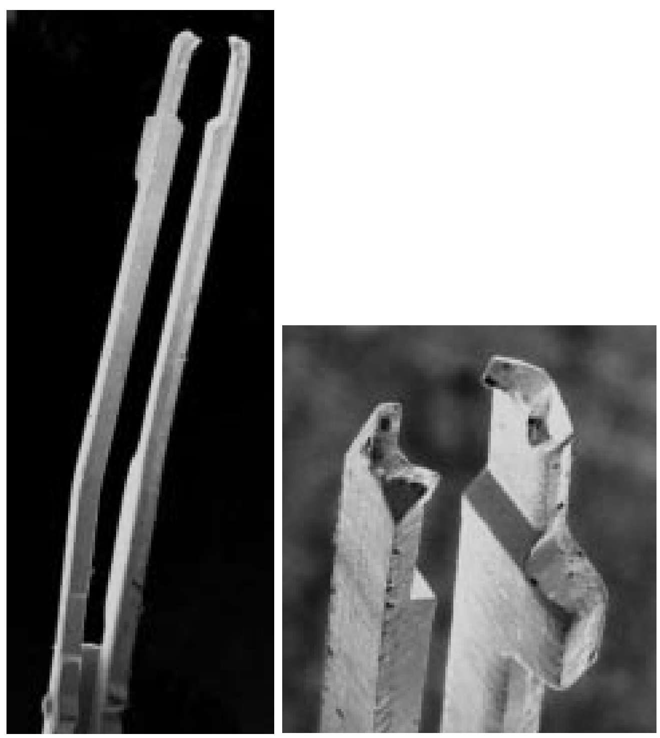
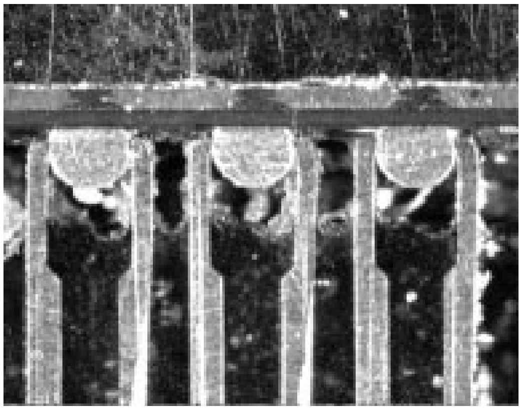


Figure 29. Pinch Contact for Solder Balls



Each contact incorporates two beams that provide an oxide-piercing interface with the sides of the balls above the central area—the equator. Since the contact is above the equator, the resultant force is downward and ensures package retention in the socket. No contact is made on the bottom of the solder ball and the original package planarity specifications are unchanged. A photomicrograph of the contact touching the solder balls is shown in Figure 30.

Figure 30. Contact Area on Solder Ball



The witness marks left on the solder ball from the contact are shown in Figure 31. This ball was contacted at room temperature and it is clear that there was no damage to the bottom of the ball or any witness marks from the contact above the equator.

The effect of burn-in on the probe marks was examined by simulating a cycle and placing a loaded socket into an oven at 125°C for 9 hours. The result is shown in Figure 32. The penetration of the contact into the solder ball due to the higher temperature is greater but is well within the acceptable range. There was no visible pickup of solder on the contact tips. This experiment is being continued to evaluate the impact of longer times on the witness marks and the solder pickup. The location of the contact pinch is clearly seen in this photograph.

Figure 31. Witness Marks on Solder Ball

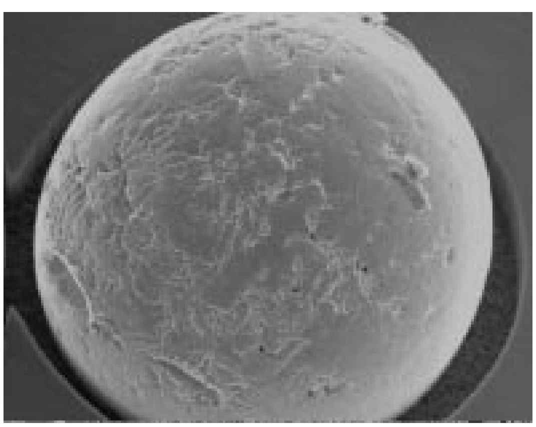
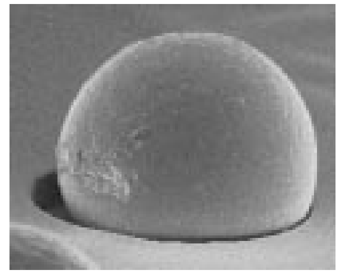


Figure 32. Effect of Burn-in on Probe Marks



Establishing Contact Force

Contact force is typically generated as a result of the deflection of the contact arm. The actual force generated is a function of the modulus of the material and the specific geometric details of the design. The solder ball diameters for CSPs tend to be small—in the range of 0.25 mm to 0.4 mm, which limits the deflection of the contact arm to a very small distance. Typically, this distance is half the ball diameter. This presents a challenge to the designer who must generate the required 15 grams of force at the contact tip, yet keep the bending stresses within the contact arms at a low enough value to achieve a 20K-cycle life. The contact force requirements are met by incorporating a pre-load, so that even for small displacements, the desired force is achieved and the socket can operate within acceptable stress levels.

The 15-gram target force is smaller than that associated with TSOP-type contact force levels, which require a 30-gram minimum. However, based on the contact tip geometry, this lower force translates to contact pressures that are high enough to achieve oxide penetration and good electrical continuity.

Conclusions and Future Work

The importance of continuing the development to 0.5-mm pitch is clear. End users want more and more electronic functionality in smaller and smaller packages. Sockets for testing these fine pitches are available today but are specialty and are considered too expensive for broad commercial application. Continued development includes innovative approaches as well as refining present methods, but at the time of the preparation of this Reference Guide, a clear-cut favorite technology had not emerged. For current progress in this and other areas of 0.5-mm-pitch technology, your local TI Field Sales representative can give you up-to-date information.

Growth rates as high as 400% for CSPs in 1998 over those in 1997 have been forecasted. The opportunity to participate in a market with this growth has provided the incentive for the socket companies to develop solutions for the infrastructure needed for burn-in test sockets. The issues of contacting the small, soft solder balls on CSPs have been solved. The price disparity between CSP sockets and TSOP sockets is to be expected during the early days of the introduction of a new technology and is due entirely to the embryonic state of the industry and the low volume. It is believed that once this packaging technology matures and volumes increase to those of conventional burn-in sockets, then the prices for sockets for CSPs will decrease and be more in line with other commercial sockets.

6
References

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James Forster, “Performance Drivers for Fine Pitch BGA Sockets,” *Chip Scale Processing*, June 1998.

Kevin Lyne, “Chip Scale Packaging From Texas Instruments: MicroStar BGA,” Texas Instruments Application Note, June 1997.

Gary Morrison, Les Stark, Ron Azcarte, S. Capistrano, K. Ano, K. Murata, M. Watanabe, T. Ohuchida, Y. Takahashi, Greg Ryan, “MicroStar BGA Packaging: Critical Interconnections,” SEMICON ’98.

Les Stark and M’hamed Idnabdeljalil, “MicroStar BGA vs. FC-CSP: Finite Element Simulation of BLR Performance: 144GGF Footprint,” Texas Instruments Application Note, August 1998.

Appendix

A

Frequently Asked Questions

Package Questions

Q. Do the solder balls come off during shipping?

A. No, this has never been observed. The balls are 100% inspected for coplanarity, diameter, and other physical properties prior to packing for shipment. Because solder is used during the ball-attachment process, uniformly high ball-attachment strengths are developed. Also, the ball-attachment strength is monitored frequently in the assembly process to prevent ball loss from vibration and other shipping forces.

Q. Is package repair possible? Are tools available?

A. Yes, some limited package repair is possible, and there are some semiautomatic M/C tools available. However, TI does not guarantee the reliability of repaired packages.

Q. What are the leads that appear on the package edge for? Are they connected to the inner pattern?

A. Those leads are used for plating connections during the plating of Ni/Au on the copper trace during the fabrication of the substrate. Since they do have electrical connection with the inner pattern, they can be used for test probing and signal analysis. There is no reliability risk with them.

Q. What is the composition and melting point of the solder balls?

A. The balls are a near-Sn/Pb eutectic solder that includes some additives to improve thermal fatigue life. The liquidus temperature is 178°C to 210°C.

Q. Is burn-in testing possible? How about ball damage?

A. There are commercial sockets available for 1.00-mm and 0.8-mm pitch package burn-in. Sockets for 0.5-mm pitch packages are now becoming available. Vendors include Texas Instruments, Yamaichi, Wells and Enplas. The ball damage observed falls within specified tolerances, so the testing does not affect board mount.

Q. Is tape-and-reel shipping available?

A. Tape-and-reel is the preferred method for shipping MicroStar BGA packages. Tray shipping methods are available upon customer request.

Q. What about actual market experience?

A. Since TI started production in May of 1996, well over 70 million units have been shipped. End products are primarily DSP Solutions such as wireless phones and digital camcorders where MicroStar BGA can create significant space savings. Technologies available in MicroStar BGAs include DSP, ASIC, Mixed Signal, and Linear devices.

Q. How does the packaging cost compare to QFPs?

A. CSPs are in many ways an ideal solution to cost reduction and miniaturization requirements. They offer enormous area reductions in comparison to QFPs and have increasing potential to do so without adding to system-level costs. In the best case, CSPs compete today on a cost-per-terminal basis with QFPs. For example, various CSPs from Texas Instruments are now available at cost parity with thin QFPs.

Assembly Questions

Q. What alignment accuracy is possible?

A. Alignment accuracy for the 0.8-mm-pitch package is dependent upon board-level pad tolerance, placement accuracy, and solder ball position tolerance. Nominal ball position tolerances are specified at ±80 µm. These packages are self-aligning during solder reflow, so final alignment accuracy may be better than placement accuracy.

Q. Can the solder joints be inspected after reflow?

A. Process yields of 5-ppm (parts per million) rejects are typically seen, so no final in-line inspection is required. Some customers are achieving satisfactory results during process set-up with lamographic X-ray techniques.

Q. How do the board assembly yields of MicroStar BGAs compare to QFPs?

A. Many customers are initially concerned about assembly yields. However, once they had MicroStar BGAs in production, most of them report improved process yields compared to QFPs. This is due to the elimination of bent and misoriented leads, the wider terminal pitch than with 0.5-mm-pitch QFPs, and the ability of these packages to self-align during reflow. The collapsing solder balls also mean that the coplanarity is improved over leaded components.

Q. Are there specific recommendations for SMT processing?

A. Texas Instruments recommends alignment with the solder balls for the CSP package, although it is possible to use the package outline for alignment. Most customers have found they do not need to change their reflow profile.

Q. Can the boards be repaired?

A. Yes, there are rework and repair tools and profiles available. We strongly recommend that removed packages be discarded.

Q. Is TI developing a lead-free version of MicroStar BGAs?

A. Yes, Texas Instruments is working toward eliminating lead in the solder balls to comply with lead-free environmental policies. The lead-free solder is in final evaluation. Only the solder will change, not the package structure or the mechanical dimensions. The solder system under development is based on Sn-Ag metallurgy. Check with your local TI Field Sales representative for sample availability.

Q. What size land diameter for these packages should I design on my board?

A. Land size is the key to board-level reliability, and Texas Instruments strongly recommends following the design rules included in this bulletin.

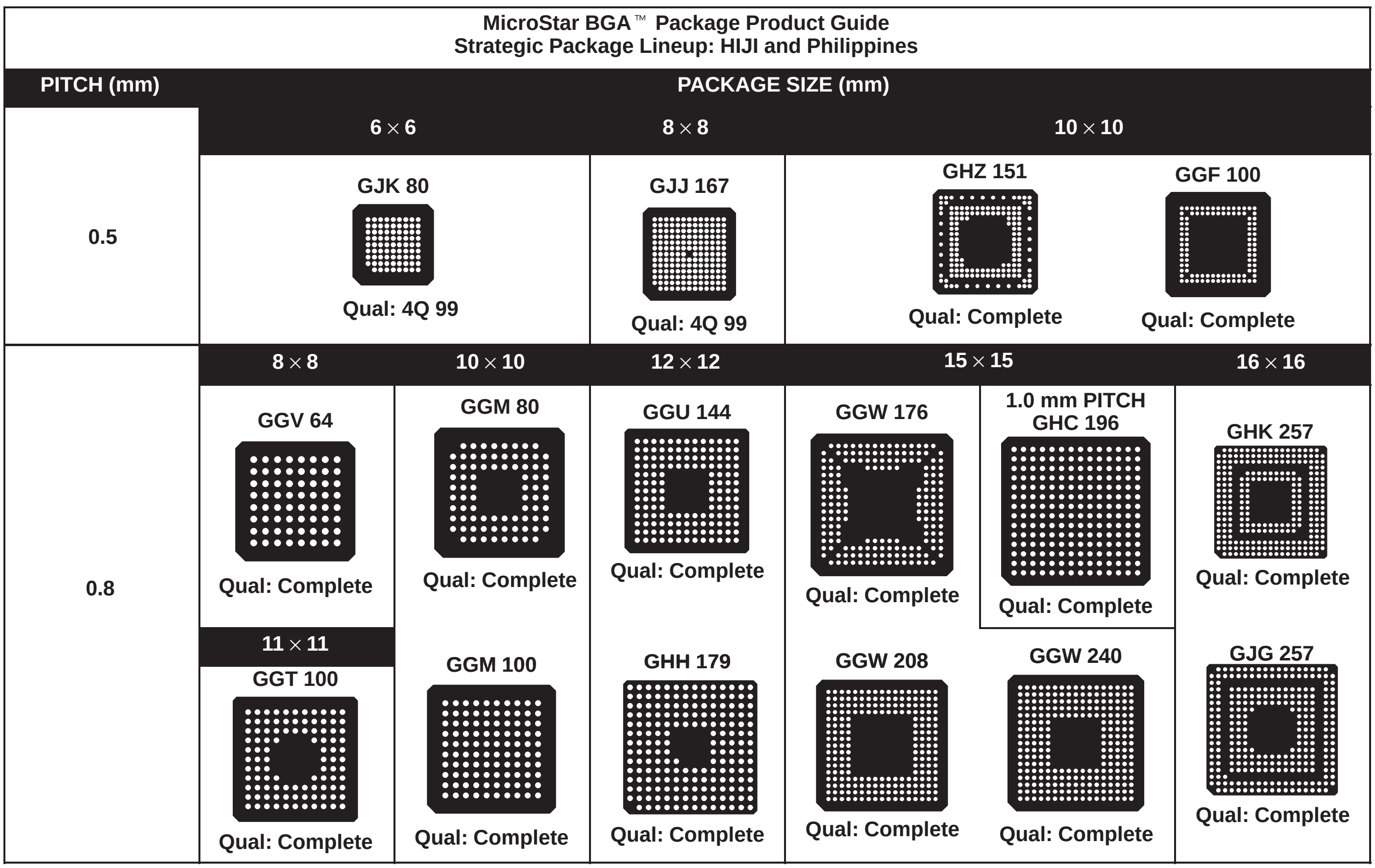
Appendix

B

Package Data Sheets

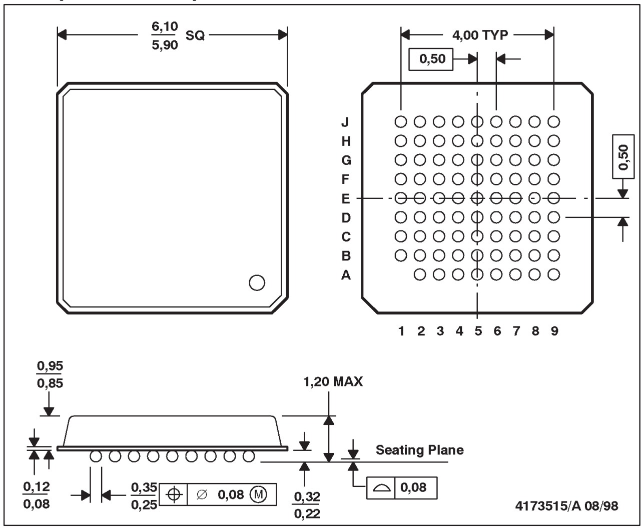
Figure 33 shows TI's strategic package lineup, followed by the package data sheets for the package families offered as standard products by Texas Instruments. As new packages are added, they will be placed on the strategic package lineup. Contact your TI field sales office for information on the most current offerings. Samples are available for all packages shown in Figure 33.

Figure 33. TI's Strategic Package Line-Up



80GJK PACKAGE OUTLINE
(6 x 6 mm, 0.5 mm pitch)

GJK (S-PBGA-N80) **PLASTIC BALL GRID ARRAY**

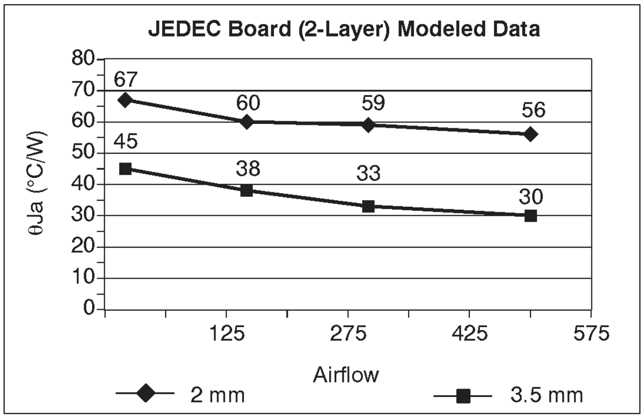


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

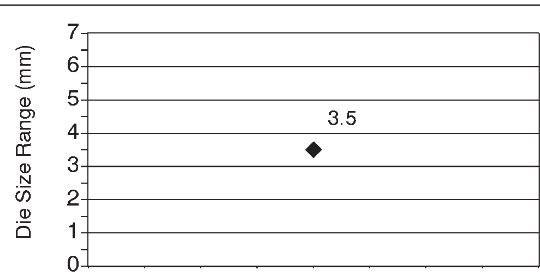
Electrical Characteristics

IN DEVELOPMENT

Thermal Characteristics

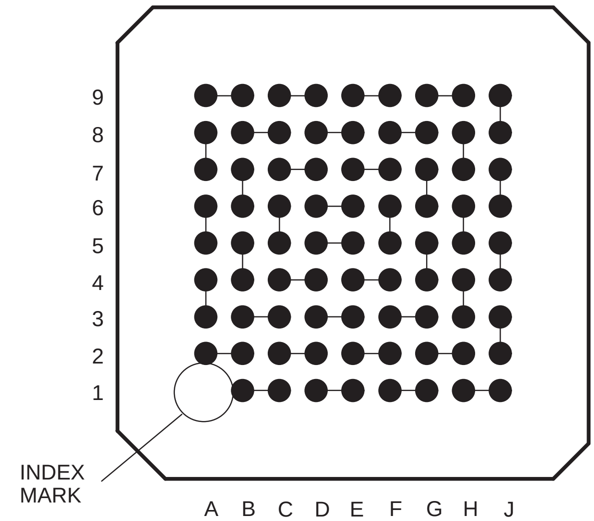


Productization



Part # 4184658
Samples Now
Qualified 4Q99

GJK 80 TOP VIEW **DAISY CHAIN NET LIST**



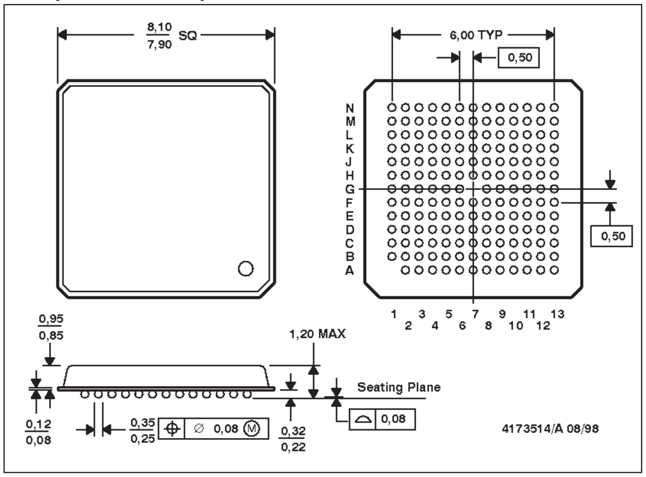
B1–C1	D9–C9	H5–H6	G4–G5
D1–E1	B9–A9	H7–H8	G6–G7
F1–G1	A8–A7	G8–F8	F7–E7
H1–J1	A6–A5	E8–D8	D7–C7
J2–J3	A4–A3	C8–B8	C6–C5
J4–J5	A2–B2	B7–B6	C4–D4
J6–J7	C2–D2	B5–B4	E4–F4
J8–J9	E2–F2	B3–C3	F5–F6
H9–G9	G2–H2	D3–E3	E6–D6
F9–E9	H3–H4	F3–G3	D5–E5

GJK 80 **PIN ASSIGNMENT NET LIST**

PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#
1	C2	21	H3	41	G8	61	B7
2	B1	22	J2	42	H9	62	A8
3	D3	23	G4	43	F7	63	C6
4	E4	24	F5	44	E6	64	D5
5	C1	25	J3	45	G9	65	A7
6	D2	26	H4	46	F8	66	B6
7	E3	27	G5	47	E7	67	C5
8	D1	28	J4	48	F9	68	A6
9	E2	29	H5	49	E8	69	B5
10	F4	30	F6	50	D6	70	D4
11	E1	31	J5	51	E9	71	A5
12	F3	32	G6	52	D7	72	C4
13	F1	33	J6	53	D9	73	A4
14	F2	34	H6	54	D8	74	B4
15	G3	35	G7	55	C7	75	C3
16	G1	36	J7	56	C9	76	A3
17	G2	37	H7	57	C8	77	B3
18	H2	38	H8	58	B8	78	B2
19	H1	39	J8	59	B9	79	A2
20	J1	40	J9	60	A9	80	E5

167GJJ PACKAGE OUTLINE
(8 x 8 mm, 0.5 mm pitch)

GJJ (S-PBGA-N167) **PLASTIC BALL GRID ARRAY**

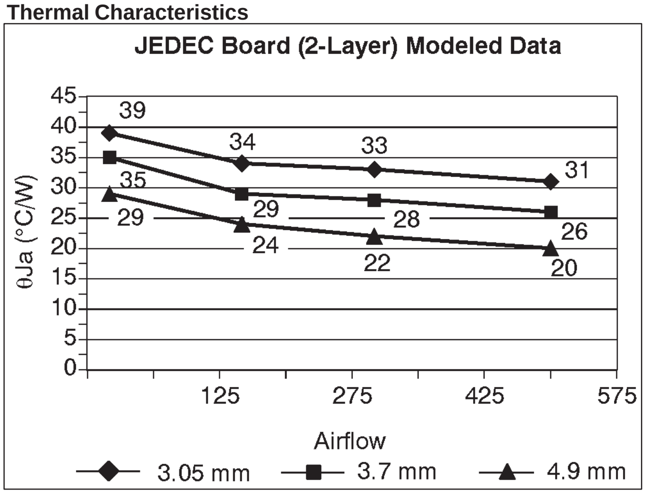


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

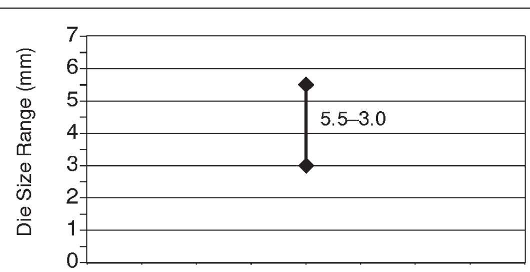
Electrical Characteristics

IN DEVELOPMENT

Thermal Characteristics



Productization



Part # 4184651
Samples Now
Qualified 4Q99

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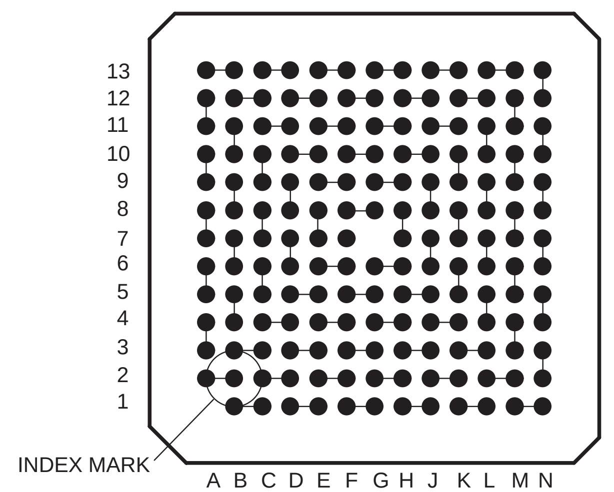
GJJ 167 TOP VIEW **DAISY CHAIN NET LIST**



B1–C1	F3–G3	K5–K6	D8–D9	N10–N11	G13–H13
D1–E1	H3–J3	M5–M6	F8–G8	A11–A12	J13–K13
F1–G1	K3–L3	B6–B7	J8–J9	C11–D11	L13–M13
H1–J1	M3–M4	D6–D7	L8–L9	E11–F11	
K1–L1	B4–B5	E6–F6	N8–N9	G11–H11	
M1–N1	C4–D4	G6–H6	A9–A10	J11–K11	
A2–B2	E4–F4	J6–J7	C9–C10	M11–M12	
C2–D2	G4–H4	L6–L7	E9–F9	B12–C12	
E2–F2	J4–K4	N6–N7	G9–H9	D12–E12	
G2–H2	L4–L5	A7–A8	K9–K10	F12–G12	
J2–K2	N4–N5	C7–C8	M9–M10	H12–J12	
L2–M2	A5–A6	E7–E8	B10–B11	K12–L12	
N2–N3	C5–C6	H7–H8	D10–E10	N12–N13	
A3–A4	D5–E5	K7–K8	F10–G10	A13–B13	
B3–C3	F5–G5	M7–M8	H10–J10	C13–D13	
D3–E3	H5–J5	B8–B9	L10–L11	E13–F13	

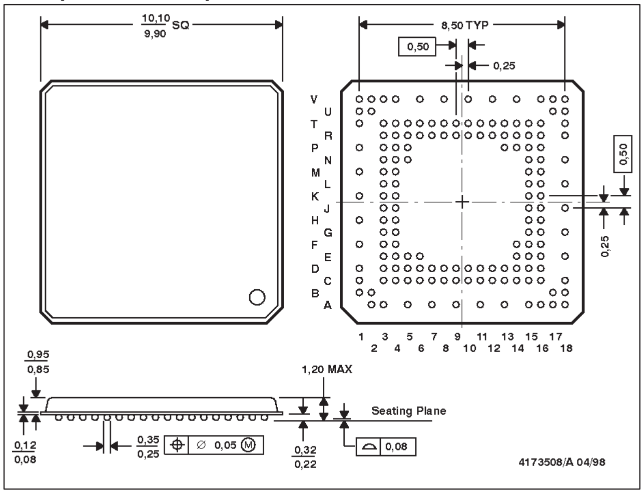
NC – F7

GJJ 167 **PIN ASSIGNMENT NET LIST**

PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#
1	C3	29	J2	57	L6	85	L11	113	E12	141	C8
2	D4	30	H4	58	M6	86	K10	114	F10	142	B8
3	B1	31	K1	59	N6	87	M13	115	D13	143	A8
4	C2	32	J3	60	H6	88	L12	116	E11	144	F8
5	D3	33	K2	61	G6	89	K11	117	D12	145	G8
6	E4	34	H5	62	N7	90	J10	118	F9	146	A7
7	C1	35	L1	63	M7	91	L13	119	C13	147	B7
8	D2	36	J4	64	L7	92	K12	120	E10	148	C7
9	E3	37	L2	65	K7	93	J11	121	C12	149	D7
10	D1	38	M1	66	N8	94	K13	122	B13	150	A6
11	F5	39	K3	67	M8	95	H9	123	D11	151	B6
12	E2	40	J5	68	J7	96	J12	124	E9	152	E7
13	F4	41	M2	69	N9	97	H10	125	B12	153	A5
14	E1	42	N1	70	L8	98	J13	126	A13	154	C6
15	F3	43	L3	71	M9	99	H11	127	C11	155	B5
16	F2	44	K4	72	K8	100	H12	128	D10	156	D6
17	F1	45	N2	73	N10	101	H13	129	A12	157	A4
18	F6	46	M3	74	L9	102	H8	130	B11	158	C5
19	F7	47	L4	75	M10	103	H7	131	C10	159	B4
20	G1	48	K5	76	J8	104	G13	132	D9	160	E6
21	G2	49	N3	77	N11	105	G12	133	A11	161	A3
22	G3	50	M4	78	K9	106	G11	134	B10	162	D5
23	G4	51	L5	79	M11	107	G10	135	C9	163	B3
24	H1	52	N4	80	N12	108	F13	136	A10	164	A2
25	H2	53	J6	81	L10	109	F12	137	E8	165	C4
26	G5	54	M5	82	J9	110	G9	138	B9	166	E5
27	J1	55	K6	83	M12	111	E13	139	D8	167	B2
28	H3	56	N5	84	N13	112	F11	140	A9		

151GHZ PACKAGE OUTLINE (10 x 10 mm, 0.5 mm pitch)

GHZ (S-PBGA-N151) PLASTIC BALL GRID ARRAY

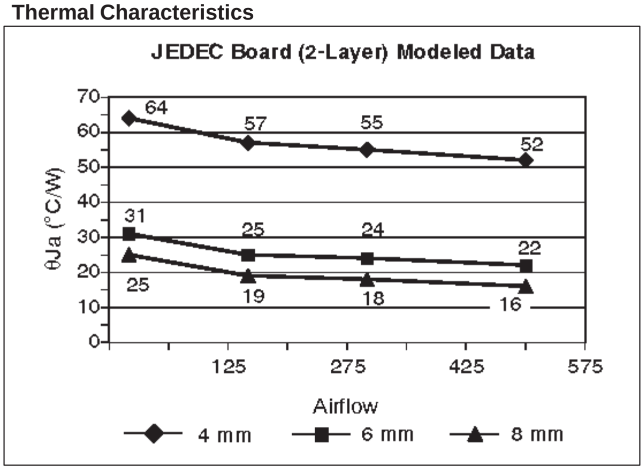


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

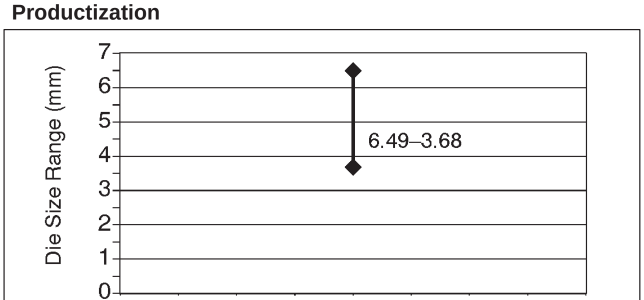
Electrical Characteristics

IN DEVELOPMENT

Thermal Characteristics



Productization



Part #	4166679
Samples	Now
Qualified	4Q99

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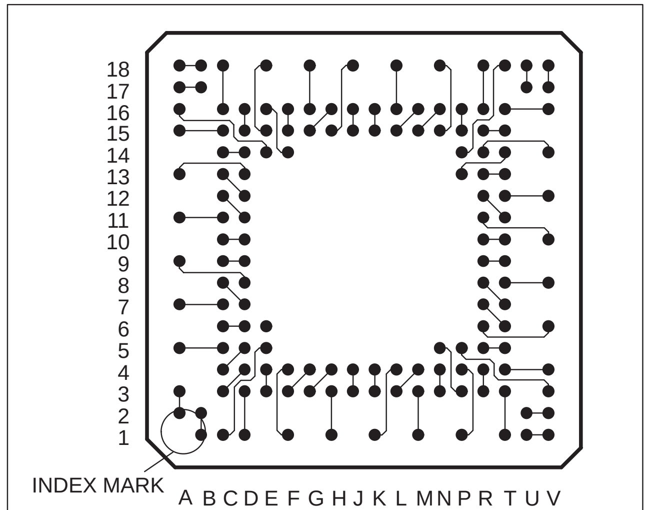
GHZ 151 TOP VIEW — DAISY CHAIN NET LIST



B1–B2	R3–R4	R13–T13	H15–J18	A11–C11
C1–E5	T1–T3	P13–T14	G15–H16	C10–D10
D1–D3	U1–V1	R14–V14	G16–G18	C9–D9
E3–E4	U2–V2	R15–T15	F15–F16	A9–D8
F1–F4	P5–V3	T16–V16	E16–F14	C8–D7
F3–G4	T4–V4	V17–V18	E15–E18	A7–C7
G3–H4	R5–T5	U17–U18	D15–D16	C6–D6
H1–H3	R6–V6	P14–T18	C16–C18	A5–C5
J3–J4	R7–T6	R16–R18	A18–B18	C4–D5
K3–K4	R8–T7	P15–P16	A17–B17	C3–D4
K1–L4	T8–V8	N15–N18	A16–E14	A2–A3
L3–M4	R9–T9	M15–N16	A15–C15	
M1–M3	R10–T10	L15–M16	C14–D14	
N3–N4	R11–V10	L16–L18	A13–D13	
N5–P3	R12–T11	K15–K16	C13–D12	
P1–P4	T12–V12	J15–J16	C12–D11	

NC – E6

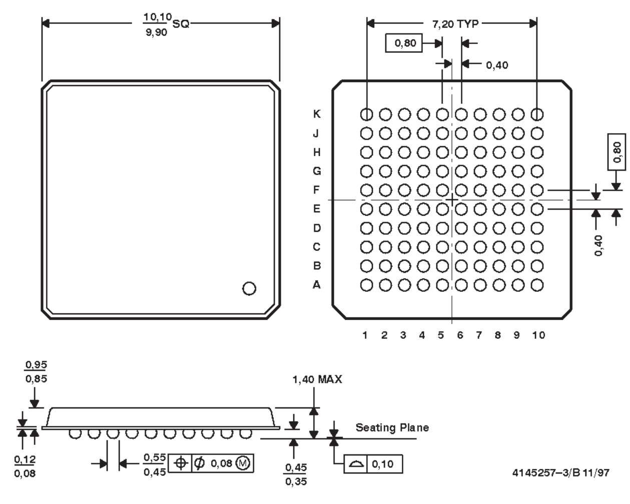
GHZ 151 PIN ASSIGNMENT NET LIST

PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#
1	B2	31	P1	61	T11	91	L18	121	D14
2	B1	32	P4	62	R12	92	L16	122	C14
3	C1	33	R3	63	T12	93	K15	123	D13
4	E5	34	R4	64	V12	94	K16	124	A13
5	D1	35	T3	65	R13	95	J15	125	C13
6	D3	36	T1	66	T13	96	J16	126	D12
7	E4	37	U1	67	P13	97	J18	127	C12
8	E3	38	V1	68	T14	98	H15	128	D11
9	F4	39	U2	69	V14	99	H16	129	A11
10	F1	40	V2	70	R14	100	G15	130	C11
11	F3	41	V3	71	T15	101	G16	131	D10
12	G4	42	P5	72	R15	102	G18	132	C10
13	G3	43	V4	73	T16	103	F15	133	D9
14	H4	44	T4	74	V16	104	F16	134	C9
15	H1	45	R5	75	V17	105	F14	135	A9
16	H3	46	T5	76	V18	106	E16	136	D8
17	J4	47	R6	77	U17	107	E18	137	C8
18	J3	48	V6	78	U18	108	E15	138	D7
19	K4	49	T6	79	T18	109	D16	139	C7
20	K3	50	R7	80	P14	110	D15	140	A7
21	K1	51	T7	81	R18	111	C16	141	D6
22	L4	52	R8	82	R16	112	C18	142	C6
23	L3	53	V8	83	P15	113	B18	143	E6
24	M4	54	T8	84	P16	114	A18	144	C5
25	M3	55	R9	85	N15	115	B17	145	A5
26	M1	56	T9	86	N18	116	A17	146	D5
27	N4	57	R10	87	N16	117	A16	147	C4
28	N3	58	T10	88	M15	118	E14	148	D4
29	N5	59	V10	89	M16	119	A15	149	C3
30	P3	60	R11	90	L15	120	C15	150	A3
								151	A2

Appendix B Package Data Sheets

100GGM PACKAGE OUTLINE
(10 x 10 mm, 0.8 mm pitch)

GGM (S-PBGA-N100) **PLASTIC BALL GRID ARRAY**

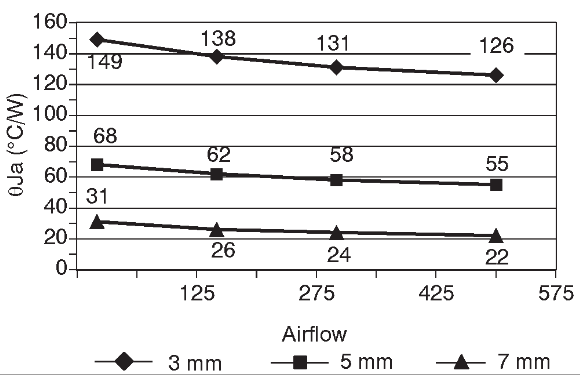


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

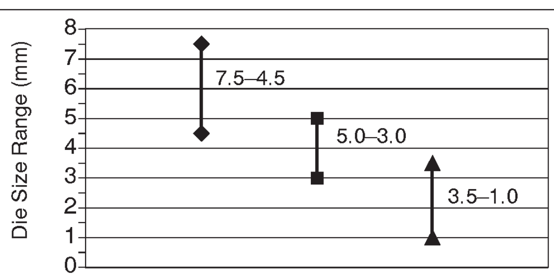
Electrical Characteristics

	R (Ω)	L (nH)	C (pF)
Min.	0.071	1.999	0.296
Mean	0.076	2.425	0.440
Max.	0.081	2.957	0.589

Thermal Characteristics



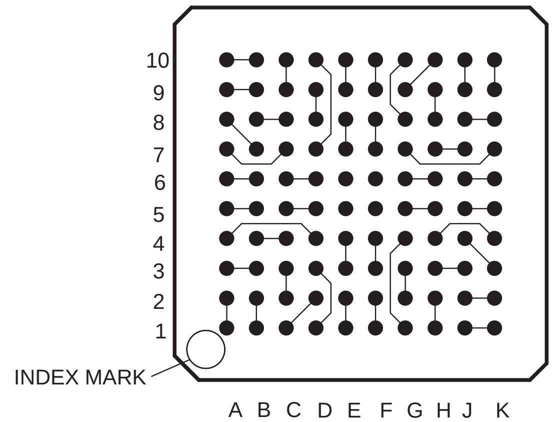
Productization



Part #	4122751	4192776	4122752
Samples	Now	Now	Now
Qualified	Complete	Complete	Complete

MicroStar BGA is a trademark of Texas Instruments Incorporated.

GGM 100 TOP VIEW **DAISY CHAIN NET LIST**



B2–B1	J2–K2	J9–J10	B9–A9
C2–C3	J3–H3	H9–H8	B8–C8
C1–D2	K3–J4	H10–G9	A8–B7
D1–D3	K4–H4	G10–G8	A7–C7
E1–E2	K5–J5	F10–F9	A6–B6
E3–E4	H5–G5	F8–F7	C6–D6
F1–F2	K6–J6	E10–E9	A5–B5
F3–F4	H6–G6	E8–E7	C5–D5
G4–G1	G7–K7	D7–D10	D4–A4
G2–G3	J7–H7	D9–D8	B4–C4
H1–H2	K8–J8	C10–C9	A3–B3
J1–K1	K9–K10	B10–A10	A2–A1

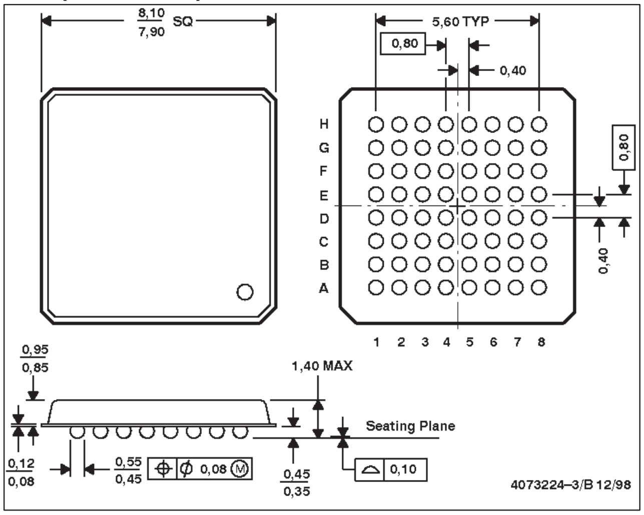
NC – E5,E6,F5,F6

GGM 100 **PIN ASSIGNMENT NET LIST**

PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#
1	B2	26	J2	51	J9	76	B9
2	B1	27	K2	52	J10	77	A9
3	C2	28	J3	53	H9	78	B8
4	C3	29	H3	54	H8	79	C8
5	C1	30	K3	55	H10	80	A8
6	D2	31	J4	56	G9	81	B7
7	D1	32	K4	57	G10	82	A7
8	D3	33	H4	58	G8	83	C7
9	E1	34	K5	59	F10	84	A6
10	E2	35	J5	60	F9	85	B6
11	E3	36	H5	61	F8	86	C6
12	E4	37	G5	62	F7	87	D6
13	E5	38	F5	63	F6	88	E6
14	F1	39	K6	64	E10	89	A5
15	F2	40	J6	65	E9	90	B5
16	F3	41	H6	66	E8	91	C5
17	F4	42	G6	67	E7	92	D5
18	G4	43	G7	68	D7	93	D4
19	G1	44	K7	69	D10	94	A4
20	G2	45	J7	70	D9	95	B4
21	G3	46	H7	71	D8	96	C4
22	H1	47	K8	72	C10	97	A3
23	H2	48	J8	73	C9	98	B3
24	J1	49	K9	74	B10	99	A2
25	K1	50	K10	75	A10	100	A1

64GGV PACKAGE OUTLINE
(8 x 8 mm, 0.8 mm pitch)

GGV (S-PBGA-N64) **PLASTIC BALL GRID ARRAY**



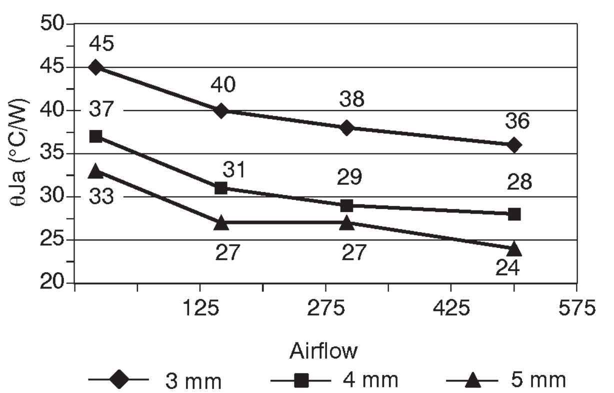
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

Electrical Characteristics

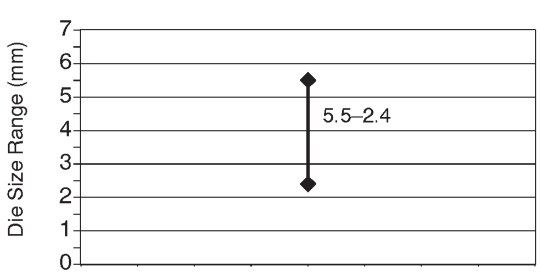
	R (Ω)	L (nH)	C (pF)
Min.	0.071	2.002	0.273
Mean	0.076	2.544	0.380
Max.	0.082	3.443	0.580

Thermal Characteristics

JEDEC Board (2-Layer) Modeled Data



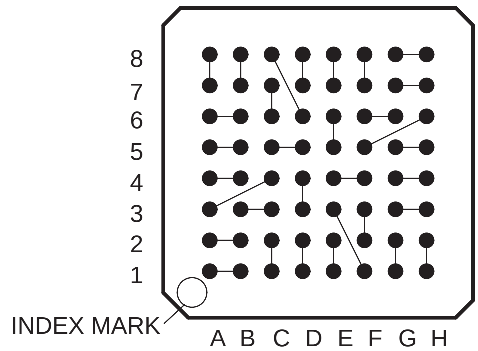
Productization



Part #	4155576
Samples	Now
Qualified	Complete

MicroStar BGA is a trademark of Texas Instruments Incorporated.

GGV 64 TOP VIEW **DAISY CHAIN NET LIST**



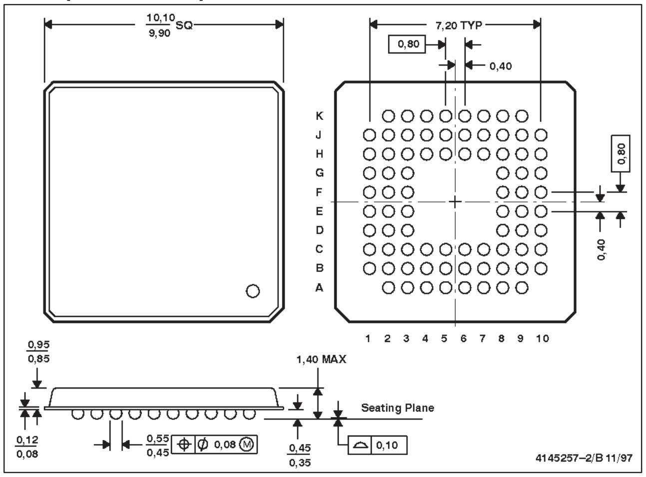
A1–B1	H8–G8
C2–C1	F7–F8
D4–D3	E5–E6
D1–D2	E8–E7
E2–E1	D7–D8
E3–F1	D6–C8
F2–F3	C7–C6
G1–G2	B8–B7
H1–H2	A8–A7
G3–H3	B6–A6
E4–F4	D5–C5
H4–G4	A5–B5
G5–H5	B4–A4
F5–H6	C4–A3
G6–F6	B3–C3
H7–G7	A2–B2

GGV 64 **PIN ASSIGNMENT NET LIST**

PIN# BALL#	PIN# BALL#	PIN# BALL#	PIN# BALL#
1 – A1	17 – H1	33 – H8	49 – A8
2 – B1	18 – H2	34 – G8	50 – A7
3 – C2	19 – G3	35 – F7	51 – B6
4 – C1	20 – H3	36 – F8	52 – A6
5 – D4	21 – E4	37 – E5	53 – D5
6 – D3	22 – F4	38 – E6	54 – C5
7 – D1	23 – H4	39 – E8	55 – A5
8 – D2	24 – G4	40 – E7	56 – B5
9 – E2	25 – G5	41 – D7	57 – B4
10 – E1	26 – H5	42 – D8	58 – A4
11 – E3	27 – F5	43 – D6	59 – C4
12 – F1	28 – H6	44 – C8	60 – A3
13 – F2	29 – G6	45 – C7	61 – B3
14 – F3	30 – F6	46 – C6	62 – C3
15 – G1	31 – H7	47 – B8	63 – A2
16 – G2	32 – G7	48 – B7	64 – B2

80GGM PACKAGE OUTLINE
(10 x 10 mm, 0.8 mm pitch)

GGM (S-PBGA-N80) **PLASTIC BALL GRID ARRAY**

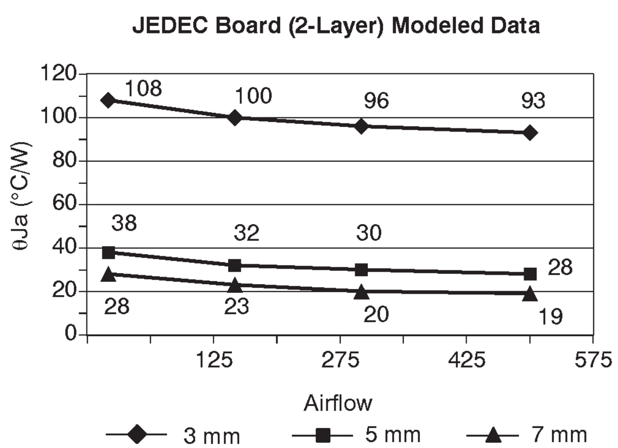


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

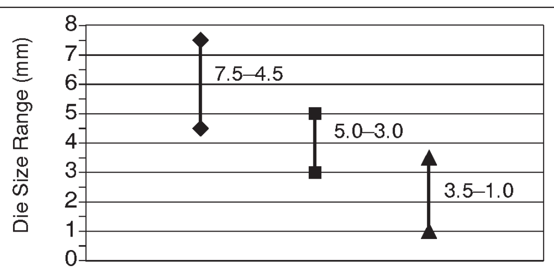
Electrical Characteristics

	R (Ω)	L (nH)	C (pF)
Min.	0.054	1.487	0.215
Mean	0.062	1.920	0.315
Max.	0.074	2.659	0.428

Thermal Characteristics



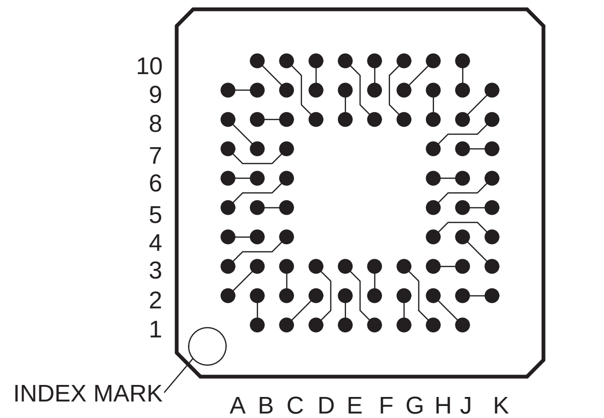
Productization



Part #	4122751	4192776	4122752
Samples	Now	Now	Now
Qualified	Complete	Complete	Complete

MicroStar BGA is a trademark of Texas Instruments Incorporated.

GGM 80 TOP VIEW **DAISY CHAIN NET LIST**



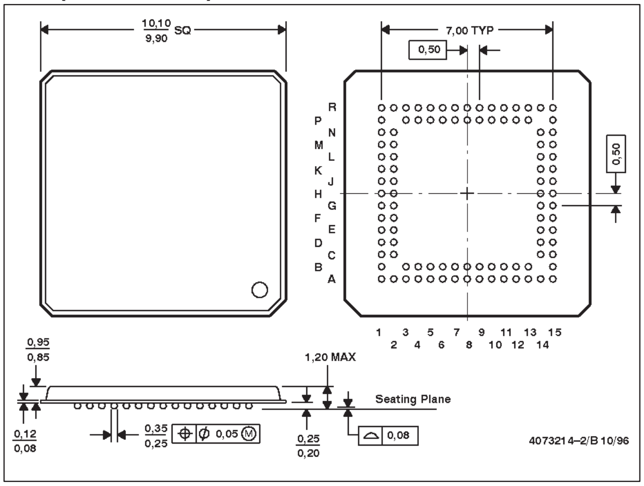
B2–B1	J2–K2	J9–J10	B9–A9
C2–C3	J3–H3	H9–H8	B8–C8
C1–D2	K3–J4	H10–G9	A8–B7
D1–D3	K4–H4	G10–G8	A7–C7
E1–E2	K5–J5	F10–F9	A6–B6
E3–F1	H5–K6	F8–E10	C6–A5
F2–F3	J6–H6	E9–E8	B5–C5
G1–G2	K7–J7	D10–D9	A4–B4
G3–H1	H7–K8	D8–C10	C4–A3
H2–J1	J8–K9	C9–B10	B3–A2

GGM 80 **PIN ASSIGNMENT NET LIST**

PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#
1	B2	21	J2	41	J9	61	B9
2	B1	22	K2	42	J10	62	A9
3	C2	23	J3	43	H9	63	B8
4	C3	24	H3	44	H8	64	C8
5	C1	25	K3	45	H10	65	A8
6	D2	26	J4	46	G9	66	B7
7	D1	27	K4	47	G10	67	A7
8	D3	28	H4	48	G8	68	C7
9	E1	29	K5	49	F10	69	A6
10	E2	30	J5	50	F9	70	B6
11	E3	31	H5	51	F8	71	C6
12	F1	32	K6	52	E10	72	A5
13	F2	33	J6	53	E9	73	B5
14	F3	34	H6	54	E8	74	C5
15	G1	35	K7	55	D10	75	A4
16	G2	36	J7	56	D9	76	B4
17	G3	37	H7	57	D8	77	C4
18	H1	38	K8	58	C10	78	A3
19	H2	39	J8	59	C9	79	B3
20	J1	40	K9	60	B10	80	A2

100GGF PACKAGE OUTLINE (10 x 10 mm, 0.5 mm pitch)

GGF (S-PBGA-N100) **PLASTIC BALL GRID ARRAY**



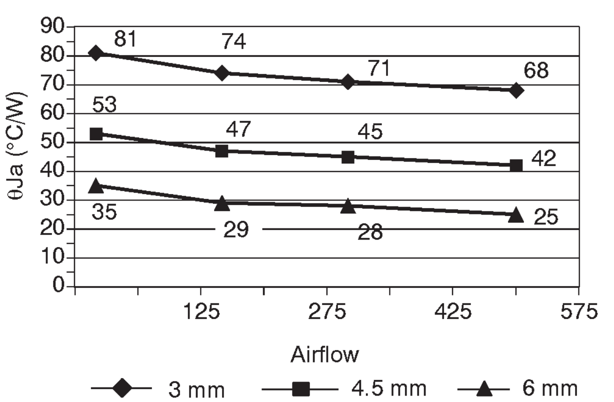
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

Electrical Characteristics

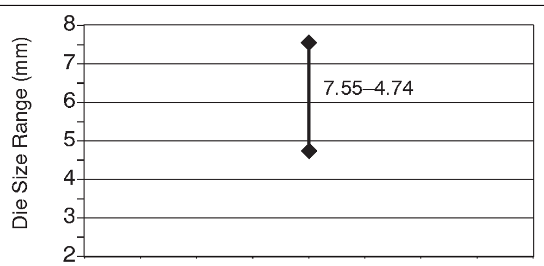
	R (Ω)	L (nH)	C (pF)
Min.	0.011	0.676	0.102
Mean	0.022	1.026	0.172
Max.	0.035	1.606	0.339

Thermal Characteristics

JEDEC Board (2-Layer) Modeled Data



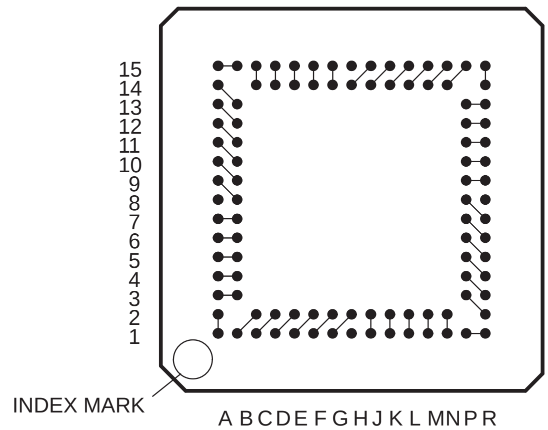
Productization



Part #	4151542
Samples	Now
Qualified	Complete

MicroStar BGA is a trademark of Texas Instruments Incorporated.

GGF 100 TOP VIEW **DAISY CHAIN NET LIST**



B1–C2	R2–P3	P15–N14	A14–B13
C1–D2	R3–P4	N15–M14	A13–B12
D1–E2	R4–P5	M15–L14	A12–B11
E1–F2	R5–P6	L15–K14	A11–B10
F1–G2	R6–P7	K15–J14	A10–B9
G1–H2	R7–P8	J15–H14	A9–B8
J1–J2	R9–P9	G15–G14	A7–B7
K1–K2	R10–P10	F15–F14	A6–B6
L1–L2	R11–P11	E15–E14	A5–B5
M1–M2	R12–P12	D15–D14	A4–B4
N1–N2	R13–P13	C15–C14	A3–B3
P1–R1	R14–R15	B15–A15	A2–A1

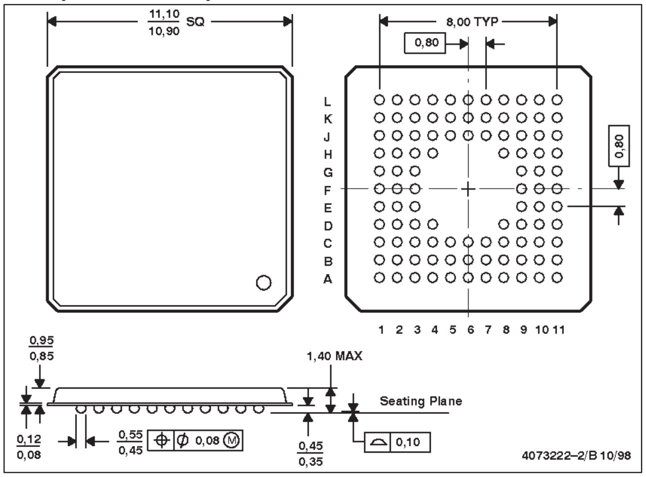
NC— H1, R8, H15, A8

GGF 100 **PIN ASSIGNMENT NET LIST**

PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#
1	B1	26	R2	51	P15	76	A14
2	C2	27	P3	52	N14	77	B13
3	C1	28	R3	53	N15	78	A13
4	D2	29	P4	54	M14	79	B12
5	D1	30	R4	55	M15	80	A12
6	E2	31	P5	56	L14	81	B11
7	E1	32	R5	57	L15	82	A11
8	F2	33	P6	58	K14	83	B10
9	F1	34	R6	59	K15	84	A10
10	G2	35	P7	60	J14	85	B9
11	G1	36	R7	61	J15	86	A9
12	H2	37	P8	62	H14	87	B8
13	H1	38	R8	63	H15	88	A8
14	J1	39	R9	64	G15	89	A7
15	J2	40	P9	65	G14	90	B7
16	K1	41	R10	66	F15	91	A6
17	K2	42	P10	67	F14	92	B6
18	L1	43	R11	68	E15	93	A5
19	L2	44	P11	69	E14	94	B5
20	M1	45	R12	70	D15	95	A4
21	M2	46	P12	71	D14	96	B4
22	N1	47	R13	72	C15	97	A3
23	N2	48	P13	73	C14	98	B3
24	P1	49	R14	74	B15	99	A2
25	R1	50	R15	75	A15	100	A1

100GGT PACKAGE OUTLINE (11 x 11 mm, 0.8 mm pitch)

GGT (S-PBGA-N100) PLASTIC BALL GRID ARRAY

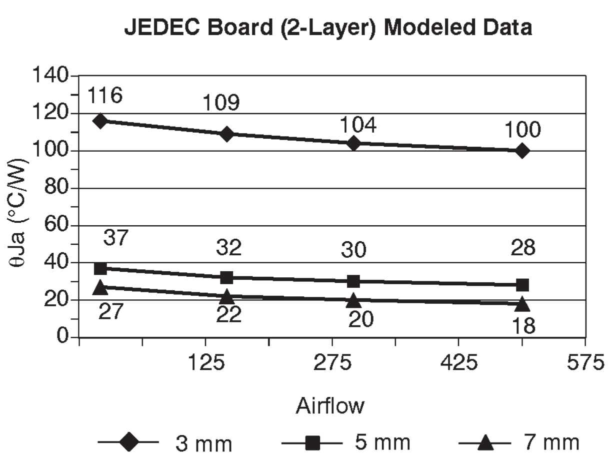


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

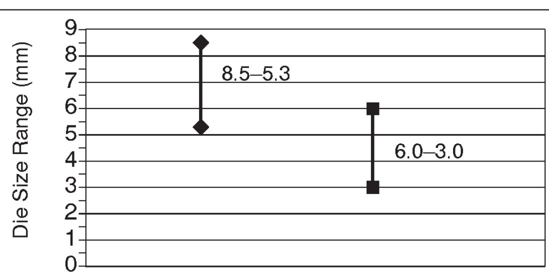
Electrical Characteristics

	R (Ω)	L (nH)	C (pF)
Min.	0.072	2.200	0.254
Mean	0.077	2.636	0.398
Max.	0.086	3.633	0.582

Thermal Characteristics



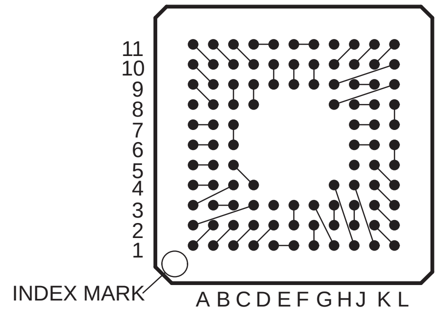
Productization



Part #	4122770	4109516
Samples Qualified	Now Complete	Now Complete

MicroStar BGA is a trademark of Texas Instruments Incorporated.

GGT 100 TOP VIEW DAISY CHAIN NET LIST



A1 — B2	L1 — K2	L11 — K10
B1 — C2	L2 — K3	K11 — J10
C1 — D2	L3 — K4	J11 — H10
D1 — E2	L4 — K5	G9 — G10
F3 — F2	J6 — K6	F9 — F10
E1 — F1	L5 — L6	G11 — F11
G1 — G2	L7 — L8	E11 — D11
G3 — H1	K7 — J7	E10 — E9
H2 — H3	K8 — J8	D10 — C11
H4 — J1	L9 — H8	D9 — D8
J2 — J3	K9 — J9	C10 — B11
K1 — J4	L10 — H9	C9 — C8

NC – E3,J5,H11,A8

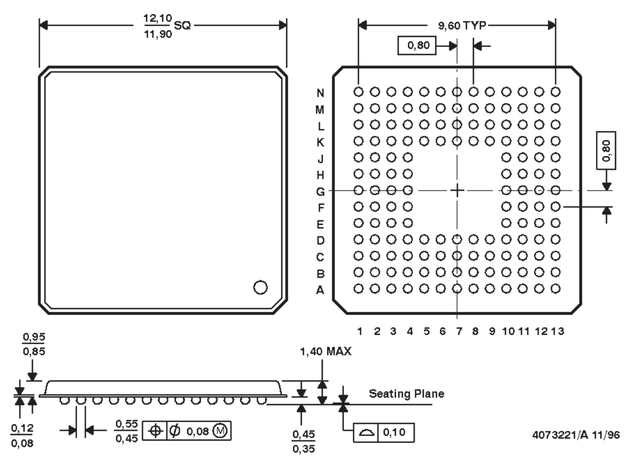
GGT 100 PIN ASSIGNMENT NET LIST

PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#
1	A1	26	L1	51	L11	76	A11
2	B2	27	K2	52	K10	77	B10
3	B1	28	L2	53	K11	78	A10
4	C2	29	K3	54	J10	79	B9
5	C1	30	L3	55	J11	80	A9
6	D2	31	K4	56	H10	81	B8
7	E3	32	J5	57	H11	82	A8
8	D1	33	L4	58	G9	83	B7
9	E2	34	K5	59	G10	84	A7
10	F3	35	J6	60	F9	85	C7
11	F2	36	K6	61	F10	86	C6
12	E1	37	L5	62	G11	87	B6
13	F1	38	L6	63	F11	88	A6
14	G1	39	L7	64	E11	89	B5
15	G2	40	L8	65	D11	90	A5
16	G3	41	K7	66	E10	91	C5
17	H1	42	J7	67	E9	92	D4
18	H2	43	K8	68	D10	93	A4
19	H3	44	J8	69	C11	94	B4
20	H4	45	L9	70	D9	95	C4
21	J1	46	H8	71	D8	96	A3
22	J2	47	K9	72	C10	97	B3
23	J3	48	J9	73	B11	98	C3
24	K1	49	L10	74	C9	99	A2
25	J4	50	H9	75	C8	100	D3

Appendix B Package Data Sheets

144GGU PACKAGE OUTLINE (12 x 12 mm, 0.8 mm pitch)

GGU (S-PBGA-N144) PLASTIC BALL GRID ARRAY

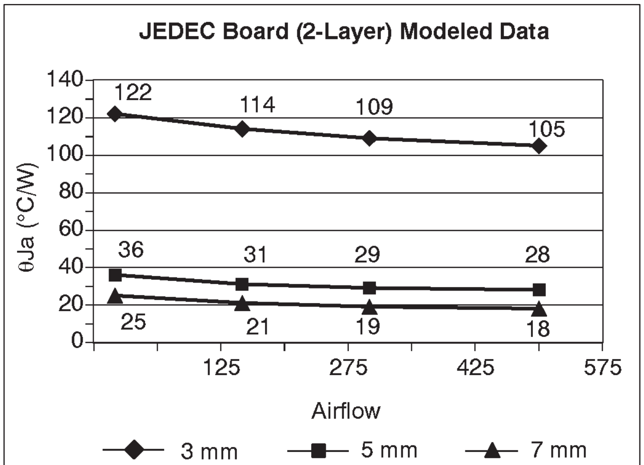


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

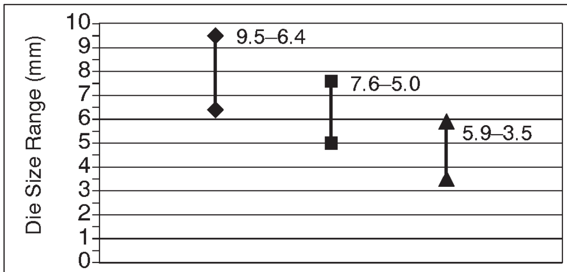
Electrical Characteristics

	R (Ω)	L (nH)	C (pF)
Min.	0.052	1.438	0.215
Mean	0.055	1.958	0.305
Max.	0.062	3.095	0.563

Thermal Characteristics



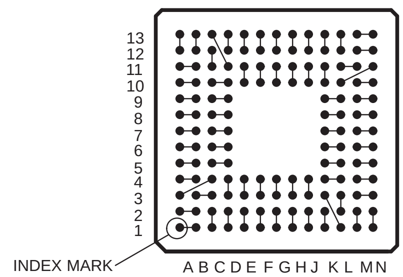
Productization



Part #	4503050	4166637	4503063
Samples	Now	Now	Now
Qualified	Complete	Complete	Complete

MicroStar BGA is a trademark of Texas Instruments Incorporated.

GGU 144 TOP VIEW DAISY CHAIN NET LIST



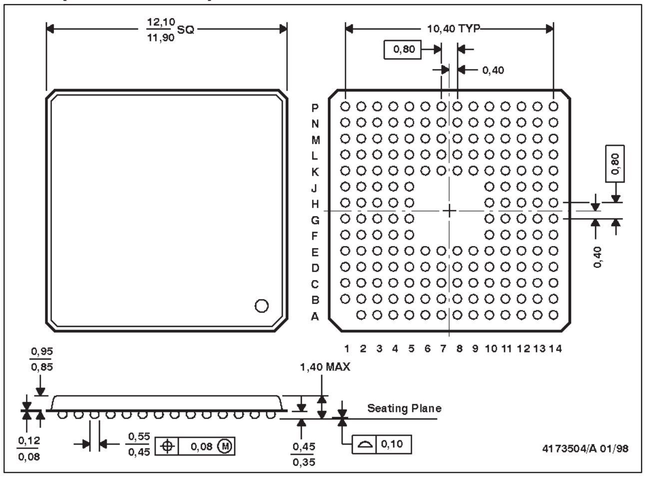
A1–B1	N1–N2	N13–M13	A13–A12
C2–C1	M3–N3	L12–L13	B11–A11
D4–D3	K4–L4	K10–K11	D10–C10
D2–D1	M4–N4	K12–K13	B10–A10
E4–E3	K5–L5	J10–J11	D9–C9
E2–E1	M5–N5	J12–J13	B9–A9
F4–F3	K6–L6	H10–H11	D8–C8
F2–F1	M6–N6	H12–H13	B8–A8
G2–G1	M7–N7	G12–G13	B7–A7
G3–G4	L7–K7	G11–G10	C7–D7
H1–H2	N8–M8	F13–F12	A6–B6
H3–H4	L8–K8	F11–F10	C6–D6
J1–J2	N9–M9	E13–E12	A5–B5
J3–J4	L9–K9	E11–E10	C5–D5
K1–K2	N10–M10	D13–D12	A4–B4
K3–L1	L10–N11	D11–C13	C4–A3
L2–L3	M11–L11	C12–C11	B3–C3
M1–M2	N12–M12	B13–B12	A2–B2

GGU 144 PIN ASSIGNMENT NET LIST

PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#
1	A1	37	N1	73	N13	109	A13
2	B1	38	N2	74	M13	110	A12
3	C2	39	M3	75	L12	111	B11
4	C1	40	N3	76	L13	112	A11
5	D4	41	K4	77	K10	113	D10
6	D3	42	L4	78	K11	114	C10
7	D2	43	M4	79	K12	115	B10
8	D1	44	N4	80	K13	116	A10
9	E4	45	K5	81	J10	117	D9
10	E3	46	L5	82	J11	118	C9
11	E2	47	M5	83	J12	119	B9
12	E1	48	N5	84	J13	120	A9
13	F4	49	K6	85	H10	121	D8
14	F3	50	L6	86	H11	122	C8
15	F2	51	M6	87	H12	123	B8
16	F1	52	N6	88	H13	124	A8
17	G2	53	M7	89	G12	125	B7
18	G1	54	N7	90	G13	126	A7
19	G3	55	L7	91	G11	127	C7
20	G4	56	K7	92	G10	128	D7
21	H1	57	N8	93	F13	129	A6
22	H2	58	M8	94	F12	130	B6
23	H3	59	L8	95	F11	131	C6
24	H4	60	K8	96	F10	132	D6
25	J1	61	N9	97	E13	133	A5
26	J2	62	M9	98	E12	134	B5
27	J3	63	L9	99	E11	135	C5
28	J4	64	K9	100	E10	136	D5
29	K1	65	N10	101	D13	137	A4
30	K2	66	M10	102	D12	138	B4
31	K3	67	L10	103	D11	139	C4
32	L1	68	N11	104	C13	140	A3
33	L2	69	M11	105	C12	141	B3
34	L3	70	L11	106	C11	142	C3
35	M1	71	N12	107	B13	143	A2
36	M2	72	M12	108	B12	144	B2

179GHH PACKAGE OUTLINE (12 x 12 mm, 0.8 mm pitch)

GHH (S-PBGA-N179) **PLASTIC BALL GRID ARRAY**



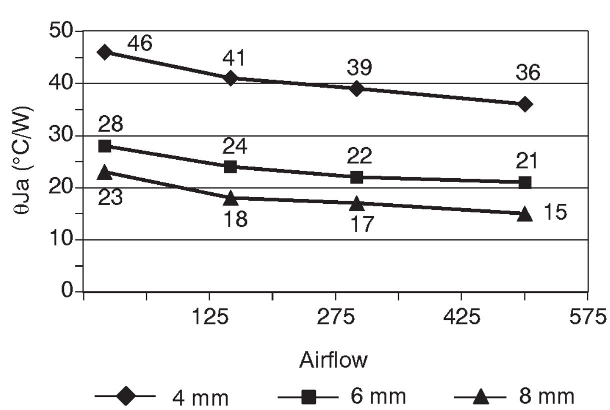
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

Electrical Characteristics

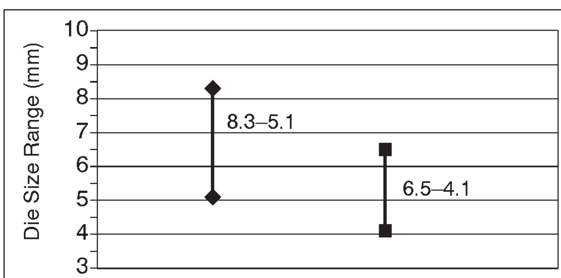
IN DEVELOPMENT

Thermal Characteristics

JEDEC Board (2-Layer) Modeled Data



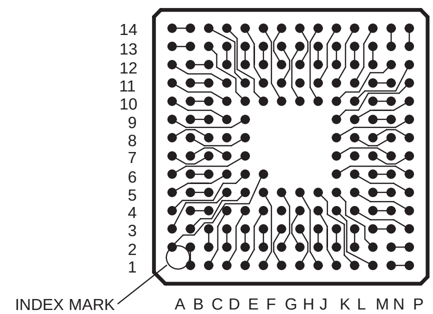
Productization



Part #	4503056	4109523
Samples	Now	Now
Qualified	Complete	Complete

MicroStar BGA is a trademark of Texas Instruments Incorporated.

GHH 179 TOP VIEW **DAISY CHAIN NET LIST**



B2–B1	H3–H1	N2–P2	M8–P8	N13–N14	G12–G14	B13–A13	C7–A7
C3–C2	H2–H4	M3–N3	N8–L8	M12–M13	G13–G11	C12–B12	B7–D7
C1–D4	H5–J1	P3–L4	K8–P9	M14–L11	G10–F14	A12–D11	E7–A6
D3–D2	J2–J3	M4–N4	N9–M9	L12–L13	F13–F12	C11–B11	B6–C6
D1–E4	J4–K1	P4–L5	L9–P10	L14–K11	F11–E14	A11–D10	D6–A5
E3–E2	K2–K3	M5–N5	N10–M10	K12–K13	E13–E12	C10–B10	B5–C5
E1–F4	J5–L1	P5–L6	K9–P11	K14–J11	F10–D14	A10–D9	E6–A4
F3–F2	L2–L3	M6–N6	N11–M11	J12–J13	D13–D12	C9–B9	B4–C4
F1–F5	K4–M1	P6–K6	L10–P12	J14–J10	E11–C14	A9–E9	D5–A3
G5–G2	M2–K5	K7–N7	N12–K10	H10–H13	C13–E10	E8–B8	B3–E5
G1–G3	N1–P1	P7–M7	P13–P14	H14–H12	B14–A14	A8–C8	F6–A2

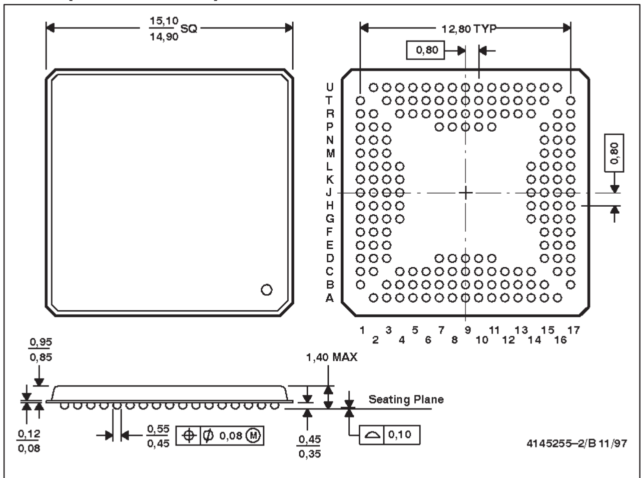
NC —— D8,G4,H11,L7,A2

GHH 179 **PIN ASSIGNMENT NET LIST**

PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#
1	B2	31	J3	61	N6	91	N13	121	F12	151	B9
2	B1	32	J4	62	P6	92	N14	122	F11	152	A9
3	C3	33	K1	63	K6	93	M12	123	E14	153	E9
4	C2	34	K2	64	K7	94	M13	124	E13	154	E8
5	C1	35	K3	65	N7	95	M14	125	E12	155	B8
6	D4	36	J5	66	P7	96	L11	126	F10	156	A8
7	D3	37	L1	67	M7	97	L12	127	D14	157	C8
8	D2	38	L2	68	L7	98	L13	128	D13	158	D8
9	D1	39	L3	69	M8	99	L14	129	D12	159	C7
10	E4	40	K4	70	P8	100	K11	130	E11	160	A7
11	E3	41	M1	71	N8	101	K12	131	C14	161	B7
12	E2	42	M2	72	L8	102	K13	132	C13	162	D7
13	E1	43	K5	73	K8	103	K14	133	E10	163	E7
14	F4	44	N1	74	P9	104	J11	134	B14	164	A6
15	F3	45	P1	75	N9	105	J12	135	A14	165	B6
16	F2	46	N2	76	M9	106	J13	136	B13	166	C6
17	F1	47	P2	77	L9	107	J14	137	A13	167	D6
18	F5	48	M3	78	P10	108	J10	138	C12	168	A5
19	G5	49	N3	79	N10	109	H10	139	B12	169	B5
20	G2	50	P3	80	M10	110	H13	140	A12	170	C5
21	G1	51	L4	81	K9	111	H14	141	D11	171	E6
22	G3	52	M4	82	P11	112	H12	142	C11	172	A4
23	G4	53	N4	83	N11	113	H11	143	B11	173	B4
24	H3	54	P4	84	M11	114	G12	144	A11	174	C4
25	H1	55	L5	85	L10	115	G14	145	D10	175	D5
26	H2	56	M5	86	P12	116	G13	146	C10	176	A3
27	H4	57	N5	87	N12	117	G11	147	B10	177	B3
28	H5	58	P5	88	K10	118	G10	148	A10	178	E5
29	J1	59	L6	89	P13	119	F14	149	D9	(179	F6 (ID ball))
30	J2	60	M6	90	P14	120	F13	150	C9	180	A2

176GGW PACKAGE OUTLINE (15 x 15 mm, 0.8 mm pitch)

GGW (S-PBGA-N176) **PLASTIC BALL GRID ARRAY**



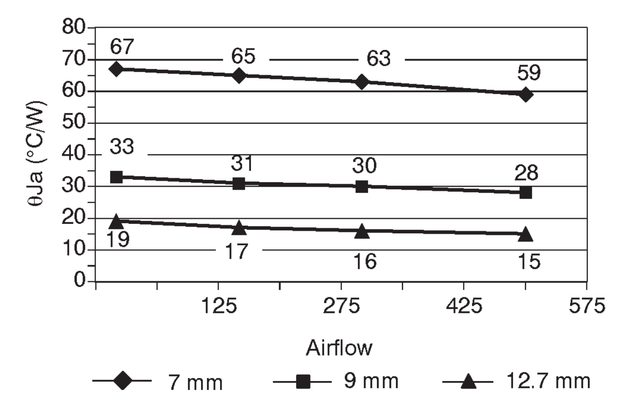
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

Electrical Characteristics

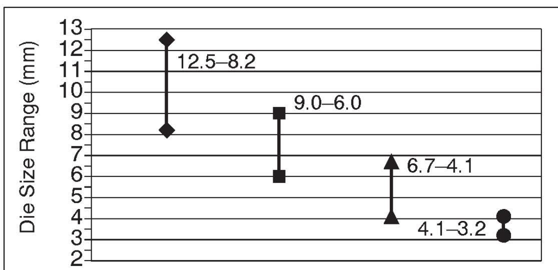
	R (Ω)	L (nH)	C (pF)
Min.	0.075	1.595	0.204
Mean	0.083	2.417	0.298
Max.	0.099	3.284	0.425

Thermal Characteristics

JEDEC Board (2-Layer) Modeled Data



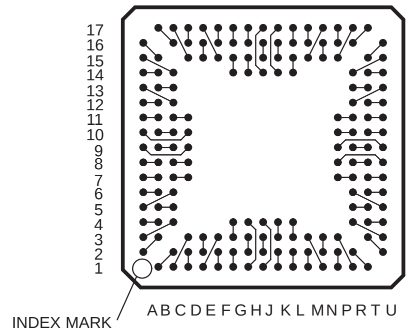
Productization



Part #	4122767	4166632	4166633	4117443
Samples	Now	Now	Now	Now
Qualified	Complete	Complete	Complete	Complete

MicroStar BGA is a trademark of Texas Instruments Incorporated.

GGW 176 TOP VIEW **DAISY CHAIN NET LIST**



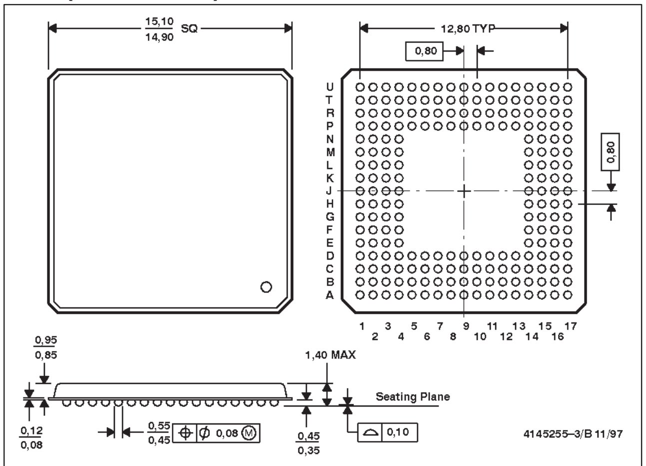
B1–C2	U2–T3	T17–R16	A16–B15
C1–D3	U3–R4	R17–P15	A15–C14
D2–D1	T4–U4	P16–P17	B14–A14
E3–E2	R5–T5	N15–N16	C13–B13
E1–F3	U5–R6	N17–M15	A13–C12
F2–F1	T6–U6	M16–M17	B12–A12
G4–G3	P7–R7	L14–L15	D11–C11
G2–G1	T7–U7	L16–L17	B11–A11
H1–H4	U8–P8	K17–K14	A10–D10
H3–H2	R8–T8	K15–K16	C10–B10
J1–J4	U9–P9	J17–J14	A9–D9
J3–J2	R9–T9	J15–J16	C9–B9
K1–K2	U10–T10	H17–H16	A8–B8
K3–K4	R10–P10	H15–H14	C8–D8
L1–L2	U11–T11	G17–G16	A7–B7
L3–L4	R11–P11	G15–G14	C7–D7
M1–M2	U12–T12	F17–F16	A6–B6
M3–N1	R12–U13	F15–E17	C6–A5
N2–N3	T13–R13	E16–E15	B5–C5
P1–P2	U14–T14	D17–D16	A4–B4
P3–R1	R14–U15	D15–C17	C4–A3
R2–T1	T15–U16	C16–B17	B3–A2

GGW 176 **PIN ASSIGNMENT NET LIST**

PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#
1	B1	36	N1	71	P10	106	K14	141	A13
2	C2	37	N2	72	R10	107	K15	142	C12
3	C1	38	N3	73	U11	108	K16	143	B12
4	D3	39	P1	74	T11	109	J17	144	A12
5	D2	40	P2	75	R11	110	J14	145	D11
6	D1	41	P3	76	P11	111	J15	146	C11
7	E3	42	R1	77	U12	112	J16	147	B11
8	E2	43	R2	78	T12	113	H17	148	A11
9	E1	44	T1	79	R12	114	H16	149	A10
10	F3	45	U2	80	U13	115	H14	150	D10
11	F2	46	T3	81	T13	116	H15	151	C10
12	F1	47	U3	82	R13	117	G17	152	B10
13	G4	48	R4	83	U14	118	G16	153	A9
14	G3	49	T4	84	T14	119	G15	154	D9
15	G2	50	U4	85	R14	120	G14	155	C9
16	G1	51	R5	86	U15	121	F17	156	B9
17	H1	52	T5	87	T15	122	F16	157	A8
18	H4	53	U5	88	U16	123	F15	158	B8
19	H3	54	R6	89	T17	124	E17	159	D8
20	H2	55	T6	90	R16	125	E16	160	C8
21	J1	56	U6	91	R17	126	E15	161	A7
22	J4	57	P7	92	P15	127	D17	162	B7
23	J3	58	R7	93	P16	128	D16	163	C7
24	J2	59	T7	94	P17	129	D15	164	D7
25	K1	60	U7	95	N15	130	C17	165	A6
26	K2	61	U8	96	N16	131	C16	166	B6
27	K4	62	P8	97	N17	132	B17	167	C6
28	K3	63	R8	98	M15	133	A16	168	A5
29	L1	64	T8	99	M16	134	B15	169	B5
30	L2	65	U9	100	M17	135	A15	170	C5
31	L3	66	P9	101	L14	136	C14	171	A4
32	L4	67	R9	102	L15	137	B14	172	B4
33	M1	68	T9	103	L16	138	A14	173	C4
34	M2	69	U10	104	L17	139	C13	174	A3
35	M3	70	T10	105	K17	140	B13	175	B3
								176	A2

208GGW PACKAGE OUTLINE (15 x 15 mm, 0.8 mm pitch)

GGW (S-PBGA-N208) **PLASTIC BALL GRID ARRAY**

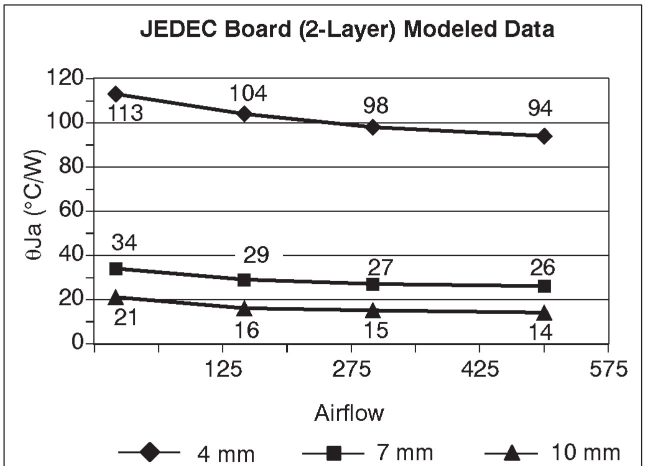


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

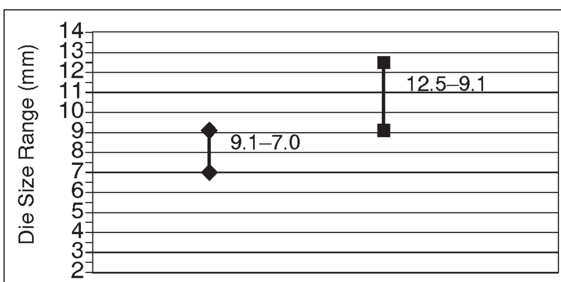
Electrical Characteristics

	R (Ω)	L (nH)	C (pF)
Min.	0.070	1.824	0.217
Mean	0.075	2.266	0.278
Max.	0.079	3.416	0.433

Thermal Characteristics



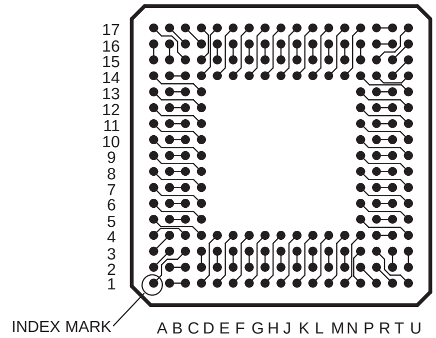
Productization



Part #	4166643	4166643
Samples	Now	Now
Qualified	Complete	Complete

MicroStar BGA is a trademark of Texas Instruments Incorporated.

GGW 208 TOP VIEW **DAISY CHAIN NET LIST**



B2–C2	J1–K4	T2–T3	U9–P10	T16–R16	J17–H14	B16–B15	A9–D8
B1–C1	K3–K2	U2–U3	R10–T10	T17–R17	H15–H16	A16–A15	C8–B8
D3–D2	K1–L4	R4–T4	U10–P11	P15–P16	H17–G14	C14–B14	A8–D7
D1–E4	L3–L2	U4–P5	R11–T11	P17–N14	G15–G16	A14–D13	C7–B7
E3–E2	L1–M4	R5–T5	U11–P12	N15–N16	G17–F14	C13–B13	A7–D6
E1–F4	M3–M2	U5–P6	R12–T12	N17–M14	F15–F16	A13–D12	C6–B6
F3–F2	M1–N4	R6–T6	U12–P13	M15–M16	F17–E14	C12–B12	A6–D5
F1–G4	N3–N2	U6–P7	R13–T13	M17–L14	E15–E16	A12–D11	C5–B5
G3–G2	N1–P4	R7–T7	U13–P14	L15–L16	E17–D14	C11–B11	A5–D4
G1–H4	P1–P3	U7–P8	U14–R14	L17–K14	D17–D15	A11–D10	A4–C4
H3–H2	P2–R1	R8–T8	T14–U15	K15–K16	D16–C17	C10–B10	B4–A3
H1–J4	R2–T1	U8–P9	T15–U16	K17–J14	C16–B17	A10–D9	B3–A2
J3–J2	R3–U1	R9–T9	R15–U17	J15–J16	C15–A17	C9–B9	C3–A1

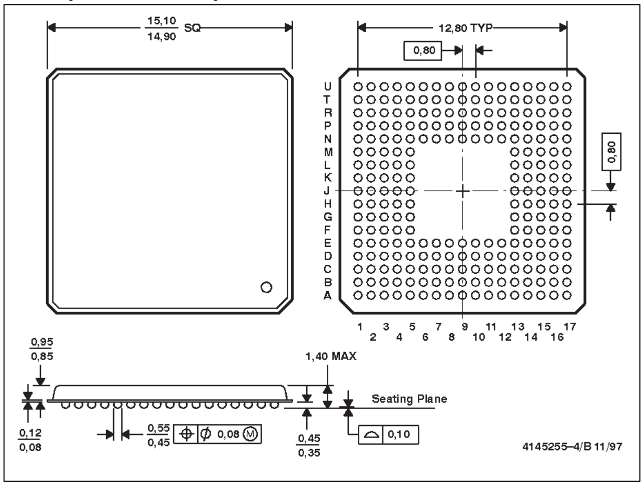
GGW 208 **PIN ASSIGNMENT NET LIST**

PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#
1	B2	27	J1	53	T2	79	U9	105	T16	131	J17	157	B16	183	A9
2	C2	28	K4	54	T3	80	P10	106	R16	132	H14	158	B15	184	D8
3	B1	29	K3	55	U2	81	R10	107	T17	133	H15	159	A16	185	C8
4	C1	30	K2	56	U3	82	T10	108	R17	134	H16	160	A15	186	B8
5	D3	31	K1	57	R4	83	U10	109	P15	135	H17	161	C14	187	A8
6	D2	32	L4	58	T4	84	P11	110	P16	136	G14	162	B14	188	D7
7	D1	33	L3	59	U4	85	R11	111	P17	137	G15	163	A14	189	C7
8	E4	34	L2	60	P5	86	T11	112	N14	138	G16	164	D13	190	B7
9	E3	35	L1	61	R5	87	U11	113	N15	139	G17	165	C13	191	A7
10	E2	36	M4	62	T5	88	P12	114	N16	140	F14	166	B13	192	D6
11	E1	37	M3	63	U5	89	R12	115	N17	141	F15	167	A13	193	C6
12	F4	38	M2	64	P6	90	T12	116	M14	142	F16	168	D12	194	B6
13	F3	39	M1	65	R6	91	U12	117	M15	143	F17	169	C12	195	A6
14	F2	40	N4	66	T6	92	P13	118	M16	144	E14	170	B12	196	D5
15	F1	41	N3	67	U6	93	R13	119	M17	145	E15	171	A12	197	C5
16	G4	42	N2	68	P7	94	T13	120	L14	146	E16	172	D11	198	B5
17	G3	43	N1	69	R7	95	U13	121	L15	147	E17	173	C11	199	A5
18	G2	44	P4	70	T7	96	P14	122	L16	148	D14	174	B11	200	D4
19	G1	45	P1	71	U7	97	U14	123	L17	149	D17	175	A11	201	A4
20	H4	46	P3	72	P8	98	R14	124	K14	150	D15	176	D10	202	C4
21	H3	47	P2	73	R8	99	T14	125	K15	151	D16	177	C10	203	B4
22	H2	48	R1	74	T8	100	U15	126	K16	152	C17	178	B10	204	A3
23	H1	49	R2	75	U8	101	T15	127	K17	153	C16	179	A10	205	B3
24	J4	50	T1	76	P9	102	U16	128	J14	154	B17	180	D9	206	A2
25	J3	51	R3	77	R9	103	R15	129	J15	155	C15	181	C9	207	C3
26	J2	52	U1	78	T9	104	U17	130	J16	156	A17	182	B9	208	A1

Appendix B
Package Data Sheets

240GGW PACKAGE OUTLINE
(15 x 15 mm, 0.8 mm pitch)

GGW (S-PBGA-N240) PLASTIC BALL GRID ARRAY

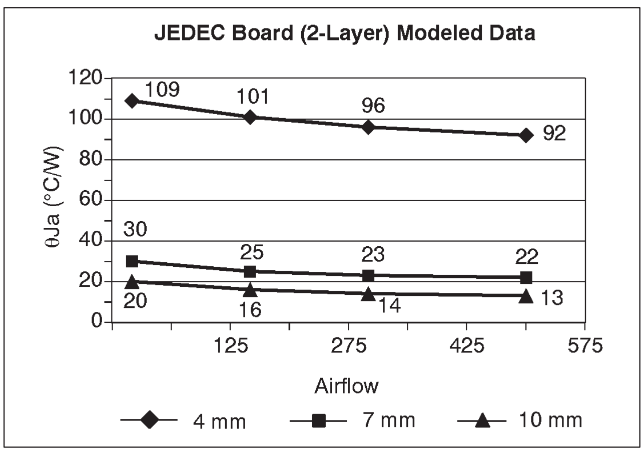


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

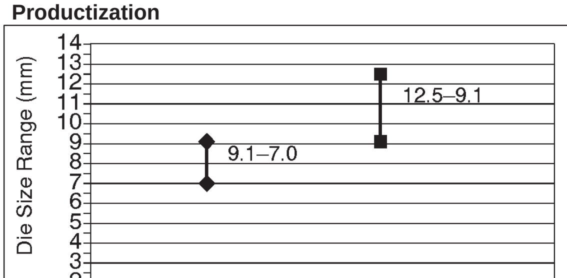
Electrical Characteristics

IN DEVELOPMENT

Thermal Characteristics



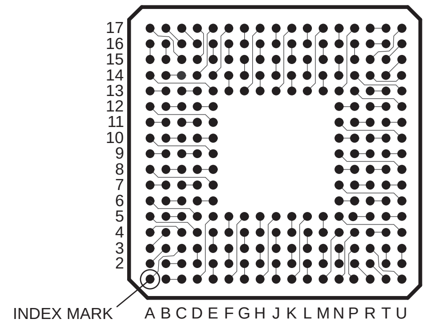
Productization



Part #	4166643	4166643
Samples	Now	Now
Qualified	Complete	Complete

MicroStar BGA is a trademark of Texas Instruments Incorporated.

GGW 240 TOP VIEW DAISY CHAIN NET LIST



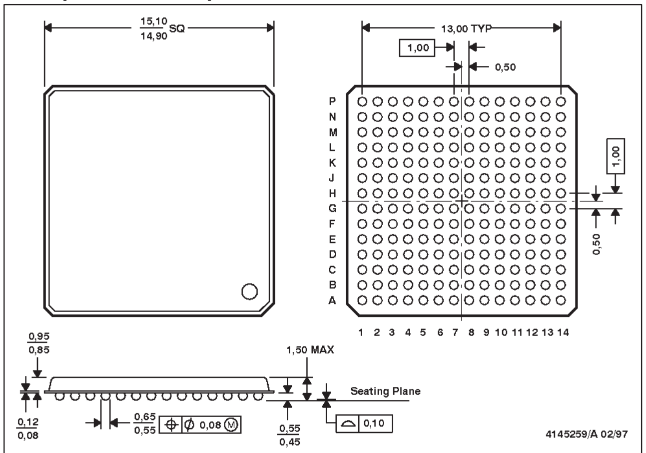
B2–C2	J2–J1	T2–T3	T9–U9	T16–R16	J16–J17	B16–B15	B9–A9
B1–C1	K5–K4	U2–U3	N10–P10	T17–R17	H13–H14	A16–A15	E8–D8
D3–D2	K3–K2	R4–T4	R10–T10	P15–P16	H15–H16	C14–B14	C8–B8
D1–E5	K1–L5	U4–N5	U10–N11	P17–N13	H17–G13	A14–E13	A8–E7
E4–E3	L4–L3	P5–R5	P11–R11	N14–N15	G14–G15	D13–C13	D7–C7
E2–E1	L2–L1	T5–U5	T11–U11	N16–N17	G16–G17	B13–A13	B7–A7
F5–F4	M5–M4	N6–P6	N12–P12	M13–M14	F13–F14	E12–D12	E6–D6
F3–F2	M3–M2	R6–T6	R12–T12	M15–M16	F15–F16	C12–B12	C6–B6
F1–G5	M1–N4	U6–N7	U12–P13	M17–L13	F17–E14	A12–E11	A6–D5
G4–G3	N3–N2	P7–R7	R13–T13	L14–L15	E15–E16	D11–C11	C5–B5
G2–G1	N1–P4	T7–U7	U13–P14	L16–L17	E17–D14	B11–A11	A5–D4
H5–H4	P1–P3	N8–P8	U14–R14	K13–K14	D17–D15	E10–D10	A4–C4
H3–H2	P2–R1	R8–T8	T14–U15	K15–K16	D16–C17	C10–B10	B4–A3
H1–J5	R2–T1	U8–N9	T15–U16	K17–J13	C16–B17	A10–E9	B3–A2
J4–J3	R3–U1	P9–R9	R15–U17	J14–J15	C15–A17	D9–C9	C3–A1

GGW 240 PIN ASSIGNMENT NET LIST

PIN# BALL#	PIN# BALL#	PIN# BALL#	PIN# BALL#	PIN# BALL#	PIN# BALL#	PIN# BALL#	PIN# BALL#
1 — B2	31 — J2	61 — T2	91 — T9	121— T16	151 — J16	181— B16	211 — B9
2 — C2	32 — J1	62 — T3	92 — U9	122— R16	152 — J17	182— B15	212 — A9
3 — B1	33 — K5	63 — U2	93 — N10	123— T17	153 — H13	183— A16	213 — E8
4 — C1	34 — K4	64 — U3	94 — P10	124— R17	154 — H14	184— A15	214 — D8
5 — D3	35 — K3	65 — R4	95 — R10	125— P15	155 — H15	185— C14	215 — C8
6 — D2	36 — K2	66 — T4	96 — T10	126— P16	156 — H16	186— B14	216 — B8
7 — D1	37 — K1	67 — U4	97 — U10	127— P17	157 — H17	187— A14	217 — A8
8 — E5	38 — L5	68 — N5	98 — N11	128— N13	158 — G13	188— E13	218 — E7
9 — E4	39 — L4	69 — P5	99 — P11	129— N14	159 — G14	189— D13	219 — D7
10 — E3	40 — L3	70 — R5	100 — R11	130— N15	160 — G15	190— C13	220 — C7
11 — E2	41 — L2	71 — T5	101 — T11	131— N16	161 — G16	191— B13	221 — B7
12 — E1	42 — L1	72 — U5	102 — U11	132— N17	162 — G17	192— A13	222 — A7
13 — F5	43 — M5	73 — N6	103 — N12	133— M13	163 — F13	193— E12	223 — E6
14 — F4	44 — M4	74 — P6	104 — P12	134— M14	164 — F14	194— D12	224 — D6
15 — F3	45 — M3	75 — R6	105 — R12	135— M15	165 — F15	195— C12	225 — C6
16 — F2	46 — M2	76 — T6	106 — T12	136— M16	166 — F16	196— B12	226 — B6
17 — F1	47 — M1	77 — U6	107 — U12	137— M17	167 — F17	197— A12	227 — A6
18 — G5	48 — N4	78 — N7	108 — P13	138— L13	168 — E14	198— E11	228 — D5
19 — G4	49 — N3	79 — P7	109 — R13	139— L14	169 — E15	199— D11	229 — C5
20 — G3	50 — N2	80 — R7	110 — T13	140— L15	170 — E16	200— C11	230 — B5
21 — G2	51 — N1	81 — T7	111 — U13	141— L16	171 — E17	201— B11	231 — A5
22 — G1	52 — P4	82 — U7	112 — P14	142— L17	172 — D14	202— A11	232 — D4
23 — H5	53 — P1	83 — N8	113 — U14	143— K13	173 — D17	203— E10	233 — A4
24 — H4	54 — P3	84 — P8	114 — R14	144— K14	174 — D15	204— D10	234 — C4
25 — H3	55 — P2	85 — R8	115 — T14	145— K15	175 — D16	205— C10	235 — B4
26 — H2	56 — R1	86 — T8	116 — U15	146— K16	176 — C17	206— B10	236 — A3
27 — H1	57 — R2	87 — U8	117 — T15	147— K17	177 — C16	207— A10	237 — B3
28 — J5	58 — T1	88 — N9	118 — U16	148— J13	178 — B17	208— E9	238 — A2
29 — J4	59 — R3	89 — P9	119 — R15	149— J14	179 — C15	209— D9	239 — C3
30 — J3	60 — U1	90 — R9	120 — U17	150— J15	180 — A17	210— C9	240 — A1

196GHC PACKAGE OUTLINE
(15 x 15 mm, 1.0 mm pitch)

GHC (S-PBGA-N196) **PLASTIC BALL GRID ARRAY**

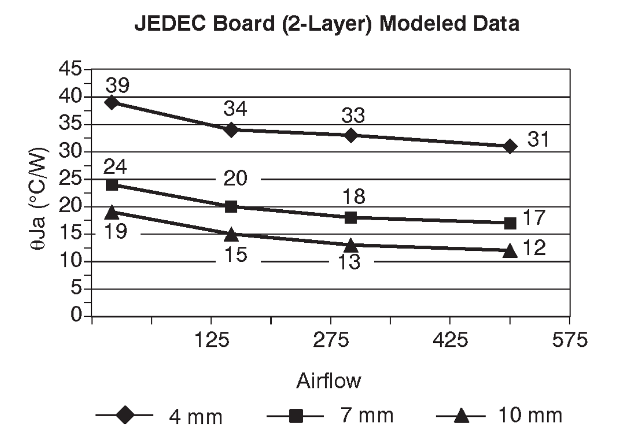


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

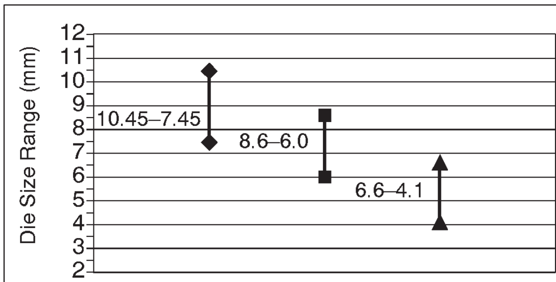
Electrical Characteristics

	R (Ω)	L (nH)	C (pF)
Min.	0.078	2.174	0.256
Mean	0.092	3.288	0.470
Max.	0.123	6.418	1.071

Thermal Characteristics



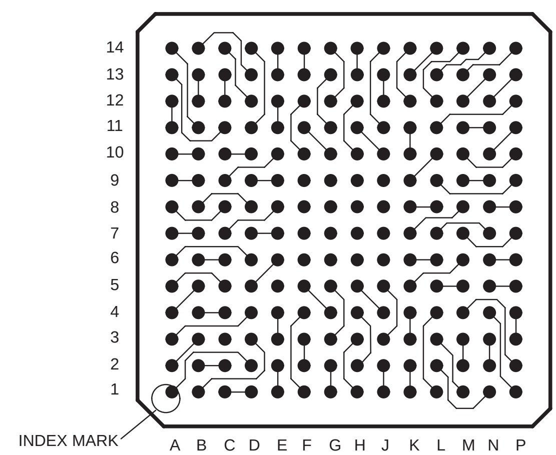
Productization



Part #	4146653	4192777	4192775
Samples	Now	Now	Now
Qualified	Complete	Complete	Complete

MicroStar BGA is a trademark of Texas Instruments Incorporated.

GHC 196 TOP VIEW **DAISY CHAIN NET LIST**



B2 – C2	H5 – J4	N5 – P5	M10 – P10	J14 – J11	D13 – B14	E8 – C7
A1 – D2	J1 – J2	M5 – L5	N10 – P11	J10 – H11	C13 – C12	A7 – B7
B1 – D3	J3 – J5	K5 – M6	L11 – P12	H13 – H14	B13 – B12	D7 – E7
C1 – D1	K4 – K3	N6 – P6	M11 – N11	H12 – H10	A14 – B11	D6 – A6
E2 – E1	K1 – K2	L6 – K6	P13 – N12	G12 – G14	A13 – C11	B6 – C6
E3 – E4	L1 – L4	L7 – N7	M12 – N13	G13 – G11	A12 – A11	E6 – D5
F3 – F2	M1 – L3	P7 – M7	M13 – P14	G10 – F11	B10 – A10	C5 – A5
F1 – F4	L2 – N1	K7 – M8	L13 – N14	F14 – F13	C10 – D10	B5 – A4
F5 – G4	M2 – M3	P8 – N8	L12 – M14	F12 – F10	E10 – C9	D4 – A3
G2 – G1	N2 – N3	L8 – K8	L14 – K13	E11 – E12	B9 – A9	C4 – B4
G3 – G5	P1 – N4	L9 – P9	K14 – K12	E14 – E13	D9 – E9	A2 – B3
H3 – H1	P2 – M4	N9 – M9	K11 – K10	D14 – D11	D8 – B8	
H2 – H4	P3 – P4	K9 – L10	J12 – J13	C14 – D12	A8 – C8	

Internal connection – E5,F6,F7,F8,F9,G6,G7,G8,G9,H6,H7,H8,H9,J6,J7,J8,J9

NC – C3

GHC 196 **PIN ASSIGNMENT NET LIST**

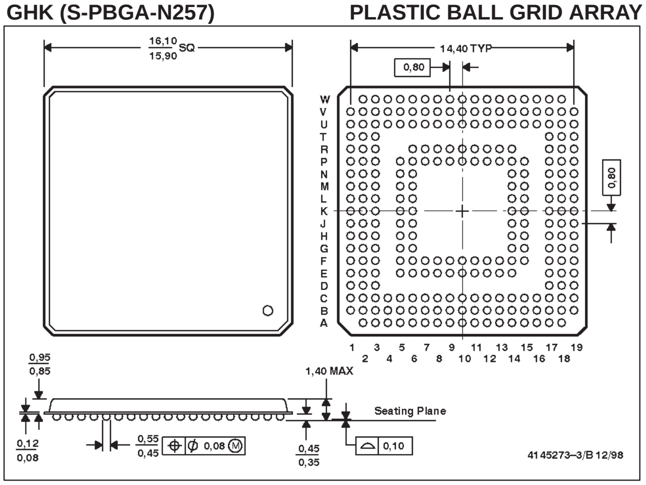
PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#
1 –	B2	27 –	H5	53 –	N5	79 –	M10	105 –	J14	131 –	D13	157 –	E8
2 –	C2	28 –	J4	54 –	P5	80 –	P10	106 –	J11	132 –	B14	158 –	C7
3 –	A1	29 –	J1	55 –	M5	81 –	N10	107 –	J10	133 –	C13	159 –	A7
4 –	D2	30 –	J2	56 –	L5	82 –	P11	108 –	H11	134 –	C12	160 –	B7
5 –	B1	31 –	J3	57 –	K5	83 –	L11	109 –	H13	135 –	B13	161 –	D7
6 –	D3	32 –	J5	58 –	M6	84 –	P12	110 –	H14	136 –	B12	162 –	E7
7 –	C1	33 –	K4	59 –	N6	85 –	M11	111 –	H12	137 –	A14	163 –	D6
8 –	D1	34 –	K3	60 –	P6	86 –	N11	112 –	H10	138 –	B11	164 –	A6
9 –	E2	35 –	K1	61 –	L6	87 –	P13	113 –	G12	139 –	A13	165 –	B6
10 –	E1	36 –	K2	62 –	K6	88 –	N12	114 –	G14	140 –	C11	166 –	C6
11 –	E3	37 –	L1	63 –	L7	89 –	M12	115 –	G13	141 –	A12	167 –	E6
12 –	E4	38 –	L4	64 –	N7	90 –	N13	116 –	G11	142 –	A11	168 –	D5
13 –	F3	39 –	M1	65 –	P7	91 –	M13	117 –	G10	143 –	B10	169 –	C5
14 –	F2	40 –	L3	66 –	M7	92 –	P14	118 –	F11	144 –	A10	170 –	A5
15 –	F1	41 –	L2	67 –	K7	93 –	L13	119 –	F14	145 –	C10	171 –	B5
16 –	F4	42 –	N1	68 –	M8	94 –	N14	120 –	F13	146 –	D10	172 –	A4
17 –	F5	43 –	M2	69 –	P8	95 –	L12	121 –	F12	147 –	E10	173 –	D4
18 –	G4	44 –	M3	70 –	N8	96 –	M14	122 –	F10	148 –	C9	174 –	A3
19 –	G2	45 –	N2	71 –	L8	97 –	L14	123 –	E11	149 –	B9	175 –	C4
20 –	G1	46 –	N3	72 –	K8	98 –	K13	124 –	E12	150 –	A9	176 –	B4
21 –	G3	47 –	P1	73 –	L9	99 –	K14	125 –	E14	151 –	D9	177 –	A2
22 –	G5	48 –	N4	74 –	P9	100 –	K12	126 –	E13	152 –	E9	178 –	B3
23 –	H3	49 –	P2	75 –	N9	101 –	K11	127 –	D14	153 –	D8	179 –	C3
24 –	H1	50 –	M4	76 –	M9	102 –	K10	128 –	D11	154 –	B8		
25 –	H2	51 –	P3	77 –	K9	103 –	J12	129 –	C14	155 –	A8		
26 –	H4	52 –	P4	78 –	L10	104 –	J13	130 –	D12	156 –	C8		

Internal connection – E5,F6,F7,F8,F9,G6,G7,G8,G9,H6,H7,H8,H9,J6,J7,J8,J9

Appendix B
Package Data Sheets

257GHK PACKAGE OUTLINE
(16 x 16 mm, 0.8 mm pitch)

GHK (S-PBGA-N257) PLASTIC BALL GRID ARRAY

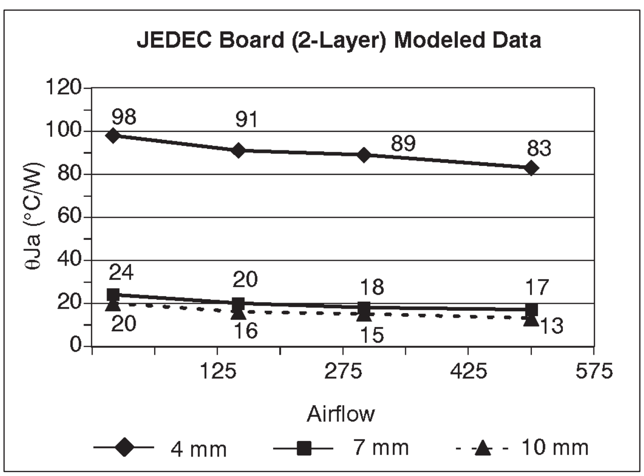


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

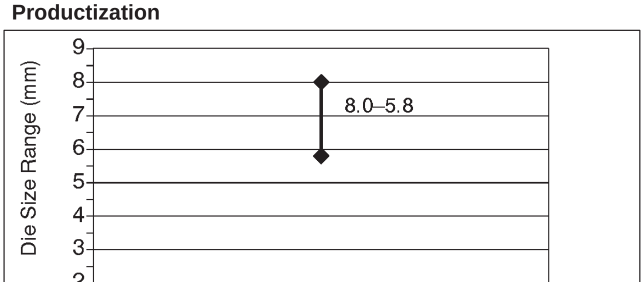
Electrical Characteristics

IN DEVELOPMENT

Thermal Characteristics



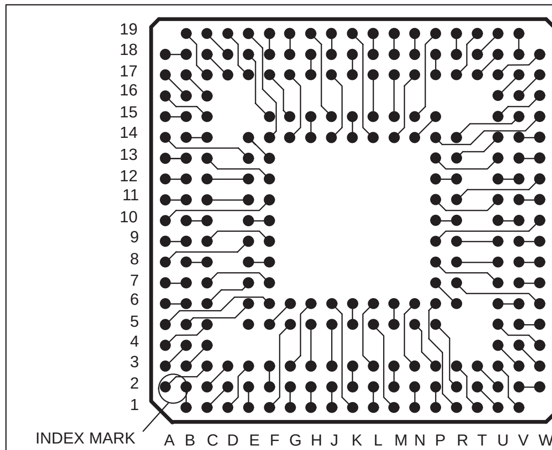
Productization



Part # 4166696
Samples Now
Qualified Complete

MicroStar BGA is a trademark of Texas Instruments Incorporated.

GHK 257 TOP VIEW DAISY CHAIN NET LIST



B2–B1	K5–K6	V2–W2	R10–P10	V18–V19	K15–K14	B18–A18	E10–F10
D3–C2	L1–L2	U4–V3	W11–V11	T17–U18	J19–J18	C16–B17	A9–B9
C1–D2	L3–L6	W3–V4	U11–P11	U19–T18	J17–J14	A17–B16	C9–F9
D1–E3	L5–M1	W4–U5	R11–W12	T19–R17	J15–H19	A16–C15	E9–A8
F5–G6	M2–M3	R6–P7	V12–U12	P15–N14	H18–H17	E14–F13	B8–C8
E2–E1	M6–M5	V5–W5	P12–R12	R18–R19	H14–H15	B15–A15	F8–E8
F3–F2	N1–N2	U6–V6	W13–V13	P17–P18	G19–G18	C14–B14	A7–B7
G5–F1	N3–N6	R7–W6	U13–P13	N15–P19	G17–G14	E13–A14	C7–F7
H6–G3	P1–P2	P8–U7	W14–V14	M14–N17	F19–F18	F12–C13	A6–B6
G2–G1	N5–P3	V7–W7	R13–U14	N18–N19	G15–F17	B13–A13	E7–C6
H5–H3	R1–P6	R8–U8	W15–P14	M15–M17	E19–F14	E12–C12	A5–F6
H2–H1	R2–P5	V8–W8	V15–R14	M18–M19	E18–F15	B12–A12	B5–E6
J1–J2	R3–T1	W9–V9	U15–W16	L19–L18	E17–D19	A11–B11	C5–A4
J3–J5	T2–U1	U9–R9	V16–W17	L17–L15	D18–C19	C11–E11	B4–A3
J6–K1	T3–U2	P9–W10	U16–V17	L14–K19	D17–C18	F11–A10	C4–B3
K2–K3	V1–U3	V10–U10	W18–U17	K18–K17	B19–C17	B10–C10	A2–C3

NC–E5

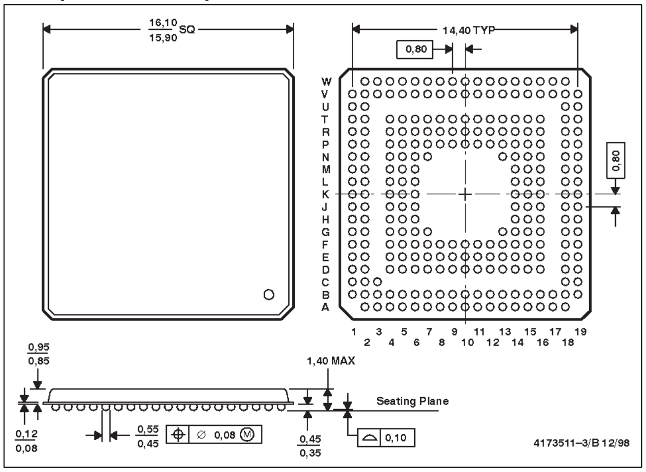
GHK 257 PIN ASSIGNMENT NET LIST

PIN#BALL#	PIN#BALL#	PIN#BALL#	PIN#BALL#	PIN#BALL#	PIN#BALL#	PIN#BALL#	PIN#BALL#
1 – B2	33 – K5	65 – V2	97 – R10	129 – V18	161 – K15	193 – B18	225 – E10
2 – B1	34 – K6	66 – W2	98 – P10	130 – V19	162 – K14	194 – A18	226 – F10
3 – D3	35 – L1	67 – U4	99 – W11	131 – T17	163 – J19	195 – C16	227 – A9
4 – C2	36 – L2	68 – V3	100 – V11	132 – U18	164 – J18	196 – B17	228 – B9
5 – C1	37 – L3	69 – W3	101 – U11	133 – U19	165 – J17	197 – A17	229 – C9
6 – D2	38 – L6	70 – V4	102 – P11	134 – T18	166 – J14	198 – B16	230 – F9
7 – D1	39 – L5	71 – W4	103 – R11	135 – T19	167 – J15	199 – A16	231 – E9
8 – E3	40 – M1	72 – U5	104 – W12	136 – R17	168 – H19	200 – C15	232 – A8
9 – F5	41 – M2	73 – R6	105 – V12	137 – P15	169 – H18	201 – E14	233 – B8
10 – G6	42 – M3	74 – P7	106 – U12	138 – N14	170 – H17	202 – F13	234 – C8
11 – E2	43 – M6	75 – V5	107 – P12	139 – R18	171 – H14	203 – B15	235 – F8
12 – E1	44 – M5	76 – W5	108 – R12	140 – R19	172 – H15	204 – A15	236 – E8
13 – F3	45 – N1	77 – U6	109 – W13	141 – P17	173 – G19	205 – C14	237 – A7
14 – F2	46 – N2	78 – V6	110 – V13	142 – P18	174 – G18	206 – B14	238 – B7
15 – G5	47 – N3	79 – R7	111 – U13	143 – N15	175 – G17	207 – E13	239 – C7
16 – F1	48 – N6	80 – W6	112 – P13	144 – P19	176 – G14	208 – A14	240 – F7
17 – H6	49 – P1	81 – P8	113 – W14	145 – M14	177 – F19	209 – F12	241 – A6
18 – G3	50 – P2	82 – U7	114 – V14	146 – N17	178 – F18	210 – C13	242 – B6
19 – G2	51 – N5	83 – V7	115 – R13	147 – N18	179 – G15	211 – B13	243 – E7
20 – G1	52 – P3	84 – W7	116 – U14	148 – N19	180 – F17	212 – A13	244 – C6
21 – H5	53 – R1	85 – R8	117 – W15	149 – M15	181 – E19	213 – E12	245 – A5
22 – H3	54 – P6	86 – U8	118 – P14	150 – M17	182 – F14	214 – C12	246 – F6
23 – H2	55 – R2	87 – V8	119 – V15	151 – M18	183 – E18	215 – B12	247 – B5
24 – H1	56 – P5	88 – W8	120 – R14	152 – M19	184 – F15	216 – A12	248 – E6
25 – J1	57 – R3	89 – W9	121 – U15	153 – L19	185 – E17	217 – A11	249 – C5
26 – J2	58 – T1	90 – V9	122 – W16	154 – L18	186 – D19	218 – B11	250 – A4
27 – J3	59 – T2	91 – U9	123 – V16	155 – L17	187 – D18	219 – C11	251 – B4
28 – J5	60 – U1	92 – R9	124 – W17	156 – L15	188 – C19	220 – E11	252 – A3
29 – J6	61 – T3	93 – P9	125 – U16	157 – L14	189 – D17	221 – F11	253 – C4
30 – K1	62 – U2	94 – W10	126 – V17	158 – K19	190 – C18	222 – A10	254 – B3
31 – K2	63 – V1	95 – V10	127 – W18	159 – K18	191 – B19	223 – B10	255 – A2
32 – K3	64 – U3	96 – U10	128 – U17	160 – K17	192 – C17	224 – C10	256 – C3

ID BALL – E5

257GJG PACKAGE OUTLINE
(16 x 16 mm, 0.8 mm pitch)

GJG (S-PBGA-N257) **PLASTIC BALL GRID ARRAY**

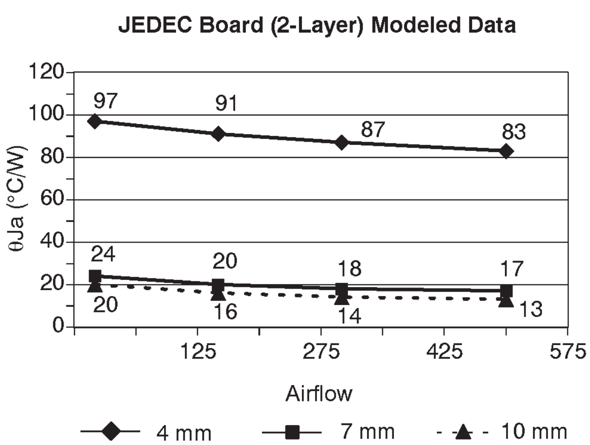


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

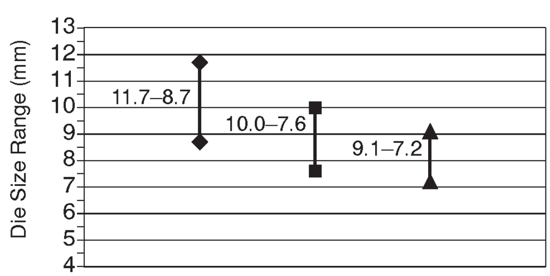
Electrical Characteristics

IN DEVELOPMENT

Thermal Characteristics



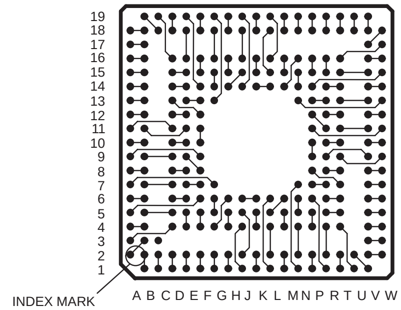
Productization



Part #	4200201	4166711	4184652
Samples	Now	Now	Now
Qualified	Complete	Complete	Complete

MicroStar BGA is a trademark of Texas Instruments Incorporated.

GJG 257 TOP VIEW **DAISY CHAIN NET LIST**



B2–B1	K4–K5	V2–W2	T10–R10	V18–V19	K16–K15	B18–A18	D10–E10
C1–C2	L6–L1	W3–V3	P11–W11	U19–U18	J14–J19	A17–B17	F9–A9
D1–D2	L2–L4	W4–V4	V11–T11	T19–T18	J18–J16	A16–B16	B9–D9
E4–E5	L5–M6	T5–R5	R11–P12	R16–R15	J15–H14	D15–E15	E9–F8
E1–E2	M1–M2	W5–V5	W12–V12	R19–R18	H19–H18	A15–B15	A8–B8
F5–F4	M4–M5	R6–T6	T12–R12	P15–P16	H16–H15	E14–D14	D8–E8
F1–F2	N7–N1	W6–V6	N13–W13	P19–P18	G13–G19	A14–B14	G7–A7
G6–G5	N2–N4	P7–R7	V13–T13	N14–N15	G18–G16	F13–E13	B7–D7
G2–G1	N5–N6	V7–W7	R13–P13	N18–N19	G15–G14	B13–A13	E7–F7
G4–H6	P1–P2	T7–P8	W14–V14	N16–M14	F19–F18	D13–F12	A6–B6
H1–H2	P4–P5	W8–V8	T14–R14	M19–M18	F16–F15	A12–B12	D6–E6
H4–H5	P6–R1	T8–R8	P14–W15	M16–M15	F14–E19	D12–E12	F6–A5
J4–J1	R2–R4	T9–W9	V15–T15	L16–L19	E18–E16	D11–A11	B5–D5
J2–J5	T1–T2	V9–R9	W16–V16	L18–L15	D19–D18	B11–E11	A4–B4
J6–K6	U1–T4	P9–P10	W17–T16	L14–K14	C19–D16	F11–F10	A3–D4
K1–K2	U2–V1	W10–V10	V17–W18	K19–K18	C18–B19	A10–B10	B3–A2

ID BALL–C3

GJG 257 **PIN ASSIGNMENT NET LIST**

PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#	PIN#	BALL#
1	B2	33	K4	65	V2	97	T10	129	V18	161	K16	193	B18	225	D10
2	B1	34	K5	66	W2	98	R10	130	V19	162	K15	194	A18	226	E10
3	C1	35	L6	67	W3	99	P11	131	U19	163	J14	195	A17	227	F9
4	C2	36	L1	68	V3	100	W11	132	U18	164	J19	196	B17	228	A9
5	D1	37	L2	69	W4	101	V11	133	T19	165	J18	197	A16	229	B9
6	D2	38	L4	70	V4	102	T11	134	T18	166	J16	198	B16	230	D9
7	E4	39	L5	71	T5	103	R11	135	R16	167	J15	199	D15	231	E9
8	E5	40	M6	72	R5	104	P12	136	R15	168	H14	200	E15	232	F8
9	E1	41	M1	73	W5	105	W12	137	R19	169	H19	201	A15	233	A8
10	E2	42	M2	74	V5	106	V12	138	R18	170	H18	202	B15	234	B8
11	F5	43	M4	75	R6	107	T12	139	P15	171	H16	203	E14	235	D8
12	F4	44	M5	76	T6	108	R12	140	P16	172	H15	204	D14	236	E8
13	F1	45	N7	77	W6	109	N13	141	P19	173	G13	205	A14	237	G7
14	F2	46	N1	78	V6	110	W13	142	P18	174	G19	206	B14	238	A7
15	G6	47	N2	79	P7	111	V13	143	N14	175	G18	207	F13	239	B7
16	G5	48	N4	80	R7	112	T13	144	N15	176	G16	208	E13	240	D7
17	G2	49	N5	81	V7	113	R13	145	N18	177	G15	209	B13	241	E7
18	G1	50	N6	82	W7	114	P13	146	N19	178	G14	210	A13	242	F7
19	G4	51	P1	83	T7	115	W14	147	N16	179	F19	211	D13	243	A6
20	H6	52	P2	84	P8	116	V14	148	M14	180	F18	212	F12	244	B6
21	H1	53	P4	85	W8	117	T14	149	M19	181	F16	213	A12	245	D6
22	H2	54	P5	86	V8	118	R14	150	M18	182	F15	214	B12	246	E6
23	H4	55	P6	87	T8	119	P14	151	M16	183	F14	215	D12	247	F6
24	H5	56	R1	88	R8	120	W15	152	M15	184	E19	216	E12	248	A5
25	J4	57	R2	89	T9	121	V15	153	L16	185	E18	217	D11	249	B5
26	J1	58	R4	90	W9	122	T15	154	L19	186	E16	218	A11	250	D5
27	J2	59	T1	91	V9	123	W16	155	L18	187	D19	219	B11	251	A4
28	J5	60	T2	92	R9	124	V16	156	L15	188	D18	220	E11	252	B4
29	J6	61	U1	93	P9	125	W17	157	L14	189	C19	221	F11	253	A3
30	K6	62	T4	94	P10	126	T16	158	K14	190	D16	222	F10	254	D4
31	K1	63	U2	95	W10	127	V17	159	K19	191	C18	223	A10	255	B3
32	K2	64	V1	96	V10	128	W18	160	K18	192	B19	224	B10	256	A2

1PIN MARK – C3

Appendix B
Package Data Sheets

Notes