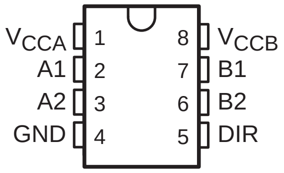
SN74LVC2T45
DUAL-BIT DUAL-SUPPLY TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

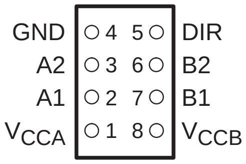
SCES516 − DECEMBER 2003

- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range**
- **V_{CC} Isolation Feature − If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State**
- **DIR Referenced to V_{CCA}**
- **Low Power Consumption, 10-µA Max I_{CC}**
- **±24-mA Output Drive at 3.3 V**
- **I_{off} Supports Partial-Power-Down Mode Operation**

DCT OR DCU PACKAGE
(TOP VIEW)



YEP OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

This dual-bit noninverting transceiver uses two separate configurable power-supply rails. The A-port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B-port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

The SN74LVC2T45 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input.

The SN74LVC2T245 is designed so that DIR is supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are in the high-impedance state.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[‡]
−40°C to 85°C	NanoStar™ − WCSP (DSBGA) 0.23-mm Large Bump − YEP	Tape and reel	SN74LVC2T45YEPR	TBD
	NanoFree™ − WCSP (DSBGA) 0.23-mm Large Bump − YZP (Pb-free)		SN74LVC2T45YZPR	
	SSOP − DCT	Tape and reel	SN74LVC2T45DCTR	TBD
	VSSOP − DCU	Tape and reel	SN74LVC2T45DCUR	TBD

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

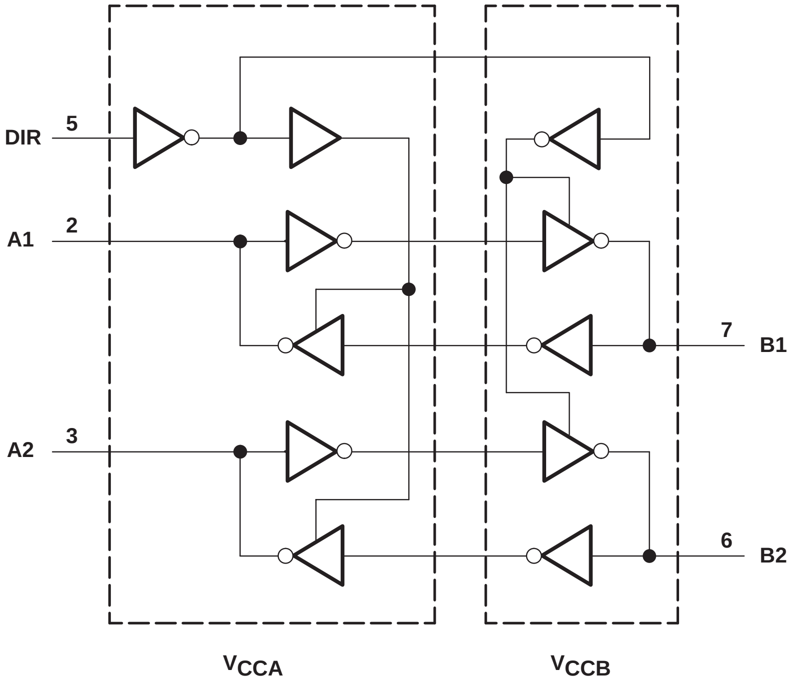
[‡] DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

NanoStar and NanoFree are trademarks of Texas Instruments.

FUNCTION TABLE
(each transceiver)

INPUT	OPERATION
DIR	
L	B data to A bus
H	A data to B bus

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CCA} and V_{CCB}	−0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	−0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	−0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	
A port	−0.5 V to V_{CCA} + 0.5V
B port	−0.5 V to V_{CCB} + 0.5V
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DCT package	220°C/W
DCU package	227°C/W
YEP/YZP package	102°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

PRODUCT PREVIEW

recommended operating conditions (see Notes 4 through 6)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.65	5.5	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs (see Note 7)	1.65 V to 1.95 V		$V_{CCI} \times 0.65$		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		$V_{CCI} \times 0.7$		
V_{IL}	Low-level input voltage	Data inputs (see Note 7)	1.65 V to 1.95 V			$V_{CCI} \times 0.35$	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			$V_{CCI} \times 0.3$	
V_{IH}	High-level input voltage	DIR (Referenced to V_{CCA}) (see Note 8)	1.65 V to 1.95 V		$V_{CCA} \times 0.65$		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		$V_{CCA} \times 0.7$		
V_{IL}	Low-level input voltage	DIR (Referenced to V_{CCA}) (see Note 8)	1.65 V to 1.95 V			$V_{CCA} \times 0.35$	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			$V_{CCA} \times 0.3$	
V_I	Input voltage				0	5.5	V
V_O	Output voltage				0	V_{CCO}	V
I_{OH}	High-level output current			1.65 V to 1.95 V		−4	mA
				2.3 V to 2.7 V		−8	
				3 V to 3.6 V		−24	
				4.5 V to 5.5 V		−32	
I_{OL}	Low-level output current			1.65 V to 1.95 V		4	mA
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		24	
				4.5 V to 5.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	Data inputs	1.65 V to 1.95 V			20	ns/V
			2.3 V to 2.7 V			20	
			3 V to 3.6 V			10	
			4.5 V to 5.5 V			5	
		Control input	1.65 V to 5.5 V			5	
T_A	Operating free-air temperature				−40	85	°C

NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.

5. V_{CCO} is the V_{CC} associated with the output port.

6. All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

7. For V_{CCI} values not specified in the data sheet, $V_{IH(min)} = V_{CCI} \times 0.7$ V, $V_{IL(max)} = V_{CCI} \times 0.3$ V.

8. For V_{CCI} values not specified in the data sheet, $V_{IH(min)} = V_{CCA} \times 0.7$ V, $V_{IL(max)} = V_{CCA} \times 0.3$ V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 9 and 10)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	−40°C to 85°C MIN	−40°C to 85°C MAX	UNIT
V_{OH}		I_{OH} = −100 µA, $V_I = V_{IH}$		1.65 V to 4.5 V	1.65 V to 4.5 V				V_{CCO}−0.1		V
		I_{OH} = −4 mA, $V_I = V_{IH}$		1.65V	1.65 V				1.2		
		I_{OH} = −8 mA, $V_I = V_{IH}$		2.3 V	2.3 V				1.9		
		I_{OH} = −24 mA, $V_I = V_{IH}$		3 V	3 V				2.4		
		I_{OH} = −32 mA, $V_I = V_{IH}$		4.5 V	4.5 V				3.8		
V_{OL}		I_{OL} = 100 µA, $V_I = V_{IL}$		1.65 V to 4.5 V	1.65 V to 4.5 V					0.1	V
		I_{OL} = 4 mA, $V_I = V_{IL}$		1.65 V	1.65 V					0.45	
		I_{OL} = 8 mA, $V_I = V_{IL}$		2.3 V	2.3 V					0.3	
		I_{OL} = 24 mA, $V_I = V_{IL}$		3 V	3 V					0.55	
		I_{OL} = 32 mA, $V_I = V_{IL}$		4.5 V	4.5 V					0.55	
I_I	DIR input	$V_I = V_{CCA}$ or GND		1.65 V to 5.5 V	1.65 V to 5.5 V			TBD		±5	µA
I_{off}	A port	V_I or V_O = 0 to 5.5 V		0 V	0 to 5.5 V			TBD		±10	µA
	B port			0 to 5.5 V	0 V			TBD		±10	
I_{OZ}	A or B ports	$V_O = V_{CCO}$ or GND		1.65 V to 5.5 V	1.65 V to 5.5 V			TBD		±10	µA
I_{CCA}		$V_I = V_{CCI}$ or GND	I_O = 0	1.95 V	1.95 V					1	µA
				2.7 V	2.7 V					1	
				3.6 V	3.6 V					1	
				5.5 V	0 V					2	
				0 V	5.5 V					0	
				5.5 V	5.5 V					1	
I_{CCB}		$V_I = V_{CCI}$ or GND	I_O = 0	1.95 V	1.95 V					1	µA
				2.7 V	2.7 V					1	
				3.6 V	3.6 V					1	
				5.5 V	0 V					0	
				0 V	5.5 V					2	
				5.5 V	5.5 V					1	
I_{CCA} + I_{CCB} (see Table 1)		$V_I = V_{CCI}$ or GND	I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V					4	µA
ΔI_{CCA}	A port	One A port at V_{CCA} − 0.6 V, DIR at V_{CCA}, B port = OPEN		3 V to 5.5 V	3 V to 5.5 V					50	µA
	DIR	DIR at V_{CCA} − 0.6 V, B port = OPEN, A port at V_{CCA} or GND								50	
ΔI_{CCB}	B port	One B port at V_{CCB} − 0.6 V, DIR at GND, A port = OPEN		3 V to 5.5 V	3 V to 5.5 V					50	µA
C_i	DIR input	$V_I = V_{CCA}$ or GND		3.3 V	3.3 V		TBD				pF
C_{io}	A or B ports	$V_O = V_{CCA/B}$ or GND		3.3 V	3.3 V		TBD				pF

NOTES: 9. V_{CCO} is the V_{CC} associated with the output port.
10. V_{CCI} is the V_{CC} associated with the input port.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B									ns
t_{PHL}											
t_{PLH}	B	A									ns
t_{PHL}											
t_{PZH}	DIR	A									ns
t_{PZL}											
t_{PZH}	DIR	B									ns
t_{PZL}											
t_{PHZ}	DIR	A									ns
t_{PLZ}											
t_{PHZ}	DIR	B									ns
t_{PLZ}											

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B									ns
t_{PHL}											
t_{PLH}	B	A									ns
t_{PHL}											
t_{PZH}	DIR	A									ns
t_{PZL}											
t_{PZH}	DIR	B									ns
t_{PZL}											
t_{PHZ}	DIR	A									ns
t_{PLZ}											
t_{PHZ}	DIR	B									ns
t_{PLZ}											

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B									ns
t_{PHL}											
t_{PLH}	B	A									ns
t_{PHL}											
t_{PZH}	DIR	A									ns
t_{PZL}											
t_{PZH}	DIR	B									ns
t_{PZL}											
t_{PHZ}	DIR	A									ns
t_{PLZ}											
t_{PHZ}	DIR	B									ns
t_{PLZ}											

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 5 V ± 0.5 V(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B									ns
t_{PHL}											
t_{PLH}	B	A									ns
t_{PHL}											
t_{PZH}	DIR	A									ns
t_{PZL}											
t_{PZH}	DIR	B									ns
t_{PZL}											
t_{PHZ}	DIR	A									ns
t_{PLZ}											
t_{PHZ}	DIR	B									ns
t_{PLZ}											

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	V_{CCA} = V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA}[†]	A port input, B port output	C_L = 0, f = 10 MHz, $t_r = t_f$ =1 ns					pF
	B port input, A port output						
C_{pdB}[†]	A port input, B port output						
	B port input, A port output						

[†] Power dissipation capacitance per transceiver

PRODUCT PREVIEW

power-up considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. Take the following precautions, in the order given, to guard against such power-up problems:

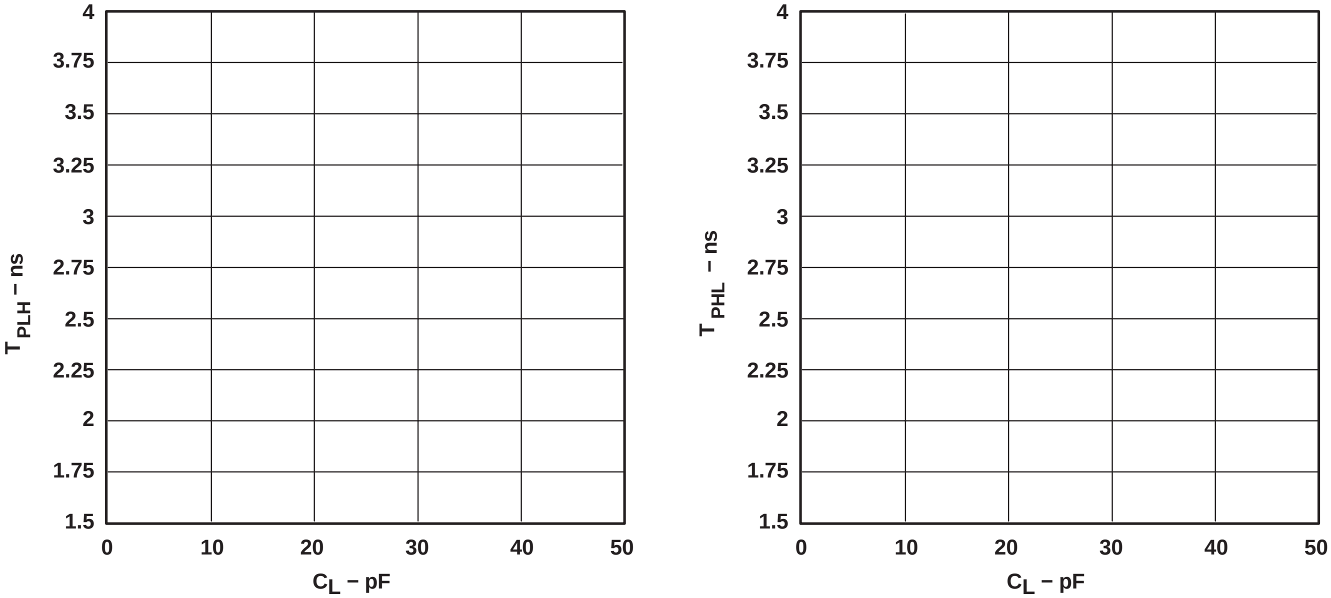
1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA}.
3. Ramp up V_{CCB} along with or after V_{CCA}.

typical total static power consumption (I_{CCA} and I_{CCB})

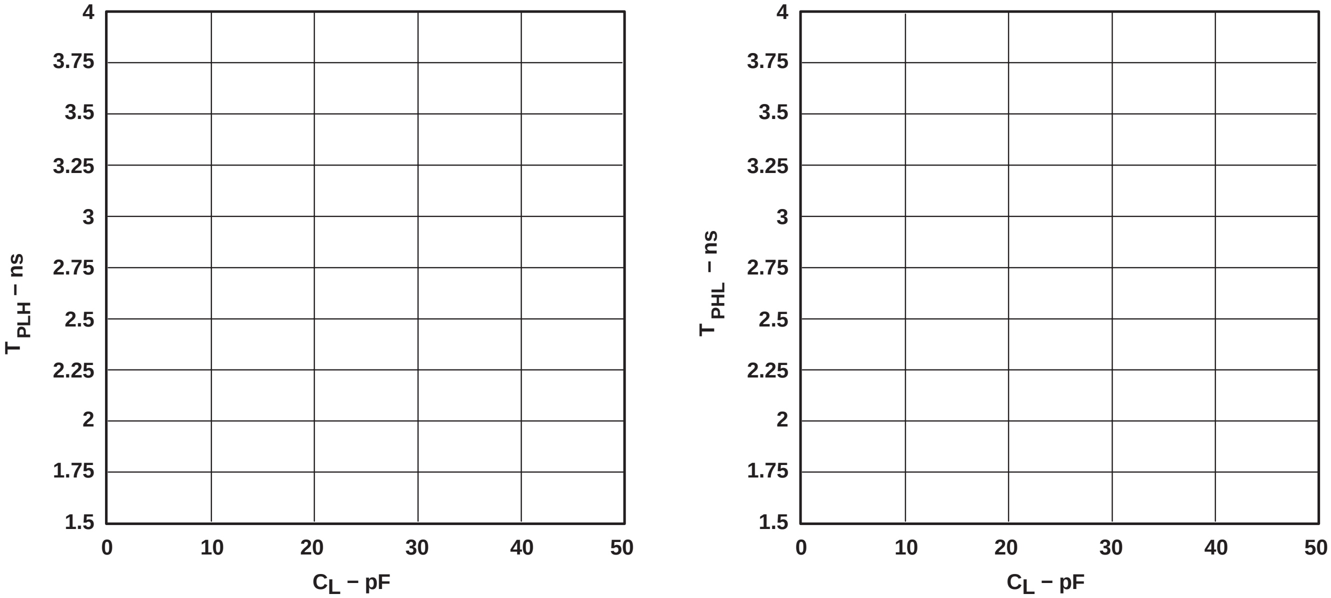
V_{CCB}	V_{CCA}				UNIT
	1.8 V	**2.5 V**	**3.3 V**	**5 V**	
1.8 V	<1	<1	<1	1.5	µA
2.5 V	<1	<1	<1	1	
3.3 V	<1	<1	<1	<1	
5 V	1.5	1	<1	<1	

TABLE 1

TYPICAL PROPAGATION DELAY vs LOAD CAPACITANCE,
$T_A = 25°C, V_{CCA} = 1.8\ V$



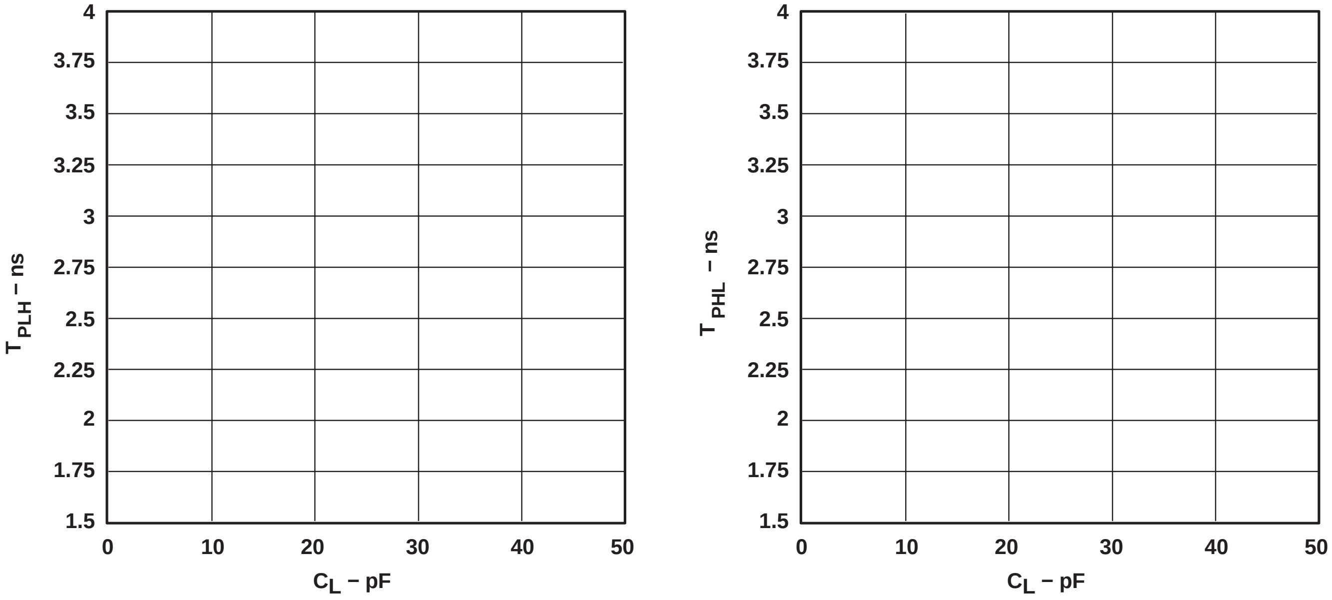
TYPICAL PROPAGATION DELAY vs LOAD CAPACITANCE,
$T_A = 25°C, V_{CCA} = 2.5\ V$



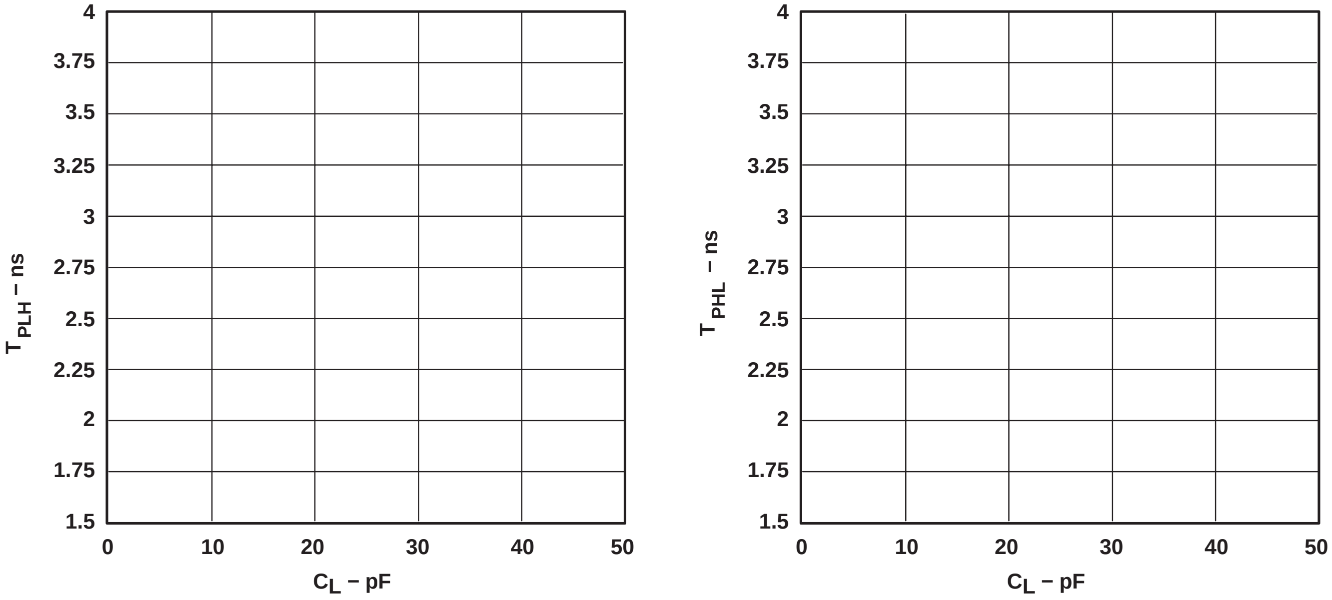
PRODUCT PREVIEW

PRODUCT PREVIEW

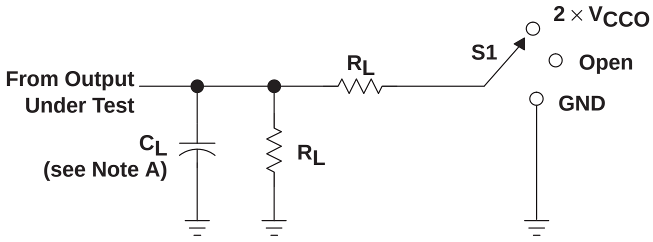
TYPICAL PROPAGATION DELAY vs LOAD CAPACITANCE,
T_A = 25°C, V_{CCA} = 3.3 V



TYPICAL PROPAGATION DELAY vs LOAD CAPACITANCE,
T_A = 25°C, V_{CCA} = 5 V



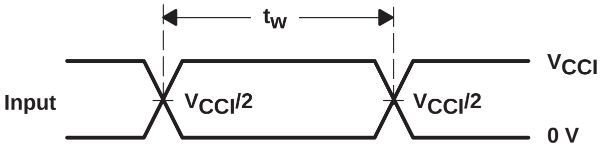
PARAMETER MEASUREMENT INFORMATION



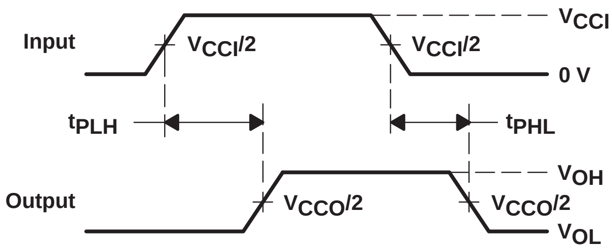
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

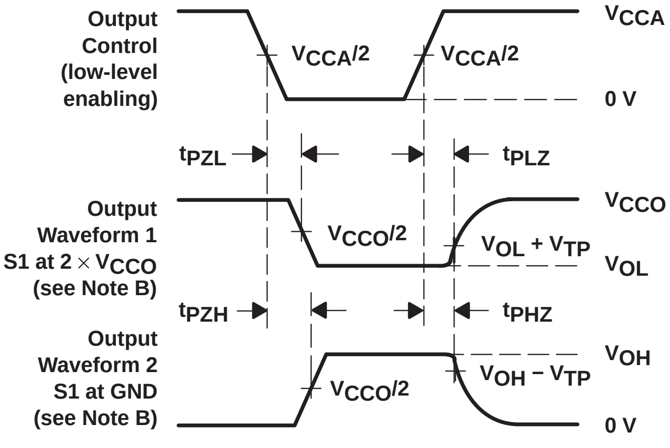
V_{CCO}	C_L	R_L	V_{TP}	t_r or t_f
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V	≤2 ns
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V	≤2 ns
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V	≤2.5 ns
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V	≤2.5 ns



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



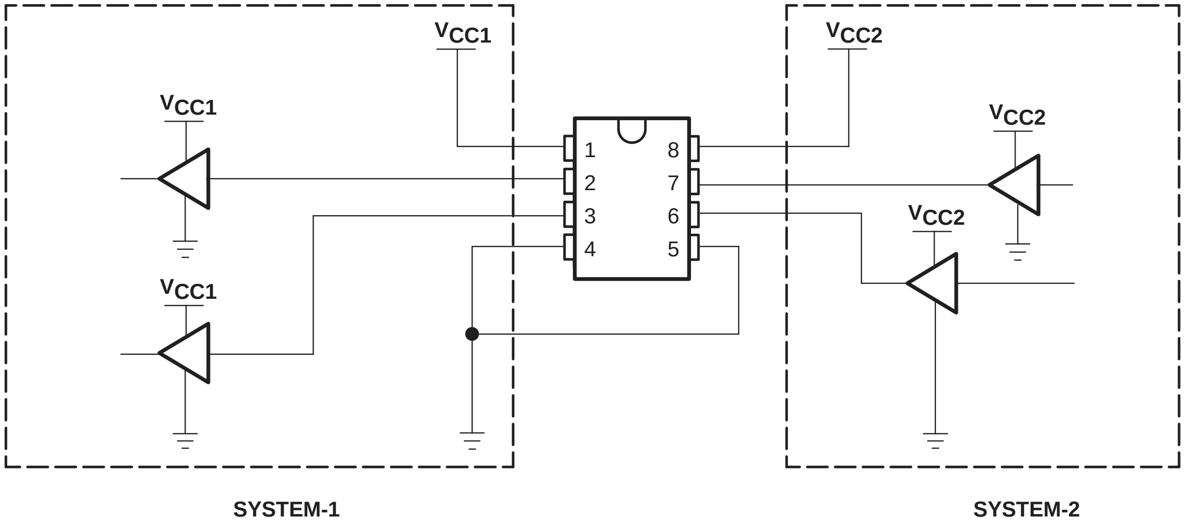
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time with one transition per measurement.
E. V_{CCI} is the power supply voltage associated with the input port.
F. V_{CCO} is the power supply voltage associated with the output port.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

The following circuit is an example of the SN74LVC2T45 used in a bidirectional logic level-shifting application.

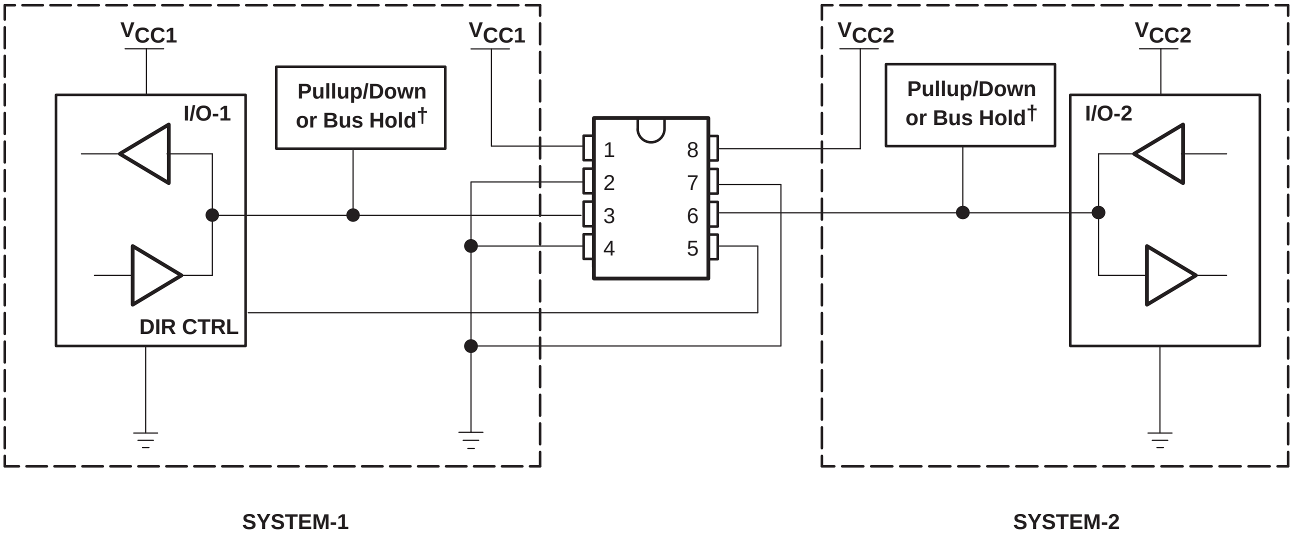


PIN	NAME	FUNCTION	DESCRIPTION
1	V_{CCA}	V_{CC1}	SYSTEM-1 supply voltage (1.65 V to 5.5 V)
2	A1	OUT1	Output level depends on V_{CC1} voltage
3	A2	OUT2	Output level depends on V_{CC1} voltage
4	GND	GND	Device GND
5	DIR	DIR	The GND (low-level) determines B-port to A-port direction
6	B2	IN2	Input threshold-value depends on V_{CC2} voltage
7	B1	IN1	Input threshold-value depends on V_{CC2} voltage
8	V_{CCB}	V_{CC2}	SYSTEM-2 supply voltage (1.65 V to 5.5 V)

Figure 2. Bidirectional Logic Level-Shifting Application

APPLICATION INFORMATION

Figure 3 shows the SN74LVC2T45 used in a bidirectional logic level-shifting application. Because the SN74LVC2T45 does not have an output enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.



The sequence in Figure 3 illustrates data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

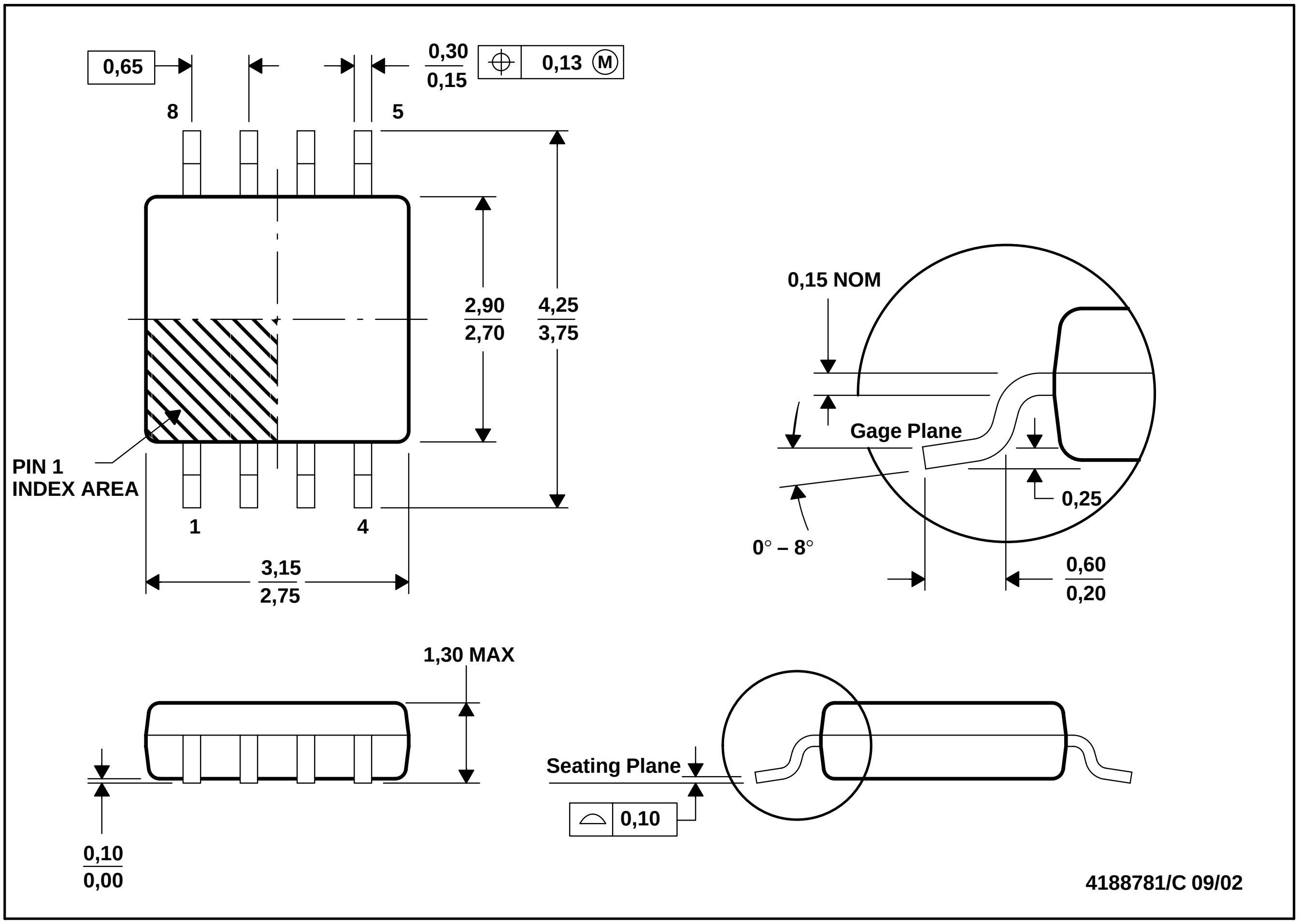
STATE	DIR CTRL	I/O 1	I/O 2	DESCRIPTION
1	H	OUT	IN	SYSTEM-1 data to SYSTEM-2
2	H	HI-Z	HI-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown.†
3	L	HI-Z	HI-Z	DIR bit is flipped. I/O-1 and I/O-2 are still disabled. The bus-line state depends on pullup or pulldown.†
4	L	OUT	IN	SYSTEM-2 data to SYSTEM-1

† SYSTEM-1 and SYSTEM-2 must use the same conditions, i.e., both pullup or both pulldown.

Figure 3. Bidirectional Logic Level-Shifting Application

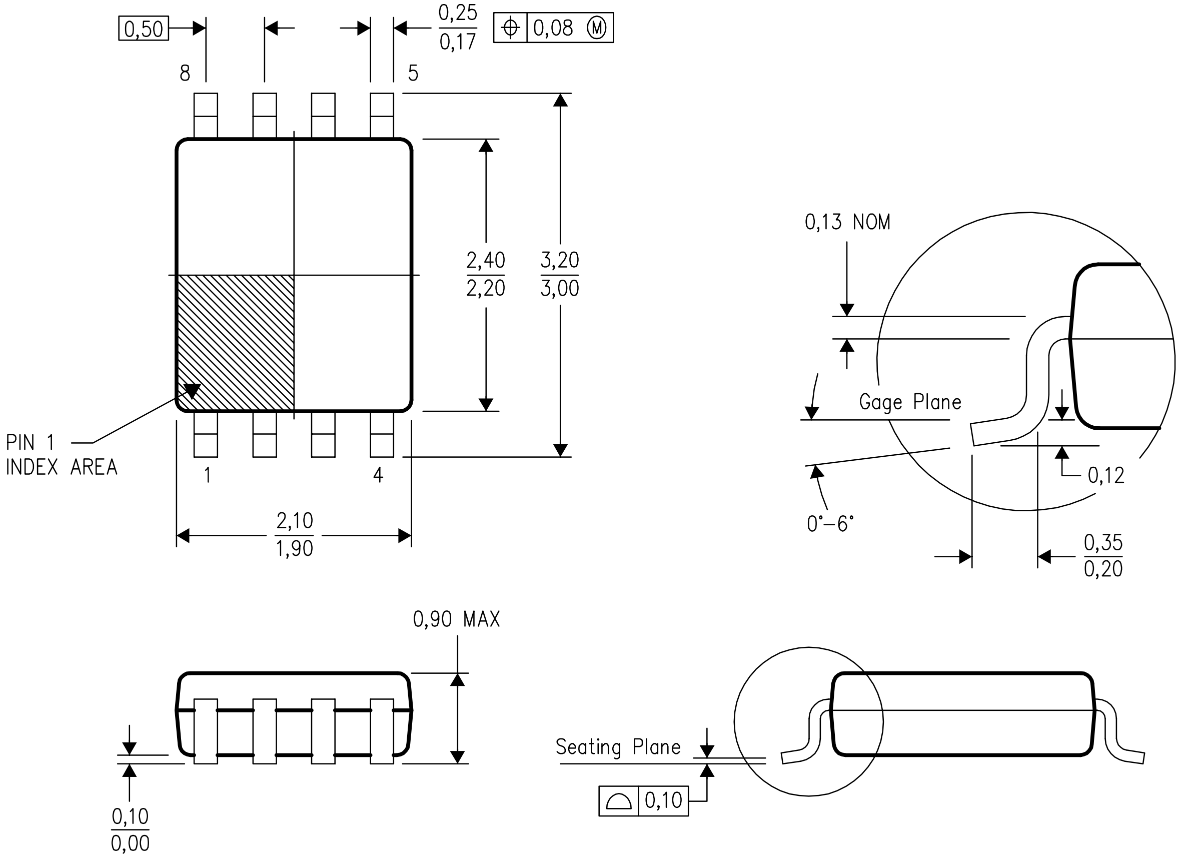
PRODUCT PREVIEW

DCT (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. Falls within JEDEC MO-187 variation DA.

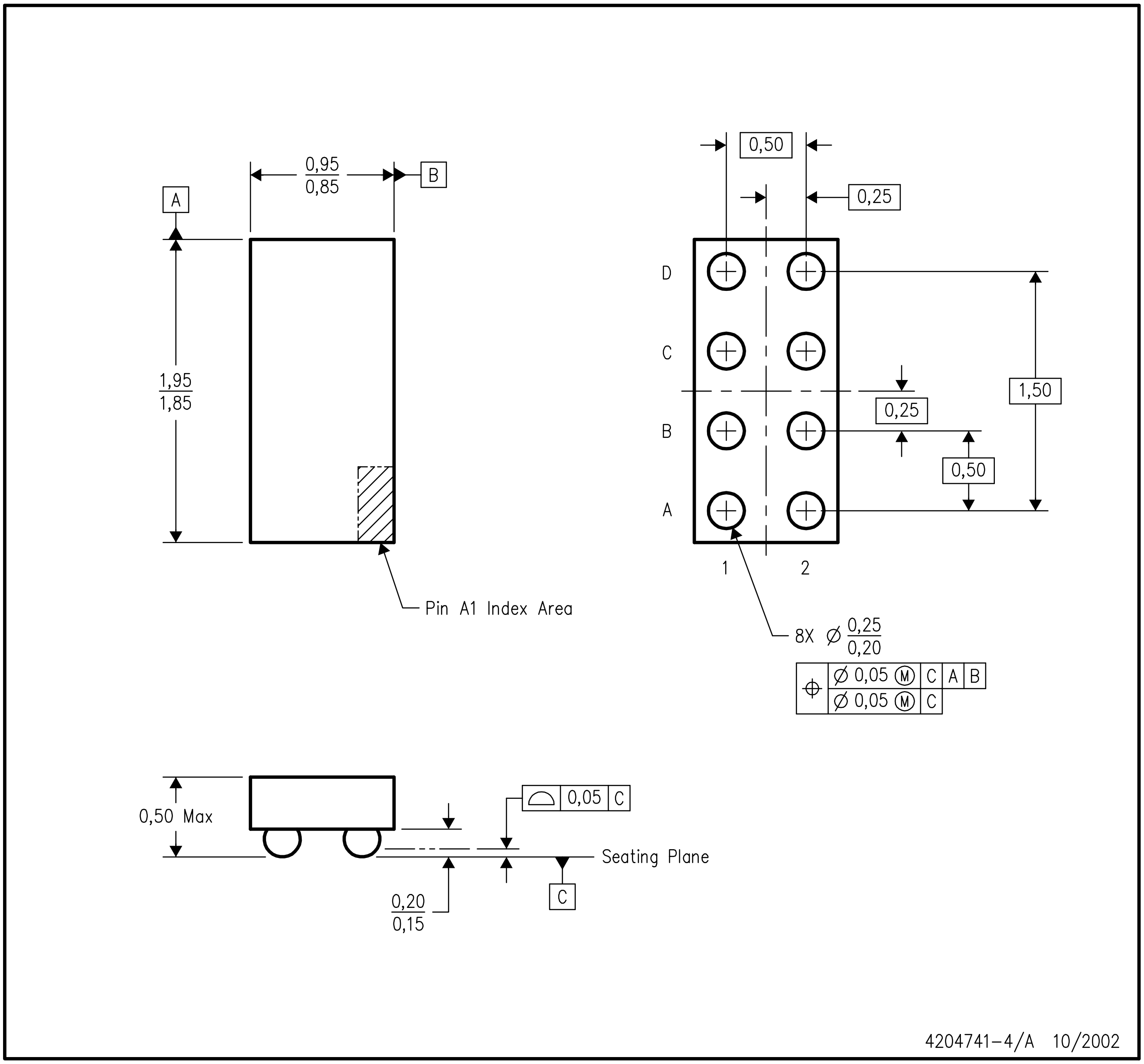
DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4200503/E 05/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO–187 variation CA.

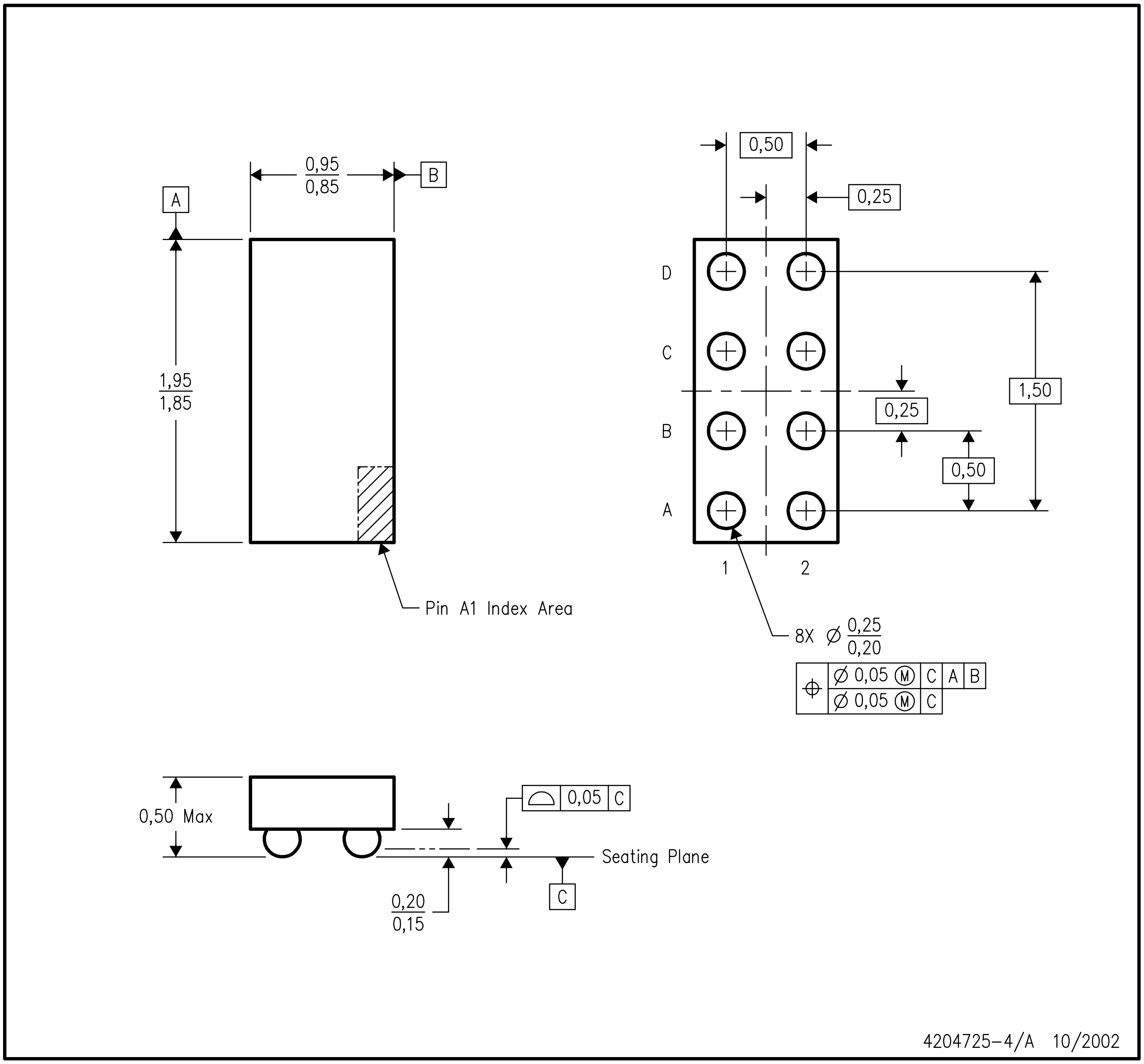
YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. This package is lead–free. Refer to the 8 YEP package (drawing 4204725) for tin–lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoStar™ package configuration.
- D. This package is tin–lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead–free.

NanoStar is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2003, Texas Instruments Incorporated