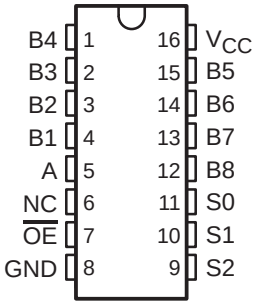
- **High-Bandwidth Data Path (Up to 500 MHz†)**
- **Equivalent To IDTQS3VH251 Device**
- **5-V Tolerant I/Os with Device Powered Up or Powered Down**
- **Low and Flat ON-State Resistance ($r_{on}$) Characteristics Over Operating Range ($r_{on}$ = 4 Ω Typical)**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V $V_{CC}$**
  - **0- to 3.3-V Switching With 2.5-V $V_{CC}$**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 3.5 pF Typical)**
- **Fast Switching Frequency ($f_{\overline{OE}}$ or $f_S$ = 20 MHz Max)**

† For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

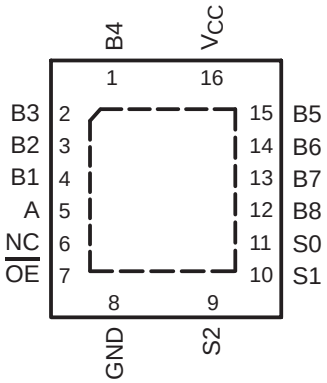
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption ($I_{CC}$ = 1 mA Typical)**
- **$V_{CC}$ Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0- to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

**DBQ, DGV, OR PW PACKAGE**
**(TOP VIEW)**




NC − No internal connection

**RGY PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## description/ordering information

The SN74CB3Q3251 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance ($r_{on}$). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3251 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

## description/ordering information (continued)

The SN74CB3Q3251 is a 1-of-8 multiplexer/demultiplexer with a single output-enable ($\overline{OE}$) input. The select (S0, S1, S2) inputs control the data path of the multiplexer/demultiplexer. When $\overline{OE}$ is low, the multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**ORDERING INFORMATION**

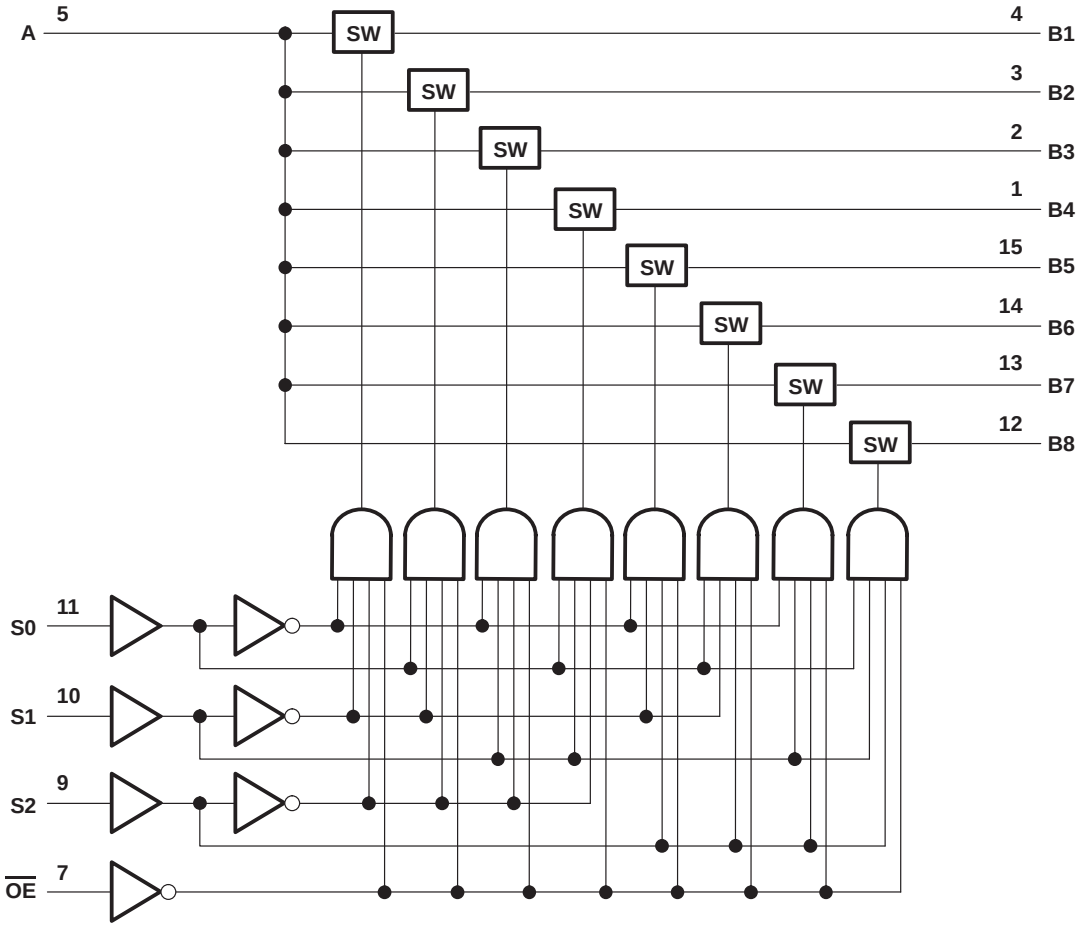
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | QFN − RGY | Tape and reel | SN74CB3Q3251RGYR | BU251 |
| | SSOP (QSOP) − DBQ | Tape and reel | SN74CB3Q3251DBQR | BU251 |
| | TSSOP − PW | Tube | SN74CB3Q3251PW | BU251 |
| | | Tape and reel | SN74CB3Q3251PWR | |
| | TVSOP − DGV | Tape and reel | SN74CB3Q3251DGVR | BU251 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

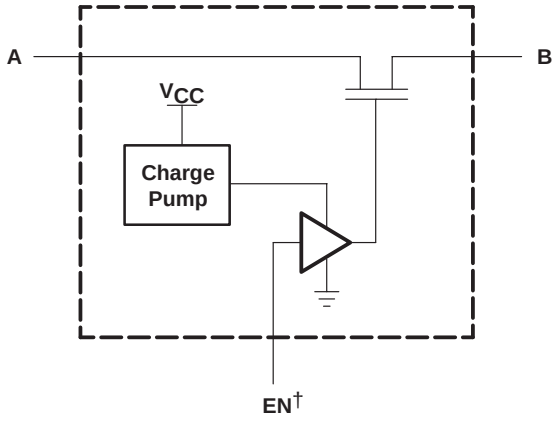
**FUNCTION TABLE**

| INPUTS | | | | INPUT/OUTPUT A | FUNCTION |
|---|---|---|---|---|---|
| $\overline{OE}$ | S2 | S1 | S0 | | |
| L | L | L | L | B1 | A port = B1 port |
| L | L | L | H | B2 | A port = B2 port |
| L | L | H | L | B3 | A port = B3 port |
| L | L | H | H | B4 | A port = B4 port |
| L | H | L | L | B5 | A port = B5 port |
| L | H | L | H | B6 | A port = B6 port |
| L | H | H | L | B7 | A port = B7 port |
| L | H | H | H | B8 | A port = B8 port |
| H | X | X | X | Z | Disconnect |

## logic diagram (positive logic)




## simplified schematic, each FET switch (SW)




† EN is the internal enable signal applied to the switch.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 4.6 V
Control input voltage range, $V_{IN}$ (see Notes 1 and 2) . . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . . −0.5 V to 7 V
Control input clamp current, $I_{IK}$ ($V_{IN}$ < 0) . . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O}$ < 0) . . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . . ±64 mA
Continuous current through $V_{CC}$ or GND terminals . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 5): DBQ package . . . . . 90°C/W
(see Note 5): DGV package . . . . . 120°C/W
(see Note 5): PW package . . . . . 108°C/W
(see Note 6): RGY package . . . . . 39°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. $V_I$ and $V_O$ are used to denote specific conditions for $V_{I/O}$.
4. $I_I$ and $I_O$ are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

### recommended operating conditions (see Note 7)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_{IH}$ | High-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | 5.5 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | 5.5 | |
| $V_{IL}$ | Low-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 0 | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 0 | 0.8 | |
| $V_{I/O}$ | Data input/output voltage | | 0 | 5.5 | V |
| $T_A$ | Operating free-air temperature | | −40 | 85 | °C |

NOTE 7: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 3.6 V, | $I_I$ = −18 mA | | | | −1.8 | V |
| $I_{IN}$ | Control inputs | $V_{CC}$ = 3.6 V, | $V_{IN}$ = 0 to 5.5 V | | | | ±1 | µA |
| $I_{OZ}$‡ | | $V_{CC}$ = 3.6 V, | $V_O$ = 0 to 5.5 V, $V_I$ = 0, | Switch OFF, $V_{IN}$ = $V_{CC}$ or GND | | | ±1 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_O$ = 0 to 5.5 V, | $V_I$ = 0 | | | 1 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, | $I_{I/O}$ = 0, Switch ON or OFF, | $V_{IN}$ = $V_{CC}$ or GND | | 1 | 4 | mA |
| $\Delta I_{CC}$§ | Control inputs | $V_{CC}$ = 3.6 V, | One input at 3 V, | Other inputs at $V_{CC}$ or GND | | | 30 | µA |
| $I_{CCD}$¶ | Per control input | $V_{CC}$ = 3.6 V, | A and B ports open, | Control input switching at 50% duty cycle | | 0.03 | 0.1 | mA/ MHz |
| $C_{in}$ | Control inputs | $V_{CC}$ = 3.3 V, | $V_{IN}$ = 5.5 V, 3.3 V, or 0 | | | 2.5 | 4.5 | pF |
| $C_{io(OFF)}$ | A port | $V_{CC}$ = 3.3 V, | Switch OFF, $V_{IN}$ = $V_{CC}$ or GND, | $V_{I/O}$ = 5.5 V, 3.3 V, or 0 | | 19.5 | 25 | pF |
| | B port | $V_{CC}$ = 3.3 V, | Switch OFF, $V_{IN}$ = $V_{CC}$ or GND, | $V_{I/O}$ = 5.5 V, 3.3 V, or 0 | | 3.5 | 4.5 | pF |
| $C_{io(ON)}$ | | $V_{CC}$ = 3.3 V, | Switch ON, $V_{IN}$ = $V_{CC}$ or GND, | $V_{I/O}$ = 5.5 V, 3.3 V, or 0 | | 15 | 19 | pF |
| $r_{on}$# | | $V_{CC}$ = 2.3 V, TYP at $V_{CC}$ = 2.5 V | $V_I$ = 0, | $I_O$ = 30 mA | | 4 | 10 | Ω |
| | | | $V_I$ = 1.7 V, | $I_O$ = −15 mA | | 4.5 | 11 | |
| | | $V_{CC}$ = 3 V | $V_I$ = 0, | $I_O$ = 30 mA | | 3.5 | 8 | |
| | | | $V_I$ = 2.4 V, | $I_O$ = −15 mA | | 4 | 10 | |

$V_{IN}$ and $I_{IN}$ refer to control inputs. $V_I$, $V_O$, $I_I$, and $I_O$ refer to data pins.
† All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.
‡ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.
¶ This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).
# Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{\overline{OE}}$ or $f_S$‖ | $\overline{OE}$ or S | A or B | | 10 | | 20 | MHz |
| $t_{pd}$☆ | A or B | B or A | | 0.12 | | 0.18 | ns |
| $t_{pd(s)}$ | S | A | 1.5 | 6.7 | 1.5 | 5.9 | ns |
| $t_{en}$ | S | B | 1.5 | 6.7 | 1.5 | 5.9 | ns |
| | $\overline{OE}$ | A or B | 1.5 | 6.7 | 1.5 | 5.9 | |
| $t_{dis}$ | S | B | 0.5 | 6.1 | 0.5 | 6.1 | ns |
| | $\overline{OE}$ | A or B | 0.5 | 6.1 | 0.5 | 6.1 | |

‖ Maximum switching frequency for control input ($V_O$ > $V_{CC}$, $V_I$ = 5 V, $R_L$ ≥ 1 MΩ, $C_L$ = 0).
☆ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

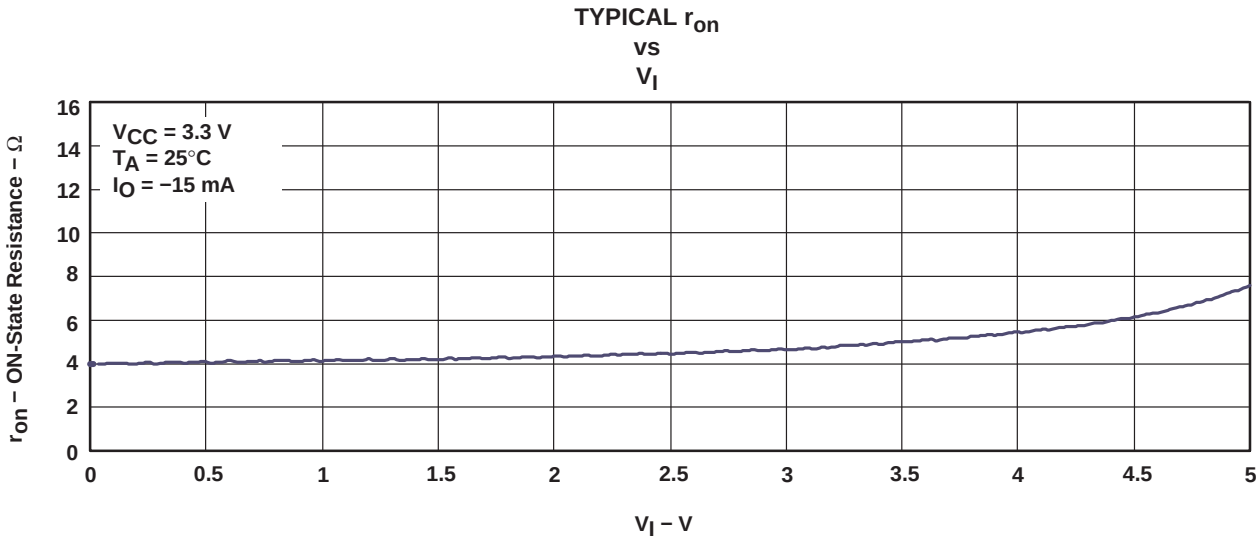



Figure 1. Typical $r_{on}$ vs $V_I$, $V_{CC}$ = 3.3 V and $I_O$ = −15 mA

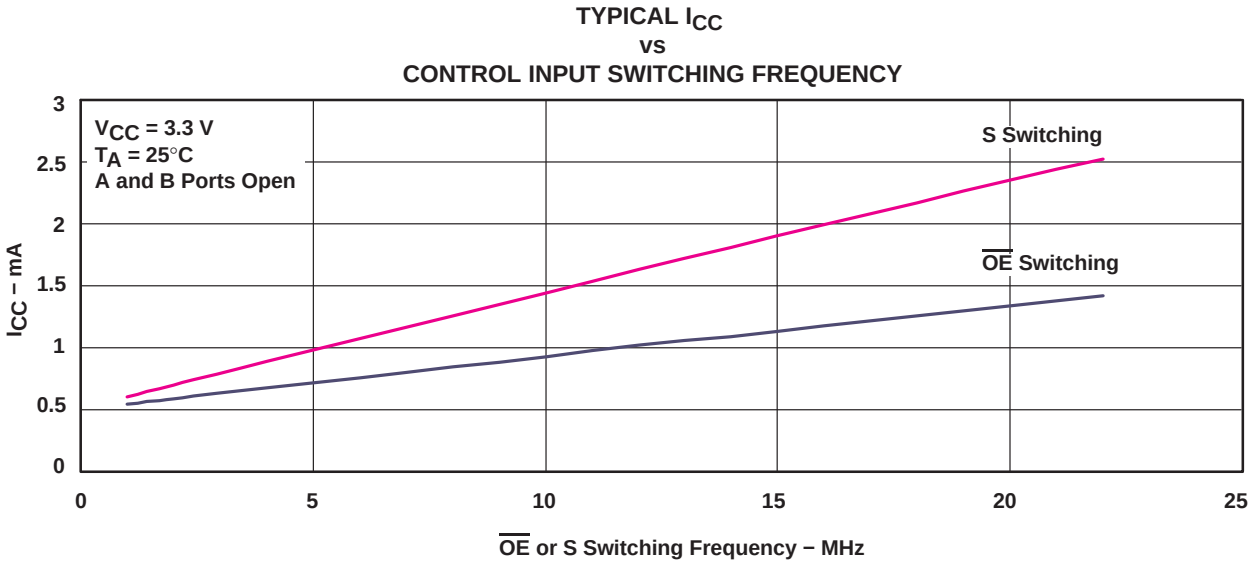
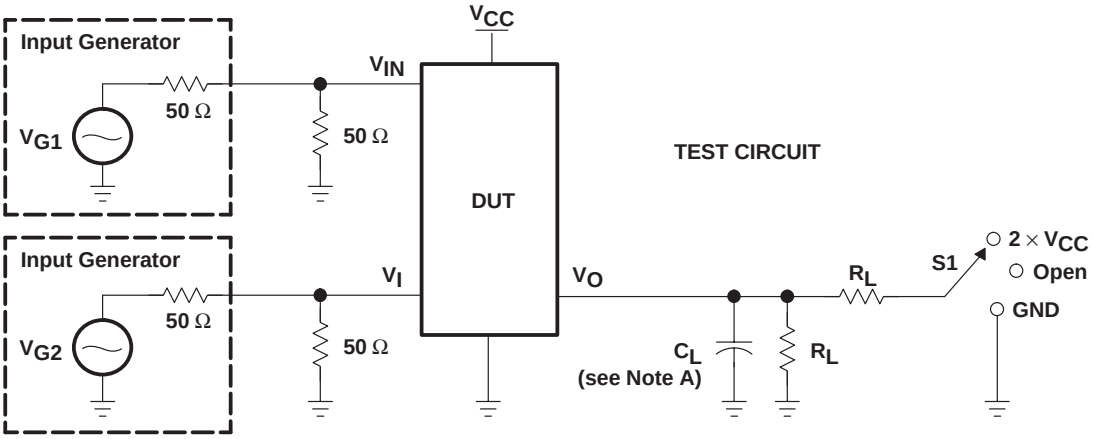
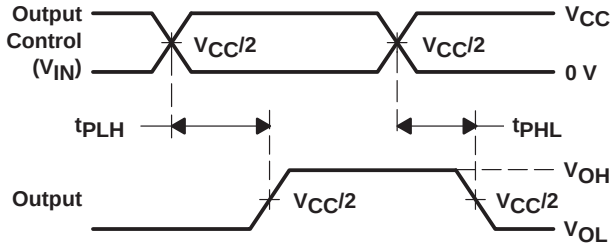



Figure 2. Typical $I_{CC}$ vs $\overline{OE}$ or S Switching Frequency, $V_{CC}$ = 3.3 V

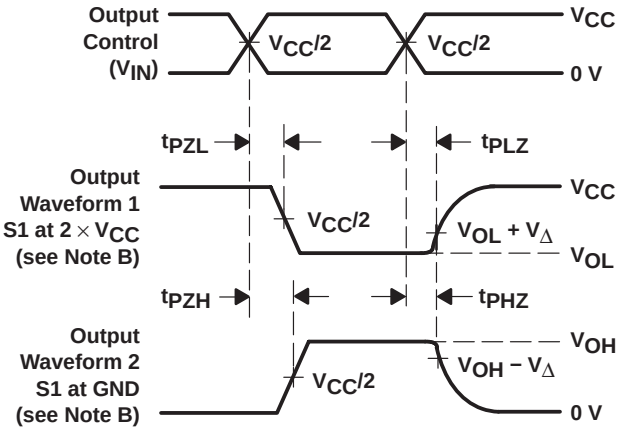
## PARAMETER MEASUREMENT INFORMATION




| TEST | $V_{CC}$ | S1 | $R_L$ | $V_I$ | $C_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|
| $t_{pd(s)}$ | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | Open<br>Open | 500 Ω<br>500 Ω | $V_{CC}$ or GND<br>$V_{CC}$ or GND | 30 pF<br>50 pF | |
| $t_{PLZ}/t_{PZL}$ | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | 2 × $V_{CC}$<br>2 × $V_{CC}$ | 500 Ω<br>500 Ω | GND<br>GND | 30 pF<br>50 pF | 0.15 V<br>0.3 V |
| $t_{PHZ}/t_{PZH}$ | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | GND<br>GND | 500 Ω<br>500 Ω | $V_{CC}$<br>$V_{CC}$ | 30 pF<br>50 pF | 0.15 V<br>0.3 V |




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



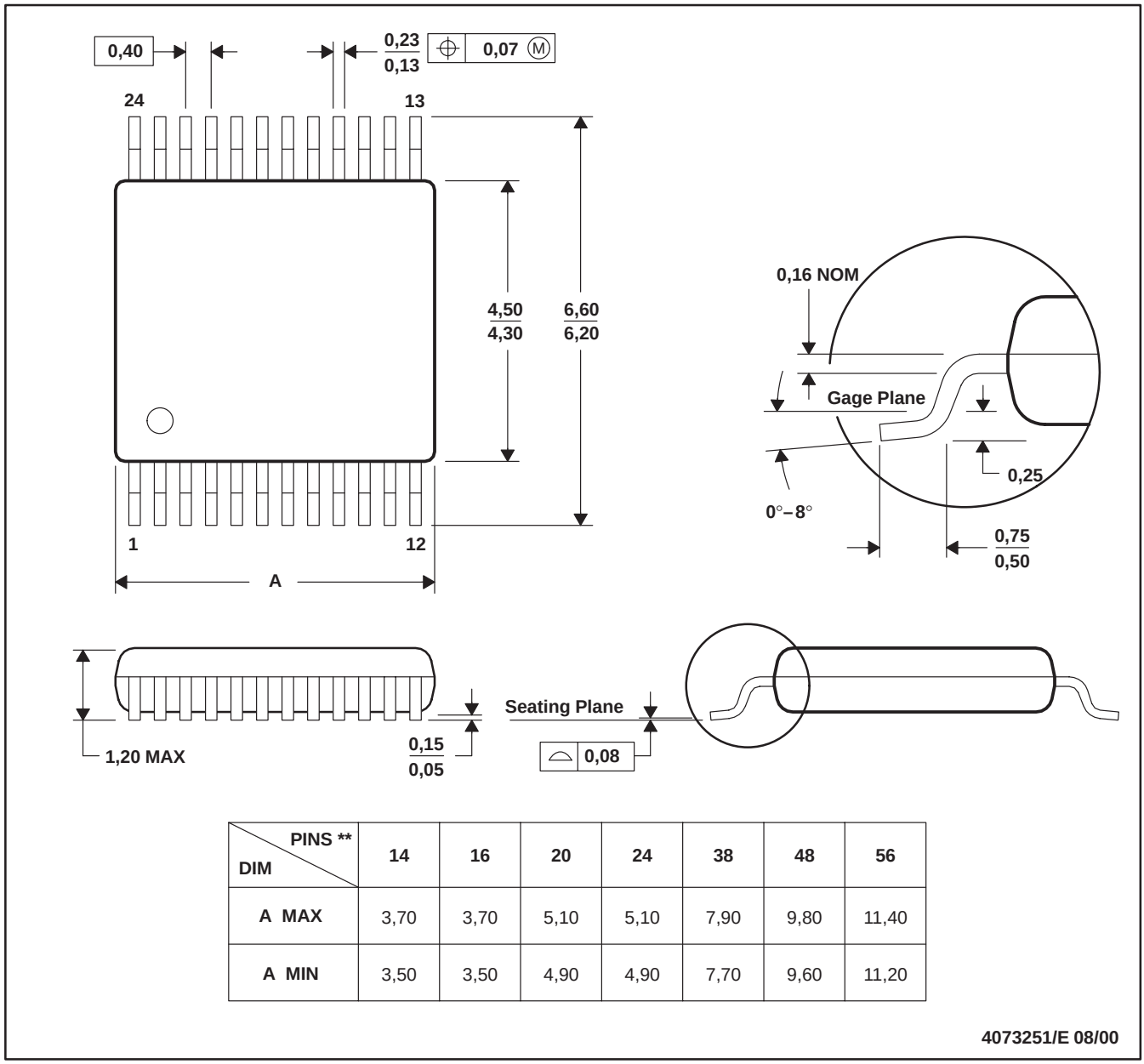

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Test Circuit and Voltage Waveforms**

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

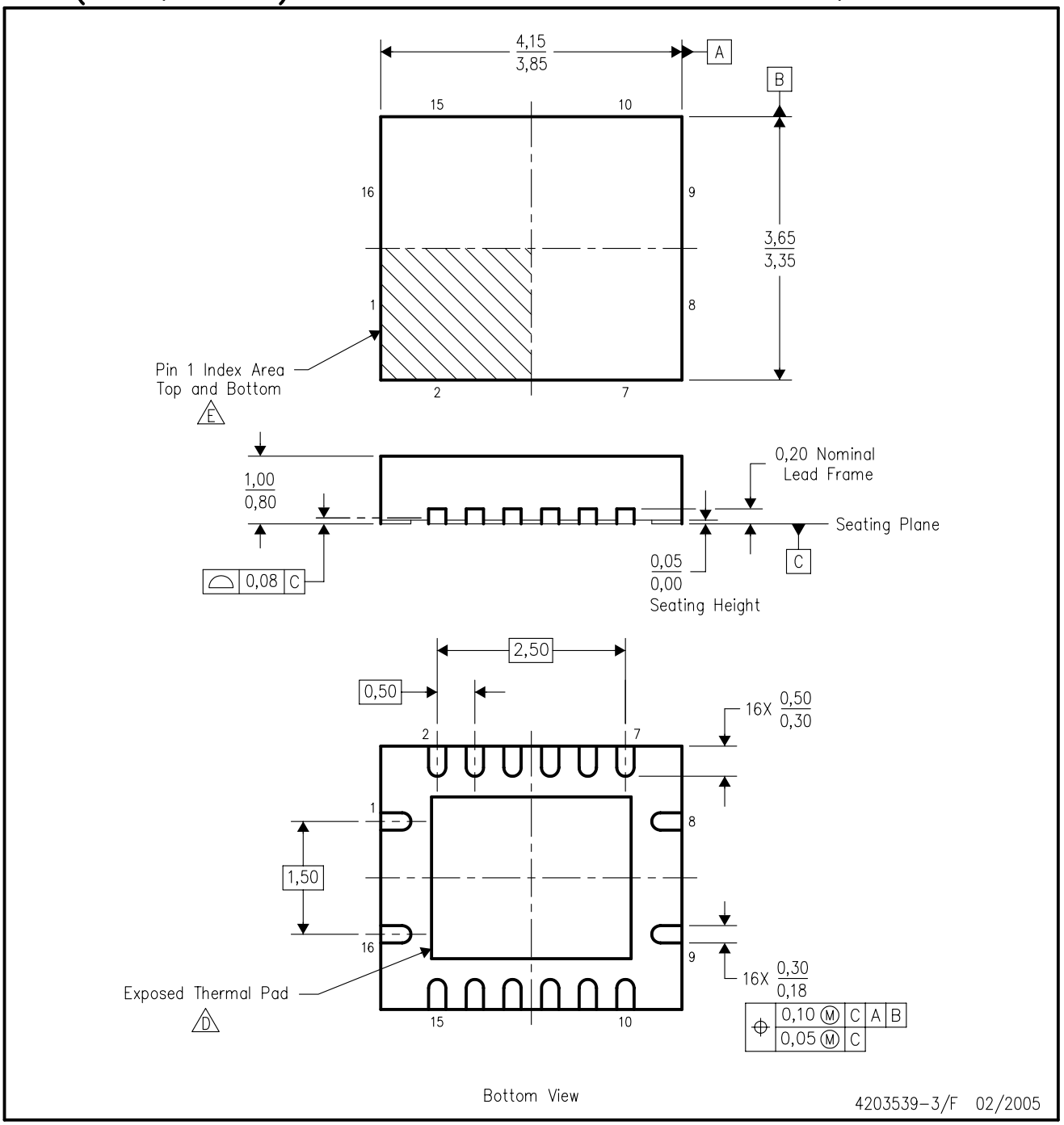



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

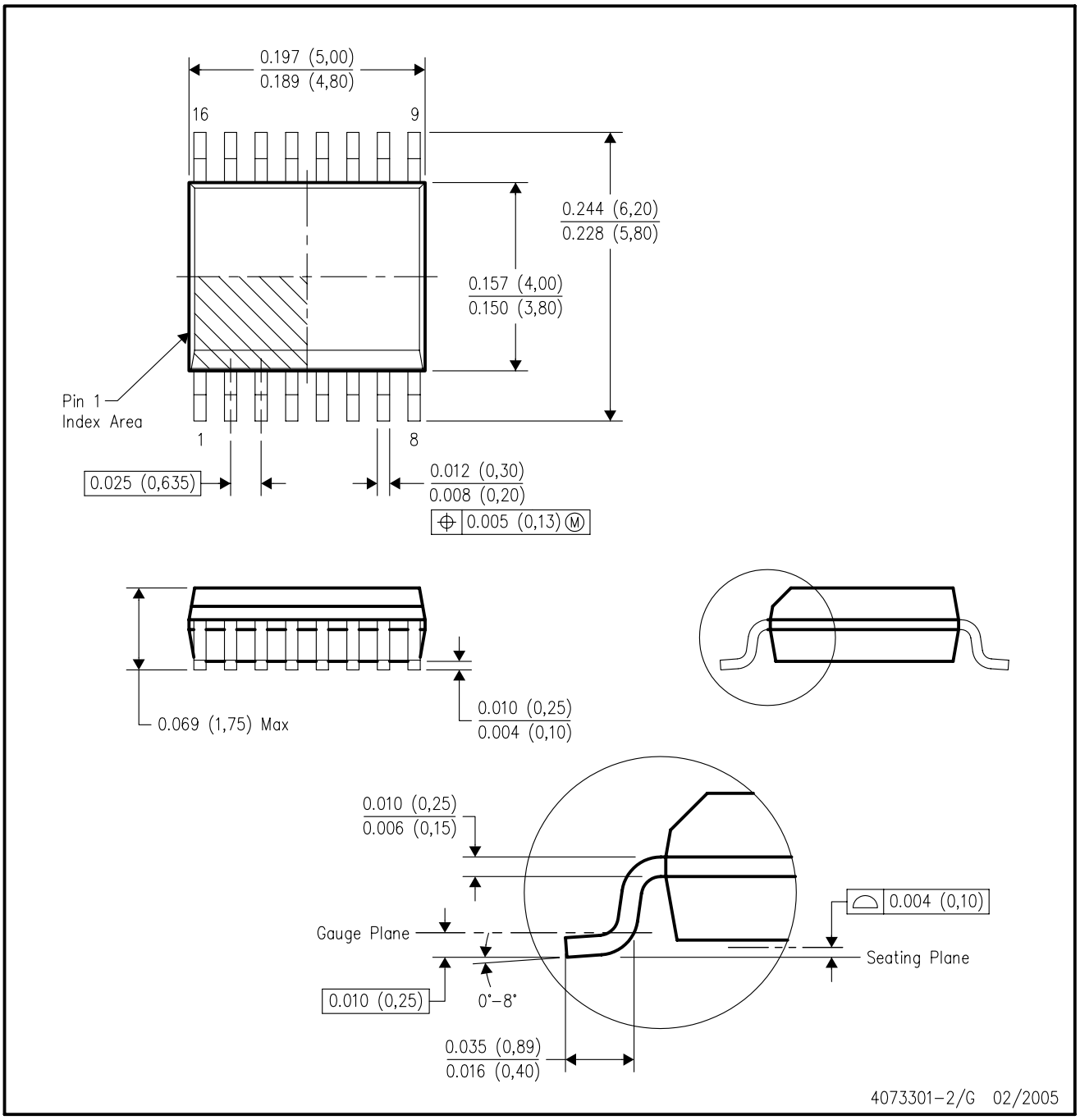
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

RGY (R–PQFP–N16) PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BB.

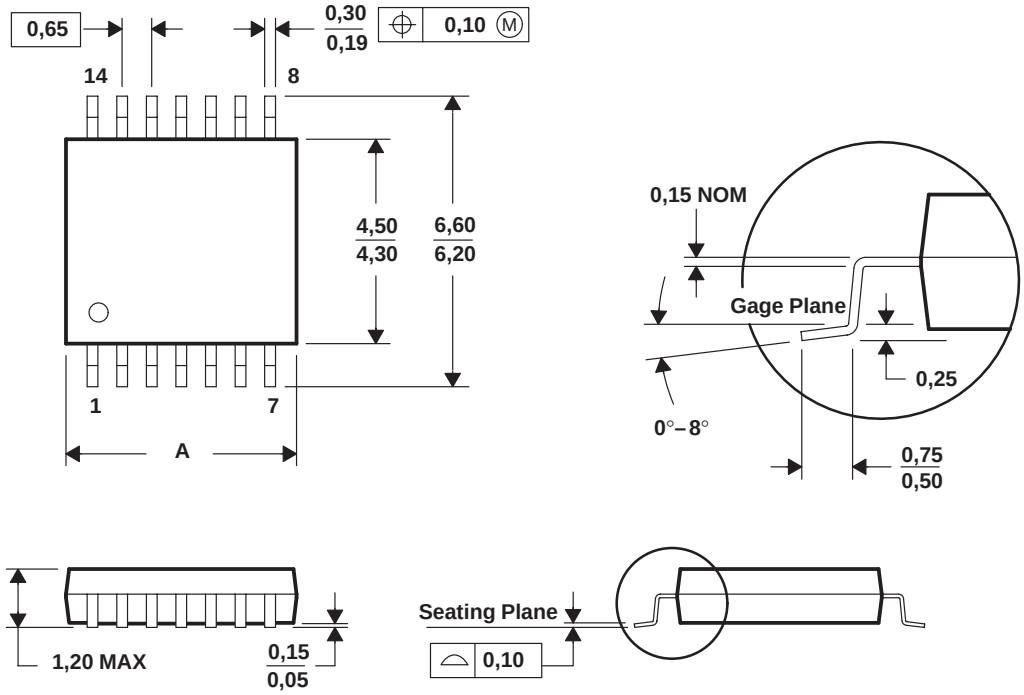
## DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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