

- **Organization:**
 - TM8TT64JPN . . . 8388608 × 64 Bits
 - TM16TT64JPN . . . 16777216 × 64 Bits
 - TM8TT72JPN . . . 8388608 × 72 Bits
 - TM16TT72JPN . . . 16777216 × 72 Bits
- Designed for 100-MHz 4-Clock Systems
- JEDEC 168-Pin Dual-In-Line Memory Module (DIMM) Without Buffer for Use With Socket
- TM8TT64JPN — Uses Eight 64M-Bit Synchronous Dynamic RAMs (SDRAMs) (8M × 8-Bit) in Plastic Thin Small-Outline Packages (TSOPs)
- TM16TT64JPN — Uses Sixteen 64M-Bit SDRAMs (8M × 8-Bit) in Plastic TSOPs
- TM8TT72JPN — Uses Nine 64M-Bit SDRAMs (8M × 8-Bit) in Plastic TSOPs
- TM16TT72JPN — Uses Eighteen 64M-Bit SDRAMs (8M × 8-Bit) in Plastic TSOPs
- **Performance Ranges:**
 - Single 3.3-V Power Supply (±10% Tolerance)
 - Byte-Read/Write Capability
 - High-Speed, Low-Noise Low-Voltage TTL (LVTTTL) Interface
 - Read Latencies 2 and 3 Supported
 - Supports Burst-Interleave and Burst-Interrupt Operations
 - Burst Length Programmable to 1, 2, 4, and 8
 - Four Banks for On-Chip Interleaving (Gapless Access)
 - Ambient Temperature Range 0°C to 70°C
 - Gold-Plated Contacts
 - Pipeline Architecture
 - Serial Presence-Detect (SPD) Using EEPROM

	SYNCHRONOUS CLOCK CYCLE TIME		ACCESS TIME CLOCK TO OUTPUT		REFRESH INTERVAL
	t _{CK3}	t _{CK2}	t _{AC3}	t _{AC2}	t _{REF}
'xTTxxJPN-8	8 ns	10 ns	6 ns	6 ns	64 ms
'xTTxxJPN-8A	8 ns	10 ns	6 ns	7.5 ns	64 ms

description

The TM8TT64JPN is a 64M-byte, 168-pin dual-in-line memory module (DIMM). The DIMM is composed of eight TMS664814ADGE, 8388608 × 8-bit SDRAMs, each in a 400-mil, 54-pin plastic thin small-outline package (TSOP) mounted on a substrate with decoupling capacitors. See the TMS664814 data sheet (literature number SMOS695).

The TM16TT64JPN is a 128M-byte, 168-pin DIMM. The DIMM is composed of sixteen TMS664814ADGE, 8388608 × 8-bit SDRAMs, each in a 400-mil, 54-pin plastic TSOP mounted on a substrate with decoupling capacitors. See the TMS664814 data sheet (literature number SMOS695).

The TM8TT72JPN is a 64M-byte, 168-pin DIMM. The DIMM is composed of nine TMS664814ADGE, 8388608 × 8-bit SDRAMs, each in a 400-mil, 54-pin plastic thin small-outline package (TSOP) mounted on a substrate with decoupling capacitors. See the TMS664814 data sheet (literature number SMOS695).

The TM16TT72JPN is a 128M-byte, 168-pin DIMM. The DIMM is composed of eighteen TMS664814ADGE, 2097152 × 8-bit SDRAMs, each in a 400-mil, 54-pin plastic TSOP mounted on a substrate with decoupling capacitors. See the TMS664814 data sheet (literature number SMOS695).



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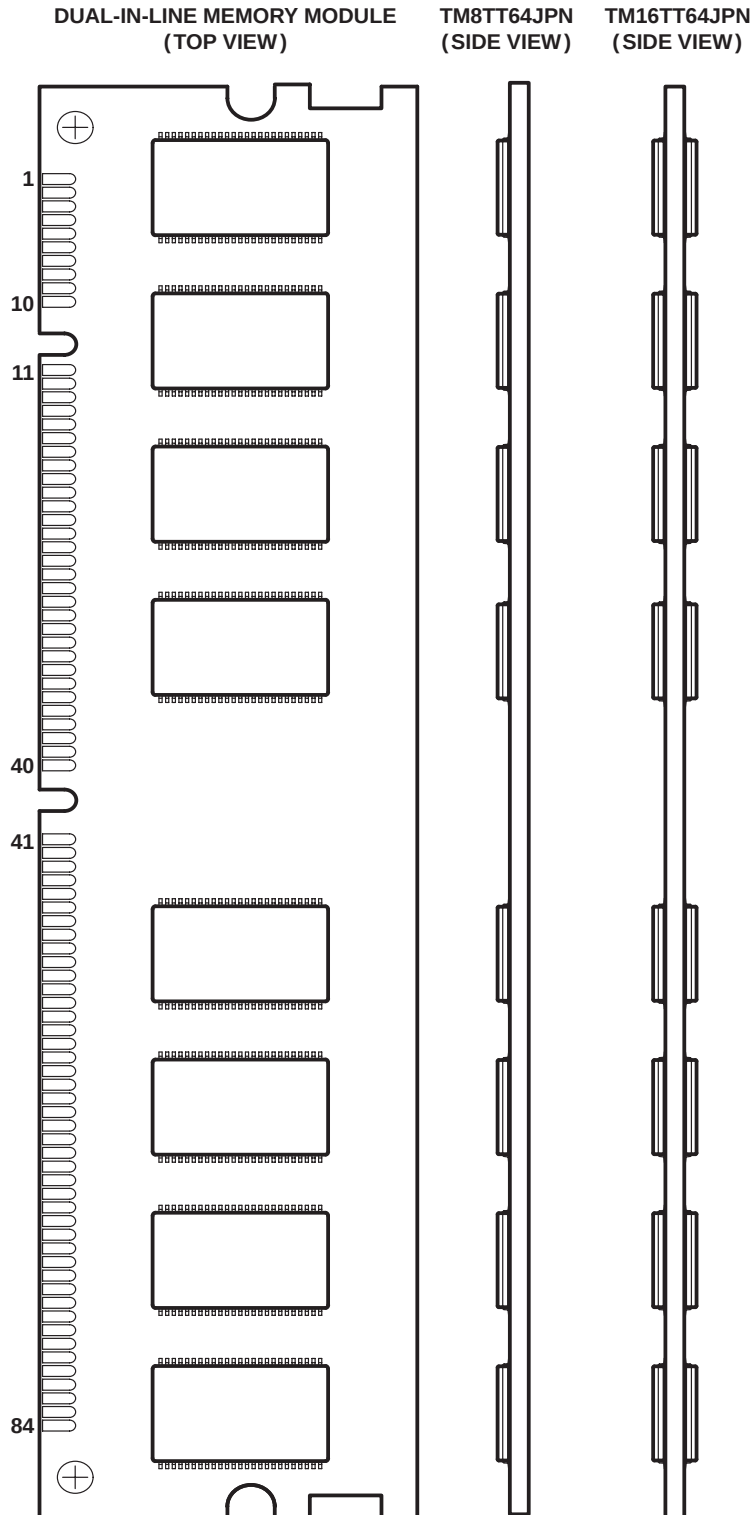
operation

The TM8TT64JPN operates as eight TMS664814DGE devices that are connected as shown in the TM8TT64JPN functional block diagram. The TM16TT64JPN operates as 16 TMS664814ADGE devices connected as shown in the TM16TT64JPN functional block diagram. The TM8TT72JPN operates as nine TMS664814ADGE devices that are connected as shown in the TM8TT72JPN functional block diagram. The TM16TT72JPN operates as 18 TMS664814ADGE devices connected as shown in the TM16TT72JPN functional block diagram.

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PIN NOMENCLATURE

A[0:11]	Row Address Inputs
A[0:8]	Column Address Inputs
A13/BA0	Bank-Select Zero
A12/BA1	Bank-Select One
$\overline{\text{CAS}}$	Column-Address Strobe
CB[0:7]	Check Bit In/Check Bit Out
CKE[0:1]	Clock Enable
CK[0:3]	System Clock
DQ[0:63]	Data-In/Data-Out
DQMB[0:7]	Data-In/Data-Out Mask Enable
NC	No Connect
$\overline{\text{RAS}}$	Row-Address Strobe
S[0:3]	Chip-Select
SA[0:2]	Serial Presence-Detect (SPD) Device Address Input
SCL	SPD Clock
SDA	SPD Address/Data
V _{DD}	3.3-V Supply
V _{SS}	Ground
WE	Write Enable
WP	Write Protect

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Pin Assignments

PIN		PIN		PIN		PIN	
NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME
1	V _{SS}	43	V _{SS}	85	V _{SS}	127	V _{SS}
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	$\overline{S2}$	87	DQ33	129	$\overline{S3}$
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V _{DD}	48	NC	90	V _{DD}	132	NC
7	DQ4	49	V _{DD}	91	DQ36	133	V _{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V _{DD}	101	DQ45	143	V _{DD}
18	V _{DD}	60	DQ20	102	V _{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	NC
22	CB1	64	V _{SS}	106	CB5	148	V _{SS}
23	V _{SS}	65	DQ21	107	V _{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V _{DD}	68	V _{SS}	110	V _{DD}	152	V _{SS}
27	$\overline{WE}$	69	DQ24	111	$\overline{CAS}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	$\overline{S0}$	72	DQ27	114	$\overline{S1}$	156	DQ59
31	NC	73	V _{DD}	115	$\overline{RAS}$	157	V _{DD}
32	V _{SS}	74	DQ28	116	V _{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	A13/BA0	164	NC
39	A12/BA1	81	WP	123	A11	165	SA0
40	V _{DD}	82	SDA	124	V _{DD}	166	SA1
41	V _{DD}	83	SCL	125	CK1	167	SA2
42	CK0	84	V _{DD}	126	NC	168	V _{DD}



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The diagram illustrates the connection of SDRAM and SPD EEPROM to the processor. SDRAM (U0-U8) is connected via CS, DQM, and DQ signals. SPD EEPROM (U9) is connected via SCL, WP, and SDA signals. Component values are specified: R = 10 Ω, R_B = 5 Ω, R_C = 10 Ω, C = 10 pF.

SDRAM Connections:

- U0, U4:** CS to $\overline{S0}$; DQM to DQMB0; DQ[0:7] to DQ[0:7] (via R).
- U1, U5:** CS to $\overline{S0}$; DQM to DQMB1; DQ[0:7] to DQ[0:7] (via R).
- U2, U6:** CS to $\overline{S2}$; DQM to DQMB2; DQ[0:7] to DQ[0:7] (via R).
- U3, U7:** CS to $\overline{S2}$; DQM to DQMB3; DQ[0:7] to DQ[0:7] (via R).
- U8:** CS to $\overline{S0}$; DQM to DQMB1; DQ[0:7] to DQ[0:7] (via R).
- U9:** CS to $\overline{S0}$; DQM to DQMB4; DQ[0:7] to DQ[0:7] (via R).

SPD EEPROM Connections:

- SCL:** Connected to WP.
- WP:** Connected to SCL.
- SDA:** Connected to SDA.
- SA0, SA1, SA2:** Connected to SDA.
- 47 kΩ:** Pull-up resistor for SCL.

Component Values:

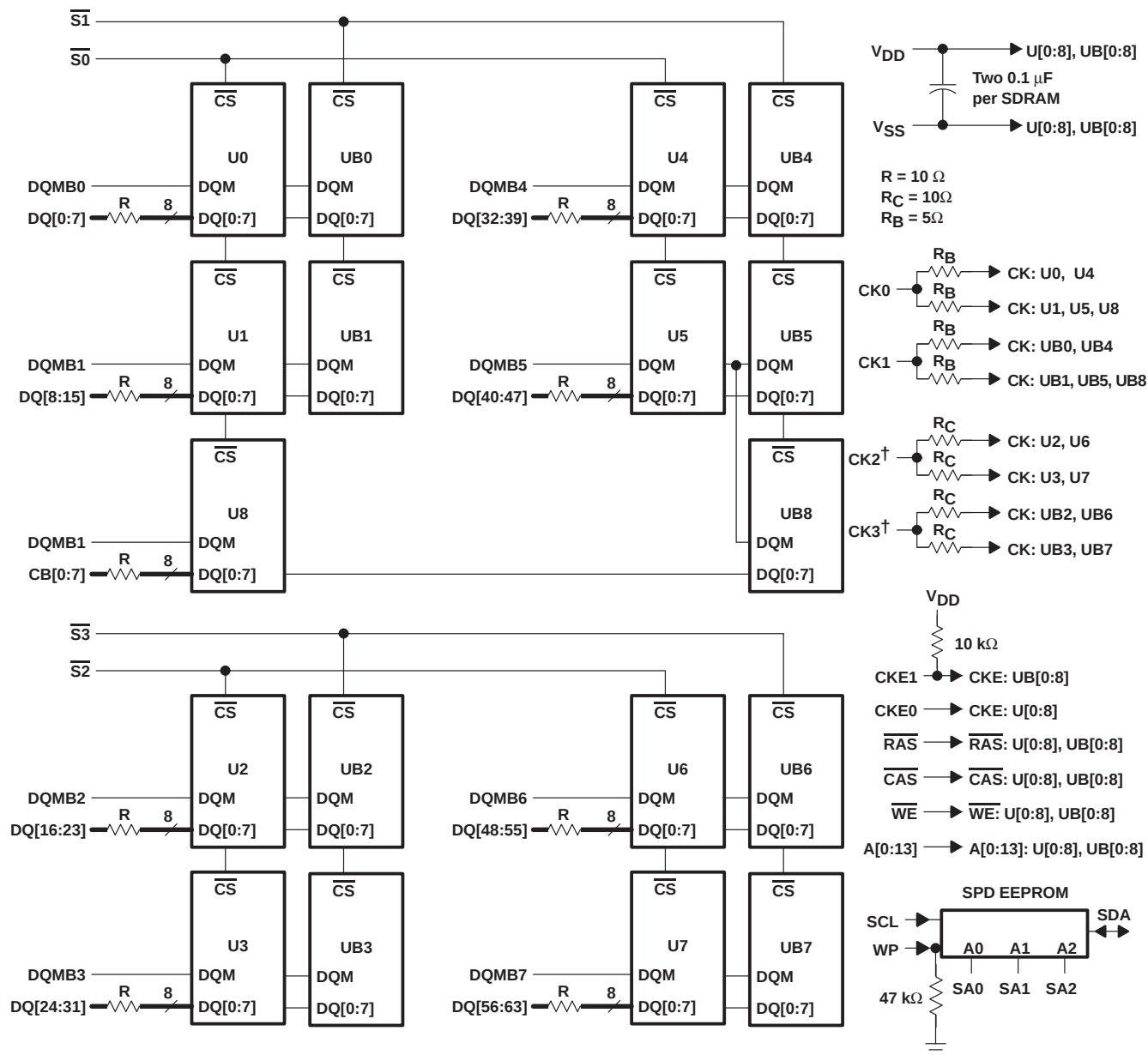
- R = 10 Ω
- R_B = 5 Ω
- R_C = 10 Ω
- C = 10 pF

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functional block diagram for the TM16TT72JPN



[†] Additional 3.3 pF capacity is used to balance loads among clocks.

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absolute maximum ratings over ambient temperature range (unless otherwise noted)[†]

Supply voltage range, V_{DD}	–0.5 V to 4.6 V
Voltage range on any pin (see Note 1)	– 0.5 V to 4.6 V
Short-circuit output current	50 mA
Power dissipation: TM8TT64JPN	8 W
TM16TT64JPN	16 W
TM8TT72JPN	9 W
TM16TT72JPN	18 W
Ambient temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	– 55°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{DD} Supply voltage	3	3.3	3.6	V
V_{SS} Supply voltage		0		V
V_{IH} High-level input voltage	2		$V_{DD} + 0.3$	V
V_{IH-SPD} High-level input voltage for SPD device	2		5.5	V
V_{IL} Low-level input voltage	–0.3		0.8	V
T_A Ambient temperature	0		70	°C

capacitance over recommended ranges of supply voltage and ambient temperature, $f = 1$ MHz (see Note 2)[‡]

PARAMETER	'xTTxxJPN		UNIT
	MIN	MAX	
$C_i(CK)$ Input capacitance, CK input	2.5	4	pF
$C_i(AC)$ Input capacitance, address and control inputs: A0–A13, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.5	5	pF
$C_i(CKE)$ Input capacitance, CKE input		5	pF
C_o Output capacitance	4	6.5	pF
$C_i(DQMBx)$ Input capacitance, DQMBx input	2.5	5	pF
$C_i(Sx)$ Input capacitance, $\overline{Sx}$ input	2.5	5	pF
$C_{i/o}(SDA)$ SDA Input/output capacitance		9	pF
$C_i(SPD)$ Input capacitance, SA0, SA1, SA2, SCL inputs		7	pF

[‡] Specifications in this table represent a single SDRAM device.

NOTE 2: $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$. Bias on pins under test is 0 V.

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electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)[†]

TMxTTxxJPN

PARAMETER		TEST CONDITIONS		'xTTxxJPN-8		'xTTxxJPN-8A		UNIT
				MIN	MAX	MIN	MAX	
V _{OH}	High-level output voltage	I _{OH} = − 2 mA		2.4		2.4		V
V _{OL}	Low-level output voltage	I _{OL} = 2 mA		0.4		0.4		V
I _I	Input current (leakage)	0 V ≤ V _I ≤ V _{DD} + 0.3 V, All other pins = 0 V to V _{DD}		± 10		± 10		μA
I _O	Output current (leakage)	0 V ≤ V _O ≤ V _{DD} + 0.3 V, Output disabled		± 10		± 10		μA
I _{CC1}	Operating current	Burst length = 1, t _{RC} ≥ t _{RC} MIN, I _{OH} /I _{OL} = 0 mA (See Notes 4, 5, and 6)	CAS latency = 2	115		95		mA
			CAS latency = 3	125		95		mA
I _{CC2P}	Precharge standby current in power-down mode	CKE ≤ V _{IL} MAX, t _{CK} = 15 ns (see Note 7)		1		1		mA
I _{CC2PS}		CKE and CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Note 8)		1		1		mA
I _{CC2N}	Active standby current in non-power-down mode	CKE ≥ V _{IH} MIN, t _{CK} = 15 ns (see Note 7)		40		40		mA
I _{CC2NS}		t _{CK} = ∞ (see Note 8)		5		5		mA
I _{CC3P}	Active standby current in power-down mode	CKE ≤ V _{IL} MAX, t _{CK} = 15 ns (see Notes 4 and 7)		8		8		mA
I _{CC3PS}		CKE and CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Notes 4 and 8)		8		8		mA
I _{CC3N}	Precharge standby current in non-power-down mode	CKE ≥ V _{IH} MIN, t _{CK} = 15 ns (see Notes 4 and 7)		50		50		mA
I _{CC3NS}		CKE ≥ V _{IH} MIN, CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Notes 4 and 8)		15		15		mA
I _{CC4}	Burst current	Page burst, I _{OH} /I _{OL} = 0 mA All banks activated, n _{CCD} = one cycle (see Notes 9 and 10)	CAS latency = 2	165		120		mA
			CAS latency = 3	225		165		mA
I _{CC5}	Auto-refresh current	t _{RC} ≤ t _{RC} MIN (see Notes 5 and 8)	CAS latency = 2	150		150		mA
			CAS latency = 3	150		150		mA
I _{CC6}	Self-refresh current	CKE ≤ V _{IL} MAX		1		1		mA

[†] Specifications in this table represent a single SDRAM device.

NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.

4. Only one bank is activated.

5. t_{RC} ≥ t_{RC} MIN

6. Control and address inputs change state twice during t_{RC}.

7. Control and address inputs change state once every 30 ns.

8. Control and address inputs do not change state (stable).

9. Control and address inputs change once every cycle.

10. Continuous burst access, n_{CCD} = 1 cycle



ac timing requirements^{†‡}

			'xTTxxJPN-8		'xxTTxxJPN-8A		UNIT
			MIN	MAX	MIN	MAX	
t _{CK2}	Cycle time, CK	CAS latency = 2	10		15		ns
t _{CK3}	Cycle time, CK	CAS latency = 3	8		8		ns
t _{CH}	Pulse duration, CK high		3		3		ns
t _{CL}	Pulse duration, CK low		3		3		ns
t _{AC2}	Access time, CK high to data out (see Note 11)	CAS latency = 2		6		7.5	ns
t _{AC3}	Access time, CK high to data out (see Note 11)	CAS latency = 3		6		6	ns
t _{OH}	Hold time, CK high to data out with 50-pF load		3		3		ns
t _{LZ}	Delay time, CK high to DQ in low-impedance state (see Note 12)		1		1		ns
t _{HZ}	Delay time, CK high to DQ in high-impedance state (see Note 13)			8		8	ns
t _{IS}	Setup time, address, control, and data input		2		2		ns
t _{IH}	Hold time, address, control, and data input		1		1		ns
t _{CESP}	Power down/self-refresh exit time		8		8		ns
t _{RAS}	Delay time, ACTV command to DEAC or DCAB command		48	100 000	48		ns
t _{RC}	Delay time, ACTV,MRS,REFR,or SLFR to ACTV,MRS,REFR,or SLFR command		68		68		ns
t _{RCD}	Delay time ACTV command to READ,READ-P,WRT,or WRT-P command (see Note 14)		20		20		ns
t _{RP}	Delay time, DEAC or DCAB command to ACTV,MRS,REFR, or SLFR command		20		20		ns
t _{RRD}	Delay time,ACTV command in one bank to ACTV command in the other bank		16		16		ns
t _{RSA}	Delay time,MRS command to ACTV,MRS,REFR,or SLFR command		16		16		ns
t _{APR}	Final data out of READ-P operation to ACTV,MRS,SLFR,or REFR command		t _{RP} – (CL–1)*t _{CK}		t _{RP} – (CL–1)*t _{CK}		ns
t _{APW}	Final data in of WRT-P operation to ACTV,MRS,SLFR,or REFR command		t _{RP} + 1 t _{CK}		t _{RP} + 1 t _{CK}		ns
t _T	Transition time		1	5	1	5	ms
t _{REF}	Refresh interval			64		64	ms
n _{CCD}	Delay time, READ or WRT command to an interrupting command		1		1		cycles
n _{CDD}	Delay time, CS low or high to input enabled or inhibited		0	0	0	0	cycles
n _{CLE}	Delay time, CKE high or low to CLK enabled or disabled		1	1	1	1	cycles
n _{CWL}	Delay time, final data in of WRT operation to READ, READ-P, WRT, or WRT-P		1		1		cycles
n _{DID}	Delay time, ENBL or MASK command to enabled or masked data in		0	0	0	0	cycles
n _{DOD}	Delay time, ENBL or MASK command to enabled or masked data out		2	2	2	2	cycles
n _{HZP2}	Delay time, DEAC or DCAB, command to DQ in high-impedance state	CAS latency = 2		2		2	cycles

[†] All references are made to the rising transition of CK unless otherwise noted.

[‡] Specifications in this table represent a single SDRAM device.

NOTES: 11. t_{AC} is referenced from the rising transition of CK that precedes the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CK that is read latency (one cycle after the READ command). Access time is measured at output reference level 1.4 V.

12. t_{LZ} is measured from the rising transition of CK that is read latency (one cycle after the READ command).

13. t_{HZ} (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.

14. For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.

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ac timing requirements^{†‡} (continued)

		'xTTxxJPN-8		'xTTxxJPN-8A		UNIT
		MIN	MAX	MIN	MAX	
nH _{ZP3}	Delay time, DEAC or DCAB, command to DQ in high-impedance state	CAS latency = 3		3		cycles
n _{WCD}	Delay time, WRT command to first data in	0	0	0	0	cycles
n _{WR}	Delay time, final data in of WRT operation to DEAC or DCAB command	1		1		cycles

[†] All references are made to the rising transition of CK unless otherwise noted.
[‡] Specifications in this table represent a single SDRAM device.

serial presence detect

The serial presence detect (SPD) is contained in a 256-byte serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, SDRAM organization, and timing parameters (see tables below). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through an IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD Standard. See the Texas Instruments *Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.

Tables in this section list the SPD contents as follows:

Table 1—TM8TT64JPN Table 2—TM16TT64JPN
Table 3—TM8TT72JPN Table 4—TM16TT72JPN

Table 1. Serial-Presence-Detect Data for the TM8TT64JPN

BYTE NO.	DESCRIPTION OF FUNCTION	TM8TT64JPN-8		TM8TT64JPN-8A	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	9	09h	9	09h
5	Number of module rows on this assembly	1 bank	01h	1 bank	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	$t_{CK} = 8 \text{ ns}$	80h	$t_{CK} = 8 \text{ ns}$	80h
10	SDRAM access from clock at CL = X	$t_{AC} = 6 \text{ ns}$	60h	$t_{AC} = 6 \text{ ns}$	60h
11	DIMM configuration type (non-parity, parity, error correcting code [ECC])	Non-Parity	00h	Non-Parity	00h
12	Refresh rate / type	15.6 μs / self-refresh	80h	15.6 μs / self-refresh	80h
13	SDRAM width, primary DRAM	x8	08h	x8	08h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8	0Fh	1, 2, 4, 8	0Fh
17	Number of banks on each SDRAM device	4 banks	04h	4 banks	04h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h
21	SDRAM module attributes	Non-buffered / Non-registered	00h	Non-buffered / Non-registered	00h
22	SDRAM device attributes: general	V_{DD} tolerance = (+10%), Burst read / write, precharge all, auto precharge	0Eh	V_{DD} tolerance = (+10%), Burst read / write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X – 1	$t_{CK} = 10 \text{ ns}$	A0h	$t_{CK} = 15 \text{ ns}$	F0h

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serial presence detect (continued)

Table 1. Serial-Presence-Detect Data for the TM8TT64JPN (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM8TT64JPN-8		TM8TT64JPN-8A	
		ITEM	DATA	ITEM	DATA
24	Maximum data-access time from clock at CL = X – 1	t _{AC} = 6 ns	60h	t _{AC} = 7.5 ns	75h
25	Minimum clock cycle time at CL = X – 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X – 2	N/A	00h	N/A	00h
27	Minimum row precharge time	t _{RP} = 20 ns	14h	t _{RP} = 20 ns	14h
28	Minimum row-active to row-active delay	t _{RRD} = 16 ns	10h	t _{RRD} = 16 ns	10h
29	Minimum RAS-to-CAS delay	t _{RCD} = 16 ns	10h	t _{RCD} = 20 ns	14h
30	Minimum RAS pulse width	t _{RAS} = 48 ns	30h	t _{RAS} = 48 ns	30h
31	Density of each bank on module	64M Bytes	10h	64M Bytes	10h
32	Command and address signal input setup time	t _{IS} = 2 ns	20h	t _{IS} = 2 ns	20h
33	Command and address signal input hold time	t _{IH} = 1 ns	10h	t _{IH} = 1 ns	10h
34	Data signal input setup time	t _{IS} = 2 ns	20h	t _{IS} = 2 ns	20h
35	Data signal input hold time	t _{IH} = 1 ns	10h	t _{IH} = 1 ns	10h
36–61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1.2	12h	Rev. 1.2	12h
63	Checksum for byte 0–62	95	5Fh	196	C4h
64–71	Manufacturer's JEDEC ID code per JEP–106E	97h	9700... 00h	97h	9700... 00h
72	Manufacturing location [†]	TBD		TBD	
73–90	Manufacturer's part number [†]	TBD		TBD	
91	Die revision code [†]	TBD		TBD	
92	PCB revision code [†]	TBD		TBD	
93–94	Manufacturing date [†]	TBD		TBD	
95–98	Assembly serial number [†]	TBD		TBD	
99–125	Manufacturer-specific data [†]	TBD		TBD	
126–127	Vendor-specific data [†]	TBD		TBD	
128–166	System-integrator-specific data [‡]	TBD		TBD	
167–255	Open				

[†] TBD indicates values are determined at manufacturing time and are module-dependent.

[‡] These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 2. Serial-Presence-Detect Data for the TM16TT64JPN

BYTE NO.	DESCRIPTION OF FUNCTION	TM16TT64JPN-8		TM16TT64JPN-8A	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	9	09h	9	09h
5	Number of module rows on this assembly	2 banks	02h	2 banks	02h
6	Data width of this assembly	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	$t_{CK} = 8 \text{ ns}$	80h	$t_{CK} = 8 \text{ ns}$	80h
10	SDRAM access from clock at CL = X	$t_{AC} = 6 \text{ ns}$	60h	$t_{AC} = 6 \text{ ns}$	60h
11	DIMM configuration type (non-parity, parity, error correcting code [ECC])	Non-Parity	00h	Non-Parity	00h
12	Refresh rate/type	15.6 μs /self-refresh	80h	15.6 μs /self-refresh	80h
13	SDRAM width, primary DRAM	x8	08h	x8	08h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8	0Fh	1, 2, 4, 8	0Fh
17	Number of banks on each SDRAM device	4 banks	04h	4 banks	04h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h
21	SDRAM module attributes	Non-buffered/ Non-registered	00h	Non-buffered/ Non-registered	00h
22	SDRAM device attributes: general	V_{DD} tolerance = (+10%). Burst read/write, precharge all, auto precharge	0Eh	V_{DD} tolerance = (+10%). Burst read/write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X – 1	$t_{CK} = 10 \text{ ns}$	A0h	$t_{CK} = 15 \text{ ns}$	F0h
24	Maximum data-access time from clock at CL = X – 1	$t_{AC} = 6 \text{ ns}$	60h	$t_{AC} = 7.5 \text{ ns}$	75h
25	Minimum clock cycle time at CL = X – 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X – 2	N/A	00h	N/A	00h
27	Minimum row precharge time	$t_{RP} = 20 \text{ ns}$	14h	$t_{RP} = 20 \text{ ns}$	1Eh
28	Minimum row-active to row-active delay	$t_{RRD} = 16 \text{ ns}$	10h	$t_{RRD} = 16 \text{ ns}$	14h
29	Minimum $\overline{\text{RAS}}$ -to-CAS delay	$t_{RCD} = 20 \text{ ns}$	14h	$t_{RCD} = 20 \text{ ns}$	1Eh
30	Minimum $\overline{\text{RAS}}$ pulse width	$t_{RAS} = 48 \text{ ns}$	30h	$t_{RAS} = 48 \text{ ns}$	32h

TM8TT64JPN, TM16TT64JPN
TM8TT72JPN, TM16TT72JPN
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serial presence detect (continued)

Table 2. Serial-Presence-Detect Data for the TM16TT64JPN (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM16TT64JPN-8		TM16TT64JPN-8A	
		ITEM	DATA	ITEM	DATA
31	Density of each bank on module	64M Bytes	10h	64M Bytes	10h
32	Command and address signal input setup time	tIS = 2 ns	20h	tIS = 2 ns	20h
33	Command and address signal input hold time	tIH = 1 ns	10h	tIH = 1 ns	10h
34	Data signal input setup time	tIS = 2 ns	20h	tIS = 2 ns	20h
35	Data signal input hold time	tIH = 1 ns	10h	tIH = 1 ns	10h
36–61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1.2	12h	Rev. 1.2	12h
63	Checksum for byte 0–62	96	60h	197	C5h
64–71	Manufacturer's JEDEC ID code per JEP–106E	97h	9700...00h	97h	9700...00h
72	Manufacturing location [†]	TBD		TBD	
73–90	Manufacturer's part number [†]	TBD		TBD	
91	Die revision code [†]	TBD		TBD	
92	PCB revision code [†]	TBD		TBD	
93–94	Manufacturing date [†]	TBD		TBD	
95–98	Assembly serial number [†]	TBD		TBD	
99–125	Manufacturer-specific data [†]	TBD		TBD	
126–127	Vendor-specific data [†]	TBD		TBD	
128–166	System-integrator-specific data [‡]	TBD		TBD	
167–255	Open				

[†] TBD indicates values are determined at manufacturing time and are module-dependent.

[‡] These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 3. Serial-Presence-Detect Data for the TM8TT72JPN

BYTE NO.	DESCRIPTION OF FUNCTION	TM8TT72JPN-8		TM8TT72JPN-8A	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	9	09h	9	09h
5	Number of module rows on this assembly	1 bank	01h	1 bank	01h
6	Data width of this assembly	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	$t_{CK} = 8 \text{ ns}$	80h	$t_{CK} = 8 \text{ ns}$	80h
10	SDRAM access from clock at CL = X	$t_{AC} = 6 \text{ ns}$	60h	$t_{AC} = 6 \text{ ns}$	60h
11	DIMM configuration type (non-parity, parity, error correcting code [ECC])	ECC	02h	ECC	02h
12	Refresh rate/type	15.6 μs /self-refresh	80h	15.6 μs /self-refresh	80h
13	SDRAM width, primary DRAM	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8	0Fh	1, 2, 4, 8	0Fh
17	Number of banks on each SDRAM device	4 banks	04h	4 banks	04h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h
21	SDRAM module attributes	Non-buffered/ Non-registered	00h	Non-buffered/ Non-registered	00h
22	SDRAM device attributes: general	V_{DD} tolerance = (+10%), Burst read/write, precharge all, auto precharge	0Eh	V_{DD} tolerance = (+10%), Burst read/write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X – 1	$t_{CK} = 10 \text{ ns}$	A0h	$t_{CK} = 15 \text{ ns}$	F0h
24	Maximum data-access time from clock at CL = X – 1	$t_{AC} = 6 \text{ ns}$	60h	$t_{AC} = 7.5 \text{ ns}$	75h
25	Minimum clock cycle time at CL = X – 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X – 2	N/A	00h	N/A	00h
27	Minimum row precharge time	$t_{RP} = 20 \text{ ns}$	14h	$t_{RP} = 20 \text{ ns}$	14h
28	Minimum row-active to row-active delay	$t_{RRD} = 16 \text{ ns}$	10h	$t_{RRD} = 16 \text{ ns}$	10h
29	Minimum $\overline{\text{RAS}}$ -to-CAS delay	$t_{RCD} = 20 \text{ ns}$	14h	$t_{RCD} = 20 \text{ ns}$	14h
30	Minimum $\overline{\text{RAS}}$ pulse width	$t_{RAS} = 48 \text{ ns}$	30h	$t_{RAS} = 48 \text{ ns}$	30h
31	Density of each bank on module	64M Bytes	10h	64M Bytes	10h
32	Command and address signal input setup time	$t_{IS} = 2 \text{ ns}$	20h	$t_{IS} = 2 \text{ ns}$	20h

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TM8TT72JPN, TM16TT72JPN
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serial presence detect (continued)

Table 3. Serial-Presence-Detect Data for the TM8TT72JPN (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM8TT72JPN-8		TM8TT72JPN-8A	
		ITEM	DATA	ITEM	DATA
33	Command and address signal input hold time	tIH = 1 ns	10h	tIH = 1 ns	10h
34	Data signal input setup time	tIS = 2 ns	20h	tIS = 2 ns	20h
35	Data signal input hold time	tIH = 1 ns	10h	tIH = 1 ns	10h
36–61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1.2	12h	Rev. 1.2	12h
63	Checksum for byte 0–62	113	71h	214	D6h
64–71	Manufacturer's JEDEC ID code per JEP–106E	97h	9700...00h	97h	9700...00h
72	Manufacturing location [†]	TBD		TBD	
73–90	Manufacturer's part number [†]	TBD		TBD	
91	Die revision code [†]	TBD		TBD	
92	PCB revision code [†]	TBD		TBD	
93–94	Manufacturing date [†]	TBD		TBD	
95–98	Assembly serial number [†]	TBD		TBD	
99–125	Manufacturer-specific data [†]	TBD		TBD	
126–127	Vendor-specific data [†]	TBD		TBD	
128–166	System-integrator-specific data [‡]	TBD		TBD	
167–255	Open				

[†] TBD indicates values are determined at manufacturing time and are module-dependent.

[‡] These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 4. Serial Presence-Detect Data for the TM16TT72JPN

BYTE NO.	DESCRIPTION OF FUNCTION	TM16TT72JPN-8		TM16TT72JPN-8A	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	9	09h	9	09h
5	Number of module rows on this assembly	2 banks	02h	2 banks	02h
6	Data width of this assembly	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	$t_{CK} = 8 \text{ ns}$	80h	$t_{CK} = 8 \text{ ns}$	80h
10	SDRAM access from clock at CL = X	$t_{AC} = 6 \text{ ns}$	60h	$t_{AC} = 6 \text{ ns}$	60h
11	DIMM configuration type (non-parity, parity, error correcting code [ECC])	ECC	02h	ECC	02h
12	Refresh rate/type	15.6 μs /self-refresh	80h	15.6 μs /self-refresh	80h
13	SDRAM width, primary DRAM	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8	0Fh	1, 2, 4, 8	0Fh
17	Number of banks on each SDRAM device	4 banks	04h	4 banks	04h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h
21	SDRAM module attributes	Non-buffered/ Non-registered	00h	Non-buffered/ Non-registered	00h
22	SDRAM device attributes: general	V_{DD} tolerance = (+10%). Burst read/write, precharge all, auto precharge	0Eh	V_{DD} tolerance = (+10%). Burst read/write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X – 1	$t_{CK} = 10 \text{ ns}$	A0h	$t_{CK} = 15 \text{ ns}$	F0h
24	Maximum data-access time from clock at CL = X – 1	$t_{AC} = 6 \text{ ns}$	60h	$t_{AC} = 7.5 \text{ ns}$	75h
25	Minimum clock cycle time at CL = X – 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X – 2	N/A	00h	N/A	00h
27	Minimum row precharge time	$t_{RP} = 20 \text{ ns}$	14h	$t_{RP} = 20 \text{ ns}$	14h
28	Minimum row-active to row-active delay	$t_{RRD} = 16 \text{ ns}$	10h	$t_{RRD} = 16 \text{ ns}$	10h
29	Minimum $\overline{\text{RAS}}$ -to-CAS delay	$t_{RCD} = 20 \text{ ns}$	14h	$t_{RCD} = 20 \text{ ns}$	14h
30	Minimum $\overline{\text{RAS}}$ pulse width	$t_{RAS} = 48 \text{ ns}$	30h	$t_{RAS} = 48 \text{ ns}$	30h
31	Density of each bank on module	64M Bytes	10h	64M Bytes	10h

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serial presence detect (continued)

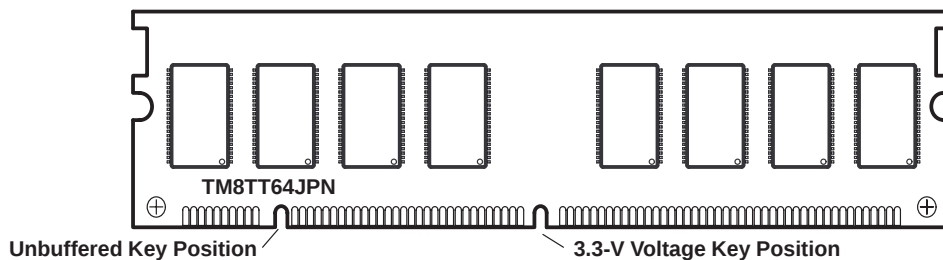
Table 4. Serial-Presence-Detect Data for the TM16TT72JPN (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM16TT72JPN-8		TM16TT72JPN-8A	
		ITEM	DATA	ITEM	DATA
32	Command and address signal input setup time	tIS = 2 ns	20h	tIS = 2 ns	20h
33	Command and address signal input hold time	tIH = 1 ns	10h	tIH = 1 ns	10h
34	Data signal input setup time	tIS = 2 ns	20h	tIS = 2 ns	20h
35	Data signal input hold time	tIH = 1 ns	10h	tIH = 1 ns	10h
36–61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1.2	12h	Rev. 1.2	12h
63	Checksum for byte 0–62	114	72h	215	D7h
64–71	Manufacturer's JEDEC ID code per JEP–106E	97h	9700...00h	97h	9700...00h
72	Manufacturing location [†]	TBD		TBD	
73–90	Manufacturer's part number [†]	TBD		TBD	
91	Die revision code [†]	TBD		TBD	
92	PCB revision code [†]	TBD		TBD	
93–94	Manufacturing date [†]	TBD		TBD	
95–98	Assembly serial number [†]	TBD		TBD	
99–125	Manufacturer-specific data [†]	TBD		TBD	
126–127	Vendor-specific data [†]	TBD		TBD	
128–166	System-integrator-specific data [‡]	TBD		TBD	
167–255	Open				

[†] TBD indicates values are determined at manufacturing time and are module-dependent.

[‡] These TBD values are determined and programmed by the customer (optional).

device symbolization (TM8TT64JPN)



YY = Year Code
 MM = Month Code
 T = Assembly Site Code
 -SS = Speed Code

NOTE A: Location of symbolization may vary.

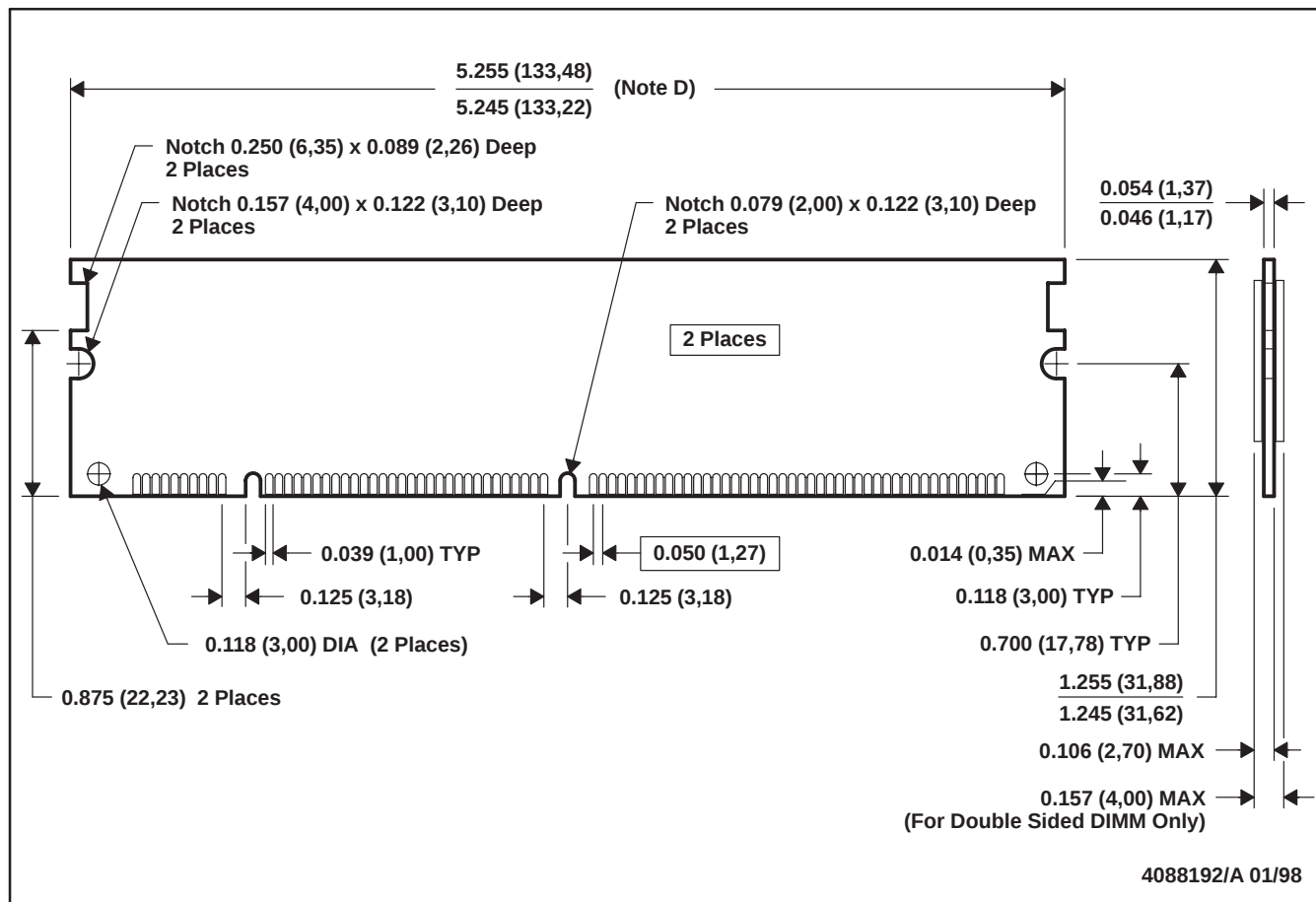
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BUV (R-PDIM-N168)

DUAL-IN-LINE MEMORY MODULE



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-161
D. Dimension includes depanelization variations; applies between notch and tab edge.
E. Outline may vary above notches to allow router/panelization irregularities.

PRODUCT PREVIEW

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