P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.10 @ V_{GS} = -10 V	±4.3
	0.16 @ V_{GS} = -4.5 V	±3.4

SO-8

Top View
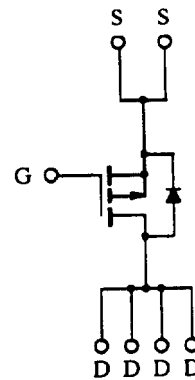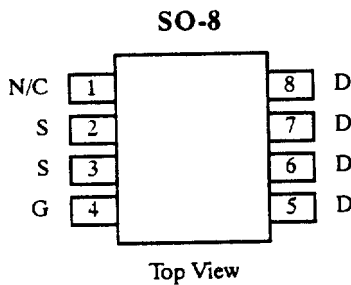
P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±4.3	A
	T_A = 70°C		±3.3	
Pulsed Drain Current		I_{DM}	±20	
Continuous Source Current (Diode Conduction)		I_S	-2.2	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	50	°C/W

Specifications ($T_J = 25\,^\circ$C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\,\mu$A	-0.5			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16$ V, $V_{GS} = 0$ V			-2	μA
		$V_{DS} = -16$ V, $V_{GS} = 0$ V, $T_J = 55\,^\circ$C			-25	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \leq -5$ V, $V_{GS} = -10$ V	-20			A
		$V_{DS} \leq -5$ V, $V_{GS} = -4.5$ V	-5			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = -10$ V, $I_D = 2.0$ A		0.07	0.10	Ω
		$V_{GS} = -4.5$ V, $I_D = 2.0$ A		0.11	0.16	
Forward Transconductance[b]	g_{fs}	$V_{DS} = -15$ V, $I_D = -4.3$ A		6		S
Diode Forward Voltage[b]	V_{SD}	$I_S = -1.25$ A, $V_{GS} = 0$ V		-1.0	-1.6	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = -10$ V, $V_{GS} = -10$ V, $I_D = -4.3$ A		29	40	nC
Gate-Source Charge	Q_{gs}			2.7	5	
Gate-Drain Charge	Q_{gd}			14	25	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10$ V, $R_L = 10\,\Omega$ $I_D \cong -1$ A, $V_{GEN} = -10$ V, $R_G = 6\,\Omega$		15	30	ns
Rise Time	t_r			30	80	
Turn-Off Delay Time	$t_{d(off)}$			142	200	
Fall Time	t_f			130	200	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25$ A, di/dt = 100 A/μs		70		

Notes:
a. Guaranteed by design, not subject to production testing.
b Pulse test, pulse width $\leq$ 300 μs, duty cycle $\leq$ 2%.

![Siliconix logo] **Siliconix**
A Member of the TEMIC Group

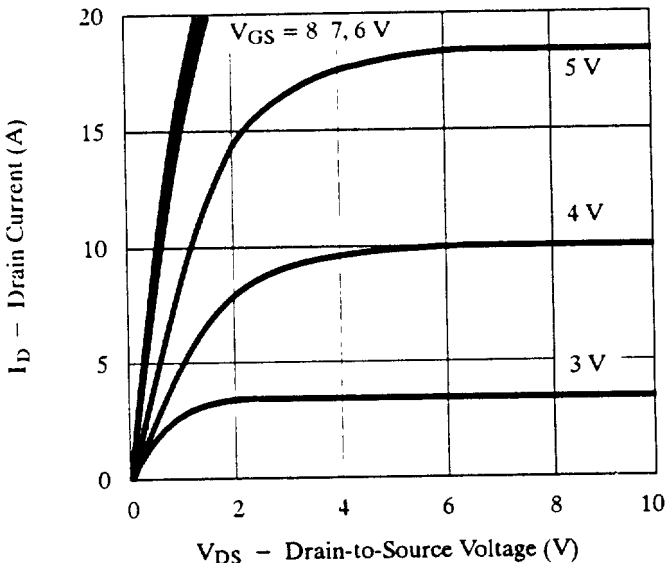# Typical Characteristics (25°C Unless Otherwise Noted)

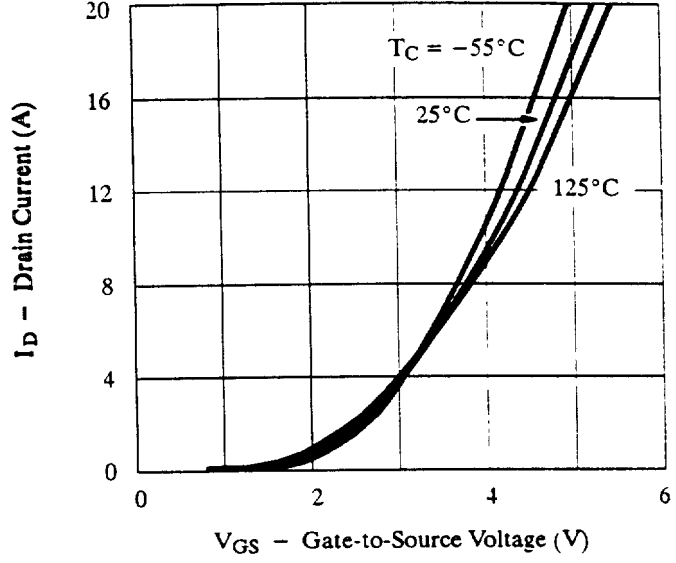
Figure 1: Output Characteristics

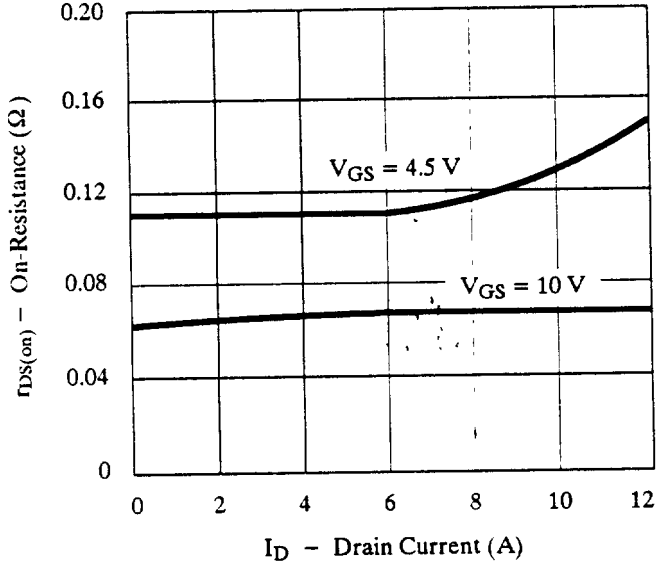**Figure 2:** Transfer Characteristics

Figure 3: On-Resistance vs. Drain Current
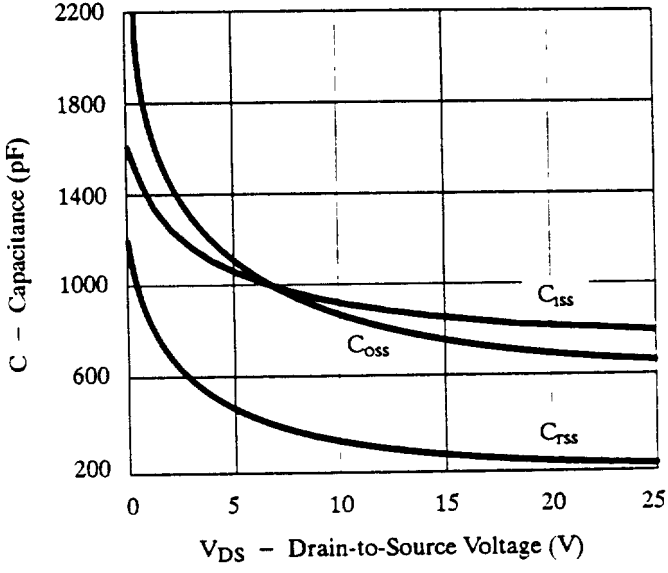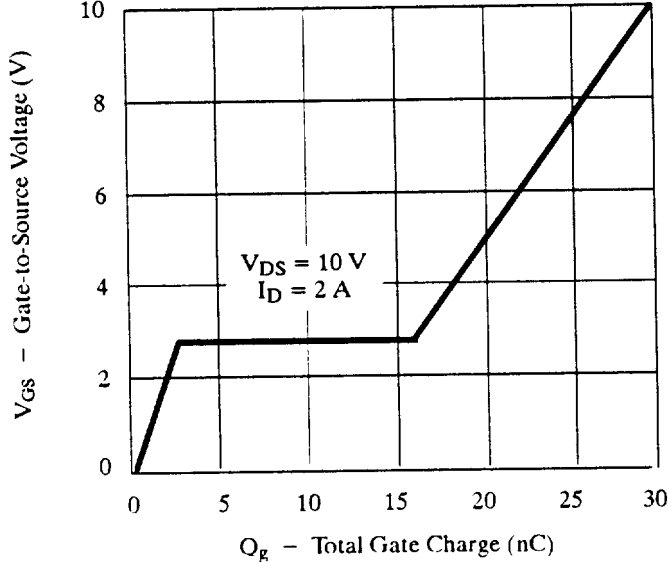

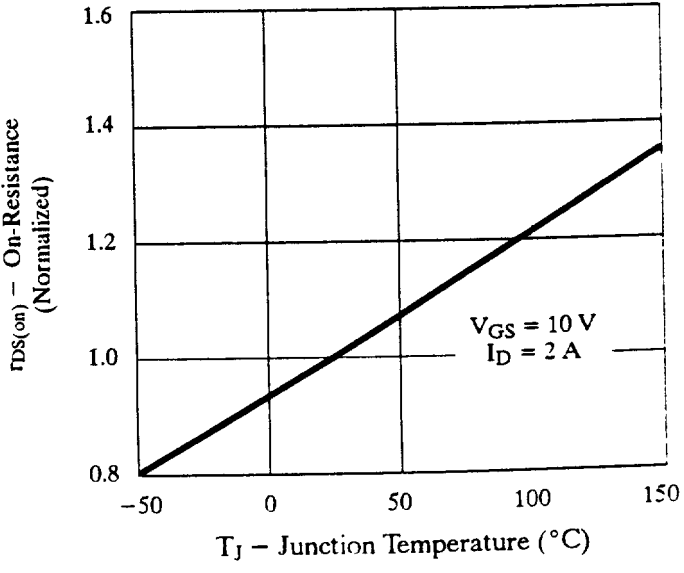**Figure 4:** Capacitance

Figure 5: Gate Charge

Figure 6: On-Resistance vs. Junction Temperature

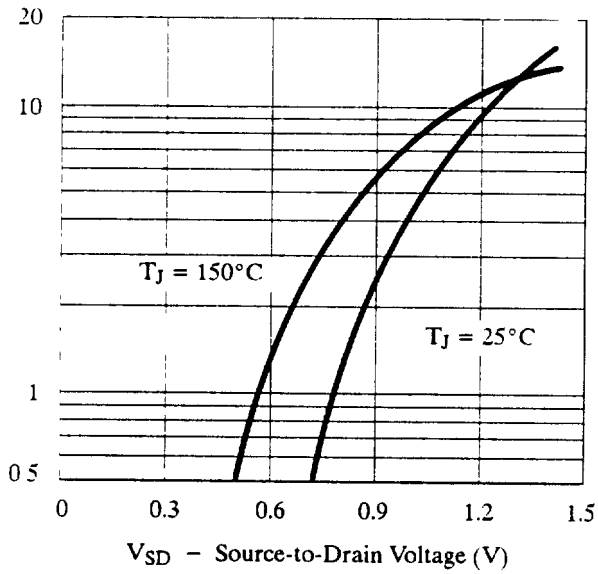## Typical Characteristics (25°C Unless Otherwise Noted)
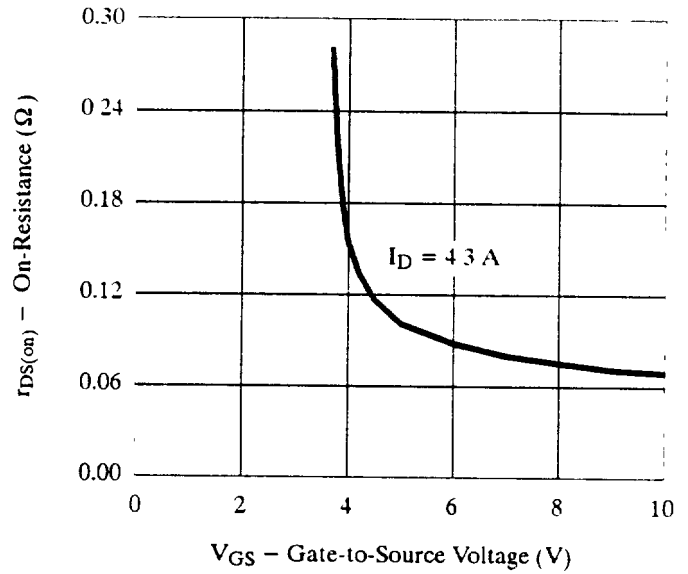
Figure 7: Source-Drain Diode Forward Voltage

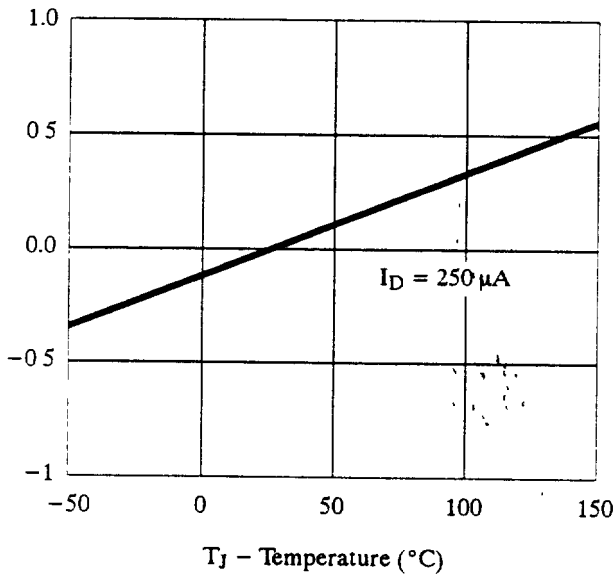Figure 8: On-Resistance vs. Gate-to-Source Voltage

Figure 9: Threshold Voltage

Figure 10: Single Pulse Power
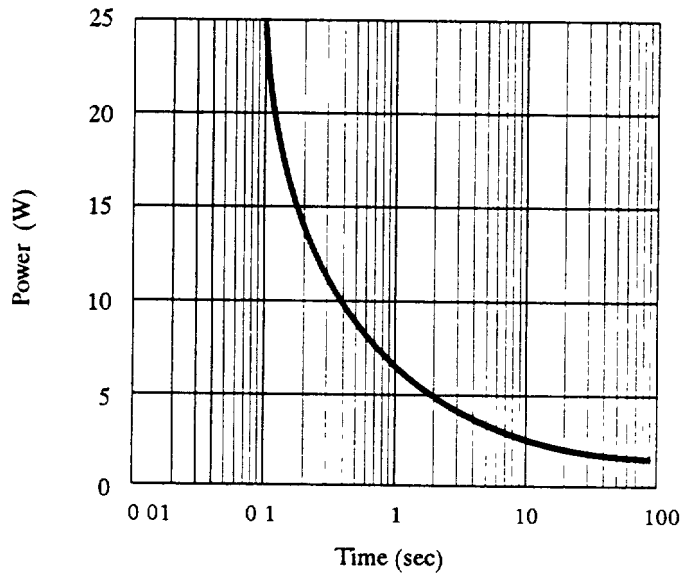
Notes

1 Duty Cycle, D = $\dfrac{t_1}{t_2}$

2. Per Unit Base = R_{thJA} = 50°C/W

3 $T_{JM} - T_A = P_{DM}Z_{thJA}^{(t)}$
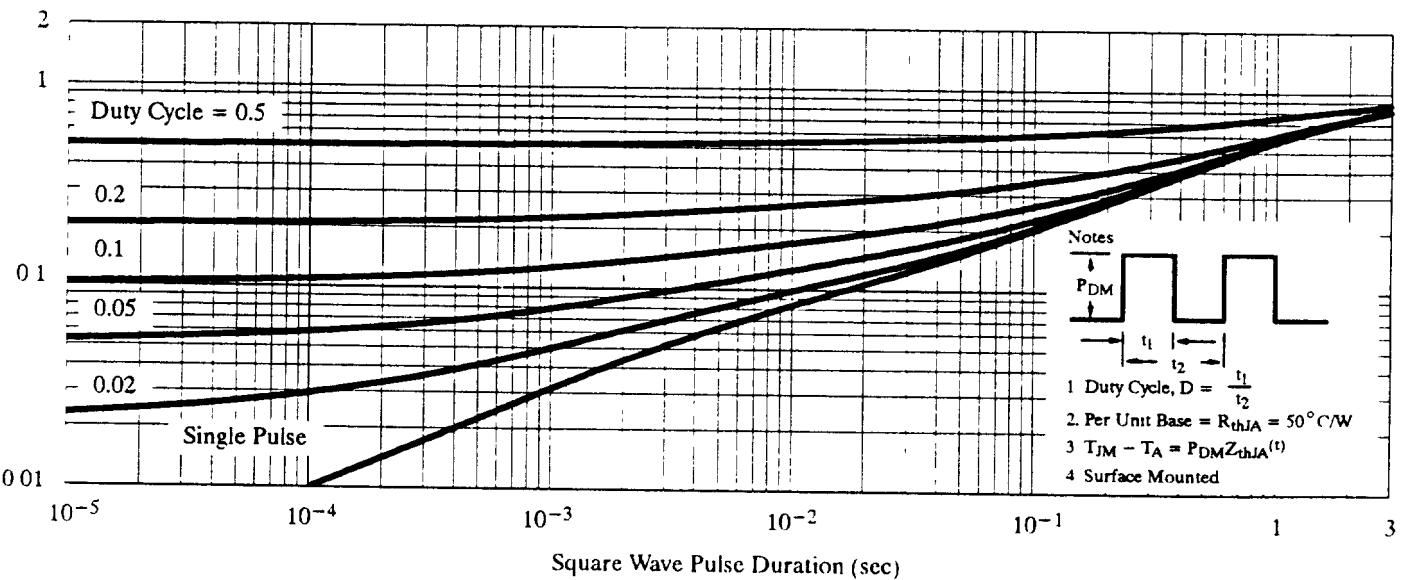
4 Surface Mounted

Figure 11: Normalized Effective Transient Thermal Impedance, Junction-to-Ambient