Quad Power Sequencing Controller

Features

- Power supply sequencer with four outputs
- Power-up and power-down sequencing
- Six programmable delays
- Maximum 90V supply voltage
- Input voltage window comparator
- Low power supply current (500µA typical)
- 16-Lead SOIC Package

Applications

- Reduction of transient current demand and protection of sensitive loads
- Telecom and networking systems
- High voltage MEMS and display driver supplies

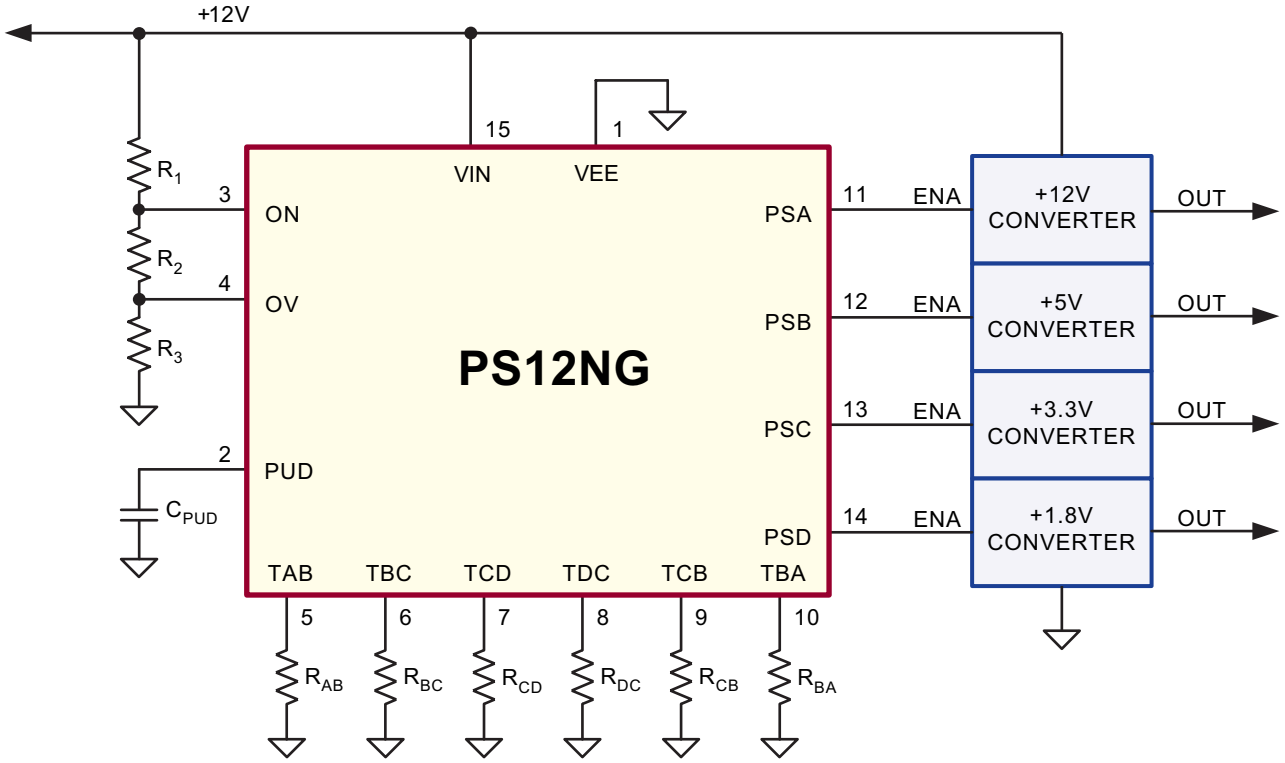
General Description

Many systems require that their power supplies are enabled and disabled sequentially in order to reduce transient current demand on the power bus, or to avoid damage to components having multiple supply voltages such as microprocessors, ASICs, MEMS drivers, etc.

The PS12 incorporates a power-up delay timer, a window voltage comparator, 4 open drain enable outputs, and 6 enable delay timers. The enable delays are individually programmable for both the power-up (ABCD) and the power-down (DCBA) sequence.

Power-up and power-down are controlled by a window comparator formed by the ON and OV voltage comparators. V_{IN} voltage within the window initiates power-up; V_{IN} voltage outside of the window maintains or initiates power-down. The power-up sequence may be interrupted while in progress. The power-down sequence, once initiated, cannot be interrupted until it is brought to completion.

Typical Application Circuit



Ordering Information

Device	Package Option
	16-Lead SOIC
PS12	PS12NG-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
VIN[1]	-0.3V...+100V
PSA...PSD[1]	-0.3V...+100V
ON, OV[1]	-0.3V...+8V
ESD (all pins except VIN, PSA...PSD)[2]	±2kV
Operating ambient temperature	-40°C...+85°C
Operating junction temperature	-40°C...+125°C
Storage temperature	-65°C...+150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

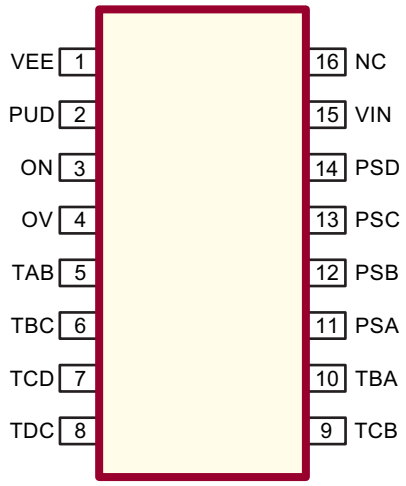
1. *Referenced to VEE*
2. *HBM, 1.5kΩ, 100pF*

Thermal Resistance

Package	θ_{ja}
16-Lead SOIC	65K/W to 120K/W

(PCB Layout dependent)

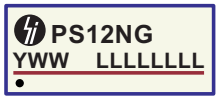
Pin Configuration



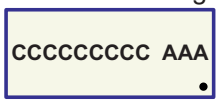
16-Lead SOIC
(top view)

Pin Configuration

Top Marking



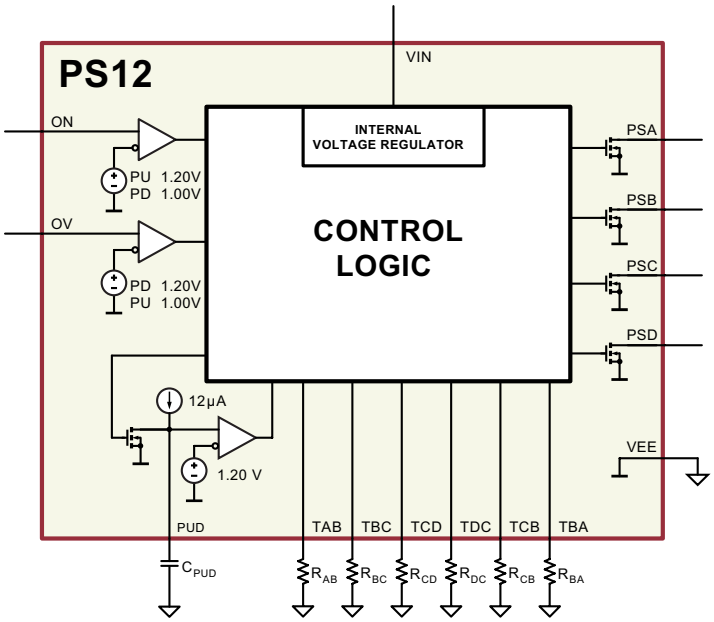
Bottom Marking



Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin
A = Assembler ID*
____ = "Green" Packaging

**May be part of top marking*

Block Diagram



Electrical Characteristics

*(T_J = 25°C unless otherwise specified. Voltages referenced to VEE, V_{VIN} = +4.5V...+90V. Values marked with * apply over the full temperature range.)*

Symbol	Parameter	Min	Typ	Max	Units		Conditions
Supply (V_{IN})							
V_{VIN}	Supply voltage	4.5	-	90	V	*	---
I_{VIN}	Supply current	-	500	625	µA	-	V_{IN} = 36V, R_T = 2MΩ
		-	400	-		-	V_{IN} = 12V, R_T = 2MΩ
Input Voltage Monitor (ON)							
V_{ONPU}	Power-up threshold	1.16	1.22	1.28	V	*	V_{ON} Rising
V_{ONPD}	Power-down threshold	1.06	1.12	1.18	V	*	V_{ON} Falling
V_{HY}	Power-up/Power-down hysteresis	-	100	-	mV	-	---
I_{ON}	Input Current	-	±1	-	nA	-	---
Input Voltage Monitor (OV)							
V_{OVPD}	Power-down threshold	1.16	1.22	1.28	V	*	V_{OV} Rising
V_{OVPU}	Power-up threshold	1.06	1.12	1.18	V	*	V_{OV} Falling
V_{HY}	Power-up/power-down hysteresis	-	100	-	mV	-	---
I_{OV}	Input current	-	±1	-	nA	-	---
Power Supply Enable Outputs (PSA, PSB, PSC, PSD)							
I_{LKG}	High state leakage current	-	-	10	µA	*	V_{PS} = 90V PS = HiZ
V_{SAT}	Low state output voltage	-	-	100	mV	-	I_{PS} = 1mA PS = Low
Power-up Delay (PUD)							
I_{PUD}	Output current	-8.4	-12	-16	µA	-	---
V_{PUD}	Threshold voltage	1.15	1.20	1.25	V	-	---
R_{DISCH}	Discharge FET ON resistance	-	500	-	Ω	-	I_{DISCH} = 1mA
Power Supply Enable Timing (TAB, TBC, TCD, TDC, TCB, TBA)							
R_T	Timing resistance range	50	-	2000	kΩ	-	---
$T_{PSPS(MAX)}$	Maximum PS-to-PS delay	160	200	240	ms	-	R_T = 2MΩ
$T_{PSPS(MIN)}$	Minimum PS-to-PS delay	4.0	5.0	6.0	ms	-	R_T = 50kΩ

Pin Description

Pin #	Function	Description
15	VIN	Power supply pins. VIN positive with respect to VEE. The outputs PSA thru PSD are pulled to a logic low state upon application of power.
1	VEE	
2	PUD	Hookup pin for the power-up-delay (PUD) timing capacitor. Pin pulls capacitor to ground upon application of power. (See timing diagram)
3	ON	Input pin of the ON comparator. Rising transition initiates power-up sequence.
4	OV	Input pin of the OV comparator. Rising transition initiates the power-down sequence.
5	TAB	Hookup pins for timing resistors. On power-up, the resistor at TAB determines the delay between the rising transitions of PSA and PSB; similarly, TBC relates to (PSB / PSC), and TCD to (PSC / PSD). On power-down, the resistor at TDC determines the delay between the falling transitions of PSD and PSC; similarly, TCB relates to (PSC / PSB), and TBA to (PSB / PSA).
6	TBC	
7	TCD	
8	TDC	
9	TCB	
10	TBA	
11	PSA	Power supply enable output pins. These four pins control loads, such as DC/DC converter modules, load switches, ICs, etc. Configured with open drain output stages. On power-up, right after expiration of the PUD delay, the sequencer asserts PSA, and subsequently asserts PSB, PSC and PSD observing the delays, programmed by the (TAB, TBC, and TCD) pins. On power-down, the sequencer deasserts PSD, and subsequently deasserts PSC, PSB, and PSA observing the delays, programmed by the (TAB, TBC, and TCD) pins.
12	PSB	
13	PSC	
14	PSD	
16	NC	No connect

Oscillograms

The figures of typical waveforms are organized in the following way:

Figure	Function	Description
1, 2, 3, 4	PS (A, B, C, D)	Power-up and power-down delays. Delay times around 5ms and 200ms.
5, 6	ON, PUD, PS (A, B, D)	ON pin detail. Fig.6. shows a power-down / power-up sequence.
7, 8	PUD, PS (A, B)	PUD pin detail; PSA is asserted when voltage at PUD pin about 1.2V. PUD pin resets when PSB is deasserted.
9	OV, PUD, PS (A, B)	OV pin detail. Overvoltage returns to voltage window.
10	ON, PS (A, B, C)	Partial power-up sequence. Power-down triggered by loss of valid ON.

Fig.1

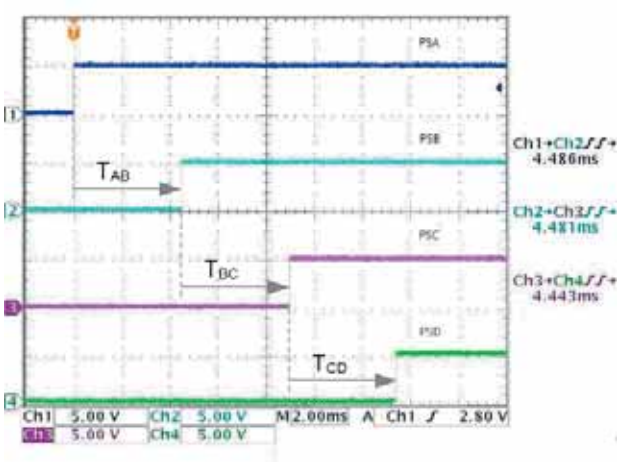


Fig.2

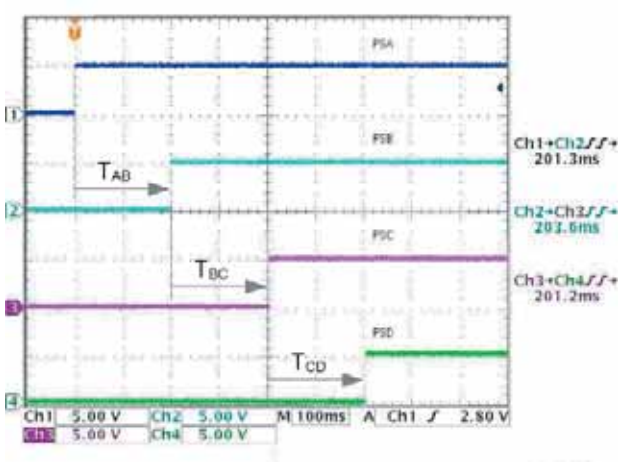


Fig.3

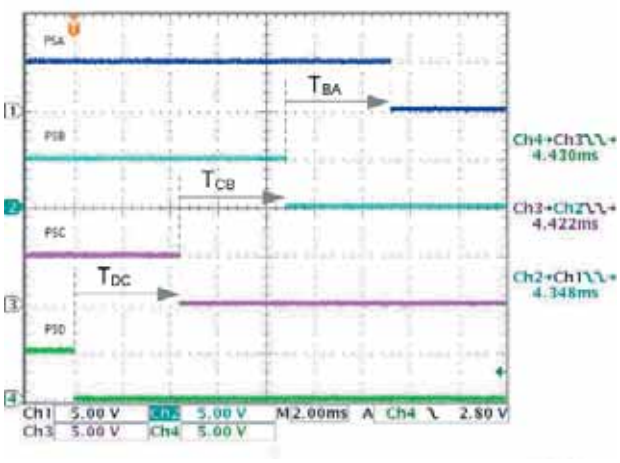


Fig.4

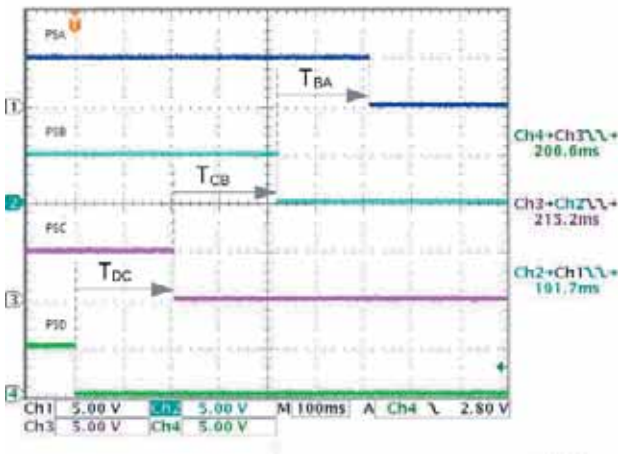


Fig.5

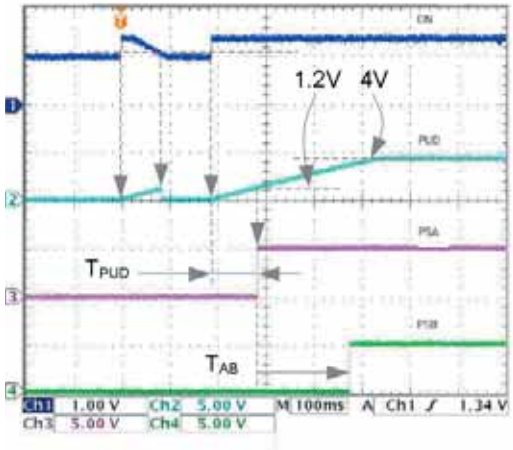


Fig.6

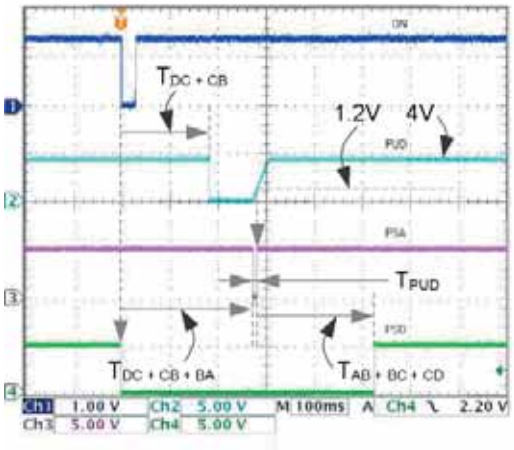


Fig.7

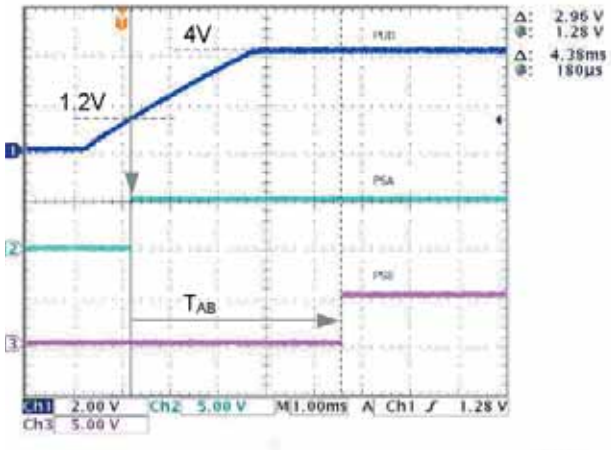


Fig.8

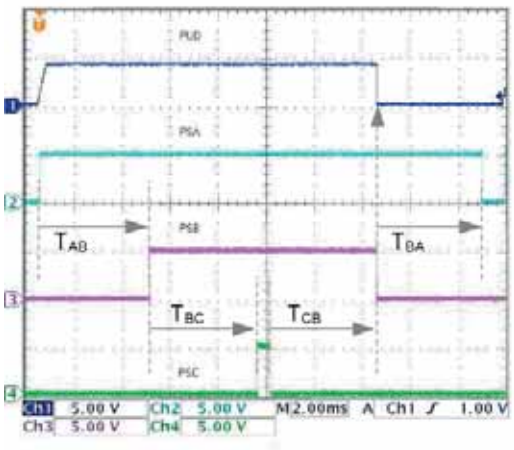


Fig.9

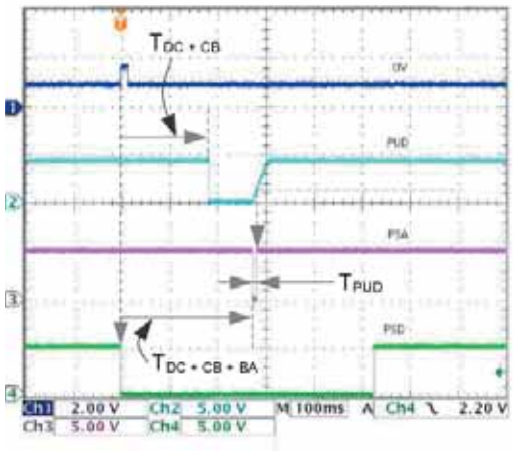
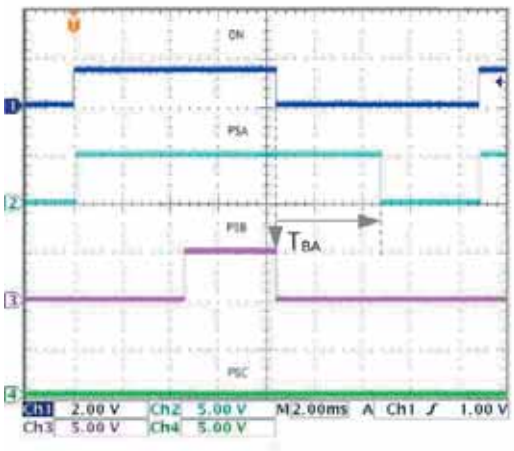


Fig.10



Functional Description

The PS12 provides power-up and power-down sequencing for devices such as power supply modules, load switches, ICs, etc. The four outputs PSA thru PSD are configured with open drain drivers, which are typically used to power supply modules. Some systems may require level-shifting or isolating drivers.

Upon application of power, the power-up delay timer is reset and the enable outputs PSA thru PSD are de-asserted.

Window Comparator

The state of the four PS outputs and the associated power-up and power-down sequencing is controlled by a window comparator formed by the ON and OV voltage comparators.

These comparators define a voltage window having thresholds programmed by an external resistive divider. The ON comparator defines the lower threshold of the window, while the OV comparator defines the upper threshold of the window. Both comparator thresholds feature 200mV hysteresis.

Power-up and Power-down Sequence

Power supply voltage moving into the window causes the start of a power-up sequence. The sequence consists of the power-up delay, programmed by C_{PUD}, and the subsequent assertion of the PS outputs in the sequence ABCD using the enable to enable delays (T_{AB}, T_{BC}, T_{CD}), as programmed by the resistors (R_{AB}, R_{BC}, R_{CD}).

Power supply voltage moving outside the window causes the start of a power-down sequence. The sequence consists of the de-assertion of the most recently asserted PS output, typically PSD, and subsequent de-assertion of other asserted PS outputs in the sequence DCBA using the enable delays (T_{DC}, T_{CB}, T_{BA}), as programmed by the resistors (R_{DC}, R_{CB}, R_{BA}).

The power-up sequence may be terminated prematurely by a power-down sequence. On the other hand, the power-down sequence is latching in nature; once power-down is initiated, the sequence is brought to completion regardless of changes in the state of the window comparator. After the power-down sequence is completed, a new power-up sequence may start, depending on the state of the window comparator at that time.

Enable Outputs at Low V_{IN}

The internal circuits of the PS12 can be expected to provide well-defined outputs at a power supply voltage of about 3.3V and above.

At lower power supply voltages, the existence of poorly defined output levels should typically not be an issue if the PS12 and the controlled loads share the same supply, since the loads may not be adequately biased as well.

Some caution is warranted when the controlled loads are independently powered and the power supply voltage to the PS12 is inadequate or ill-defined.

Delay Time Considerations

The PS12 is characterized for enable to enable delay times between 5ms and 200ms, which should cover most applications. Initial characterization of this device shows excellent linearity between delay time and programming resistance for a delay time in the range of 2.5ms to 5 seconds.

Shorting of a programming pin is not advised, and may reduce long term reliability, as internal circuits are not dimensioned for sourcing the resultant pin current.

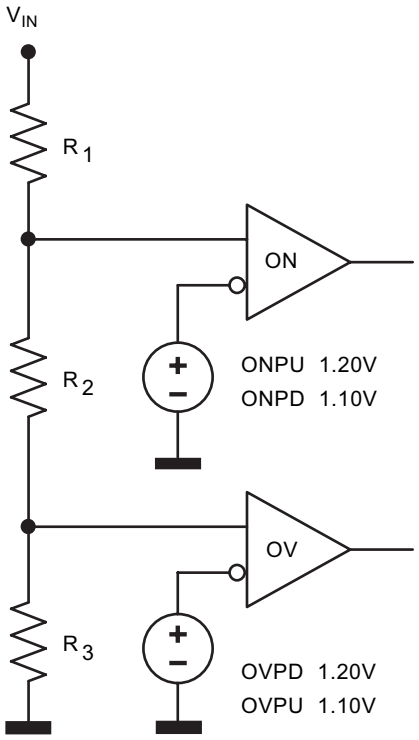
Power-up Delay (PUD)

The power-up delay is set by the time required to charge the C_{PUD} capacitor to 1.2V. The PUD pin sources a current of 12µA, resulting in a delay time of 100ms per µF. Charging continues past the power-up delay until a voltage of about 4V is reached.

An internal voltage comparator at the PUD pin inhibits the power-up sequence, should the C_{PUD} capacitor not be discharged before initiating the power-up delay.

Discharge of the C_{PUD} capacitor occurs during the power-down sequence. The discharge transistor is turned on at the end of the sequence when PSA is the last remaining asserted output.

Programming ON and UV



The ON and OV inputs draw negligible current, allowing the use of a high impedance divider. A divider current between 10µA and 100µA is more than adequate.

$$R_{DIV} = R_1 + R_2 + R_3$$

$$I_{DIV} = \frac{V_{IN}}{R_{DIV}}$$

V_{IN} thresholds can be determined from the following:

ON Power-up:	V_{ONPU} = 1.20V	$\frac{VIN_{ONPU}}{R_{DIV}} = \frac{V_{ONPU}}{R_2 + R_3}$
ON Power-down:	V_{ONPD} = 1.00V	$\frac{VIN_{ONPD}}{R_{DIV}} = \frac{V_{ONPD}}{R_2 + R_3}$
OV Power-down:	V_{OVPD} = 1.20V	$\frac{VIN_{OVPD}}{R_{DIV}} = \frac{V_{OVPD}}{R_3}$
OV Power-up:	V_{OVPU} = 1.00V	$\frac{VIN_{OVPU}}{R_{DIV}} = \frac{V_{OVPU}}{R_3}$

Start the design by programming the power-up voltage. The power-down voltage VIN_{ONPD} is fixed at 83.3% of the power-up voltage. Next, program the overvoltage power down voltage V_{OVPD} by selecting the multiplying factor R_2 / R_3, knowing VIN_{ONPU}.

A numerical example:
V_{IN} = 12V and [R_1, R_2, R_3] = [107kΩ, 4.99kΩ, 9.09kΩ], results in the following:

(1) R_{DIV} = 121.1kΩ,
(2) I_{DIV} = 99.1µA,
(3) [VIN_{ONPU}, VIN_{ONPD}, VIN_{OVPD}, VIN_{OVPU}] = [10.32V, 8.60V, 15.98V, 13.32V].

Note the following:

$$\frac{VIN_{OVPD}}{VIN_{ONPU}} = \frac{\frac{V_{OVPD}}{R_3}}{\frac{V_{ONPU}}{R_2+R_3}} = \frac{1.20}{1.20}\left(\frac{R_2+R_3}{R_3}\right) = 1+\frac{R_2}{R_3}$$

Programming the Power-up Delay

The power-up delay (T_{PUD}) is set by the time required to charge the C_{PUD} capacitor to the threshold voltage V_{PUD}:

$$V_{PUD} = 1.20V$$

$$I_{PUD} = 12\mu A$$

$$T_{PUD} = \frac{C_{PUD} \bullet V_{PUD}}{I_{PUD}}$$

A numerical example:
A 100nF capacitor results in a T_{PUD} of 12ms.

Programming the PS to PS Delay

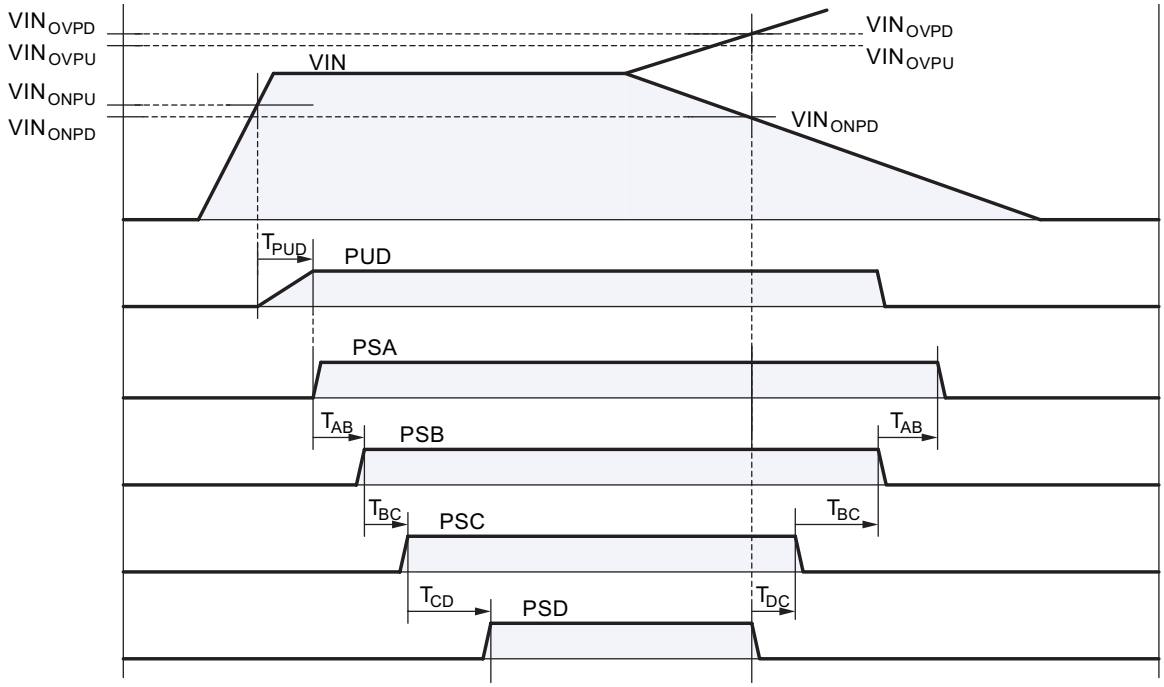
The PS to PS delays are set by the six timing resistors. Delay time and resistance are related as follows:

$$T_{PSPS} = K_T \bullet R_T$$

$$K_T = 100\,\frac{ns}{\Omega}$$

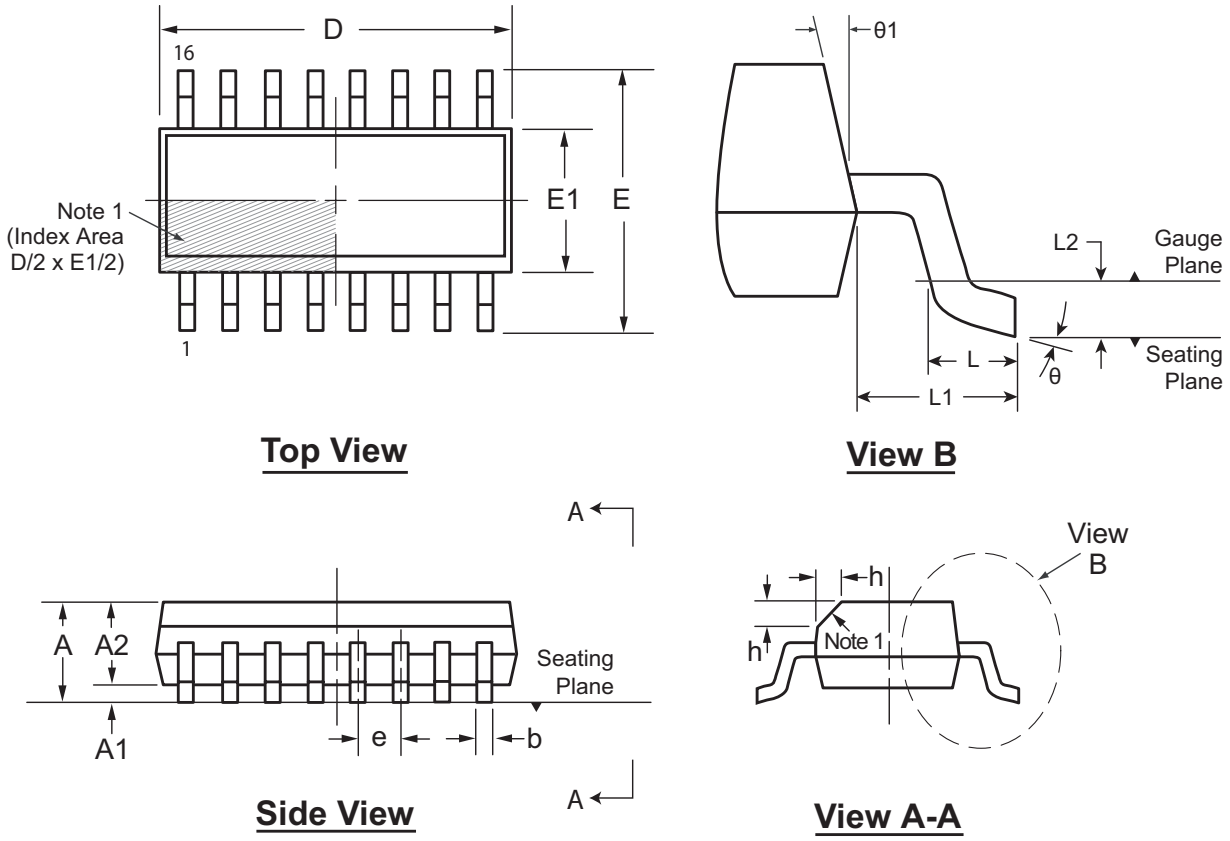
A numerical example:
A resistance of 100kΩ results in a delay time of 10ms.

Timing Diagram



16-Lead SOIC (Narrow Body) Package Outline (NG)

9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note 1:

This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35	0.10	1.25	0.31	9.80	5.80	3.80	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65	0.51	10.00	6.20	4.00		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.

Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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