

AP6679GI

Pb Free Plating Product

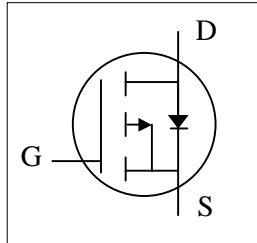


**Advanced Power
Electronics Corp.**

P-CHANNEL ENHANCEMENT MODE

POWER MOSFET

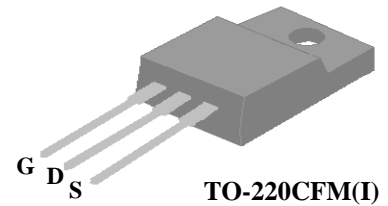
- ▼ Low Gate Charge
- ▼ Single Drive Requirement
- ▼ Lower On-resistance
- ▼ RoHS Compliant



BV_{DSS}	-30V
$R_{DS(ON)}$	9m Ω
I_D	-48A

Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.



The TO-220CFM isolation package is universally preferred for all commercial-industrial through hole applications.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 25	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	-48	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	-30	A
I_{DM}	Pulsed Drain Current ¹	300	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation	31.3	W
	Linear Derating Factor	0.25	W/ $^\circ C$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Thermal Resistance Junction-case	Max. 4	$^\circ C/W$
Rthj-a	Thermal Resistance Junction-ambient	Max. 62	$^\circ C/W$



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Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =-1mA	-	-0.02	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-30A	-	-	9	mΩ
		V _{GS} =-4.5V, I _D =-24A	-	-	15	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1	-	-3	V
g _{fs}	Forward Transconductance	V _{DS} =-10V, I _D =-30A	-	43	-	S
I _{DSS}	Drain-Source Leakage Current (T _j =25°C)	V _{DS} =-30V, V _{GS} =0V	-	-	-1	uA
	Drain-Source Leakage Current (T _j =150°C)	V _{DS} =-24V, V _{GS} =0V	-	-	-25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} = ±25	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =-30A	-	40	67	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-25V	-	8	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-4.5V	-	28	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =-15V	-	15	-	ns
t _r	Rise Time	I _D =-30A	-	75	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =-10V	-	50	-	ns
t _f	Fall Time	R _D =0.5Ω	-	90	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	3100	4590	pF
C _{oss}	Output Capacitance	V _{DS} =-25V	-	930	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	690	-	pF
R _g	Gate Resistance	f=1.0MHz	-	2.7	4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =-30A, V _{GS} =0V	-	-	-1.3	V
t _{rr}	Reverse Recovery Time	I _S =-24A, V _{GS} =0V, dI/dt=-100A/μs	-	47	-	ns
Q _{rr}	Reverse Recovery Charge		-	45	-	nC

Notes:

- 1.Pulse width limited by safe operating area.
- 2.Pulse width ≤300us , duty cycle ≤2%.

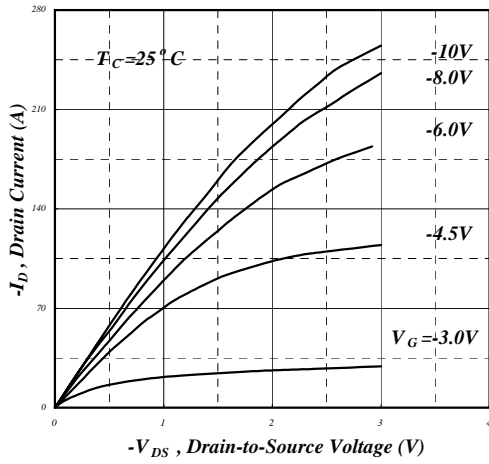


Fig 1. Typical Output Characteristics

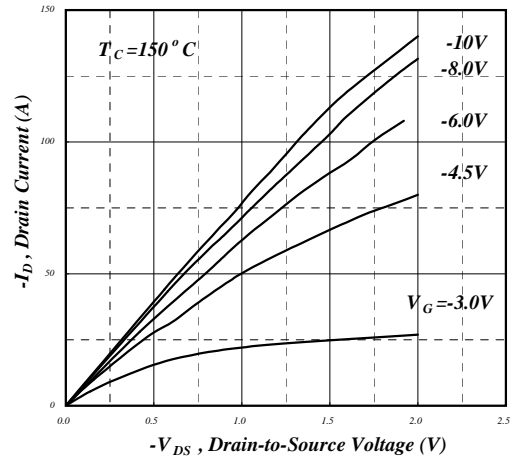


Fig 2. Typical Output Characteristics

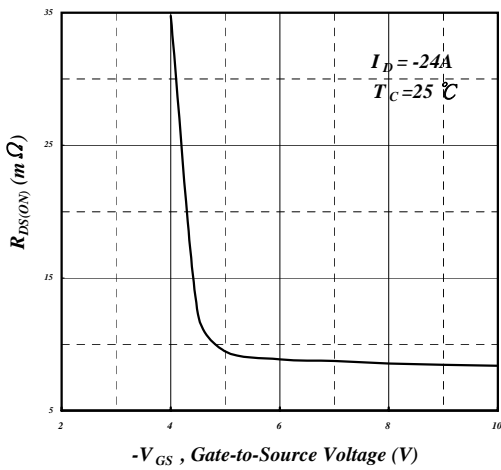


Fig 3. On-Resistance v.s. Gate Voltage

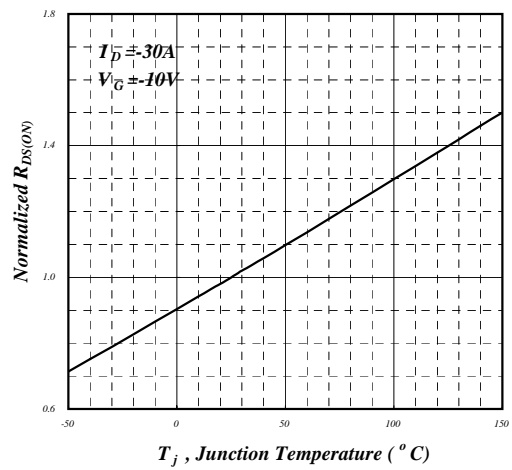


Fig 4. Normalized On-Resistance v.s. Junction Temperature

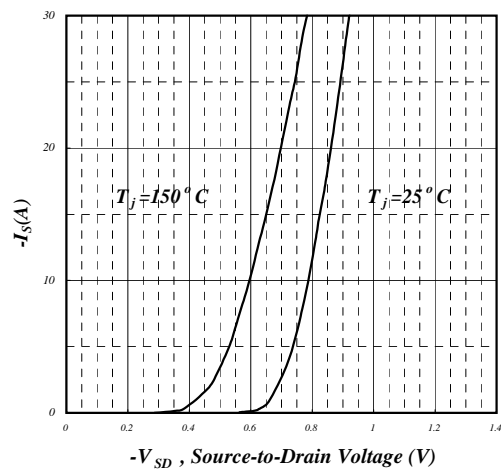


Fig 5. Forward Characteristic of Reverse Diode

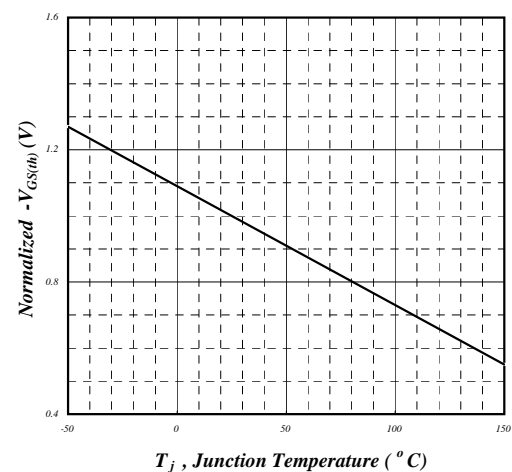


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

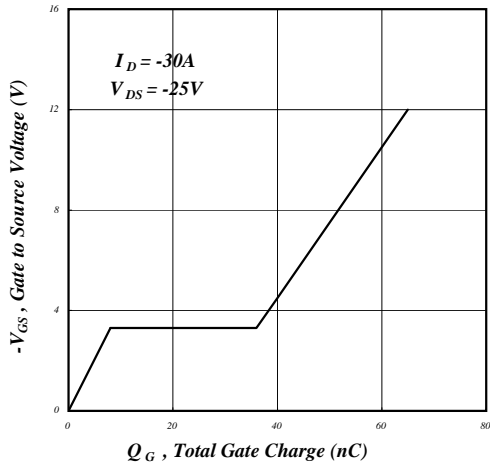


Fig 7. Gate Charge Characteristics

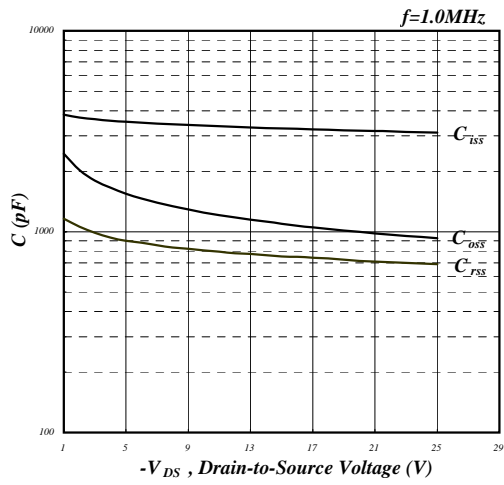


Fig 8. Typical Capacitance Characteristics

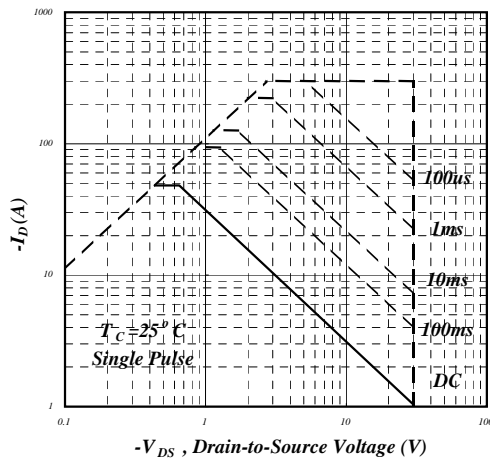


Fig 9. Maximum Safe Operating Area

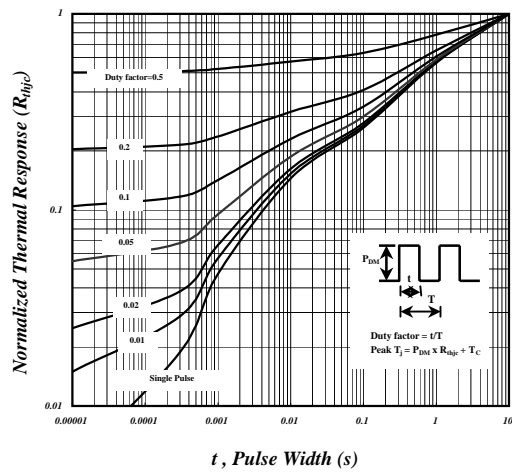


Fig 10. Effective Transient Thermal Impedance

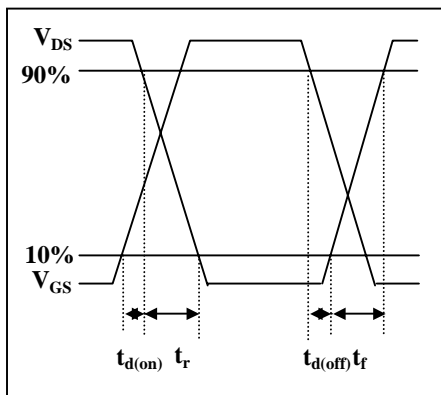


Fig 11. Switching Time Waveform

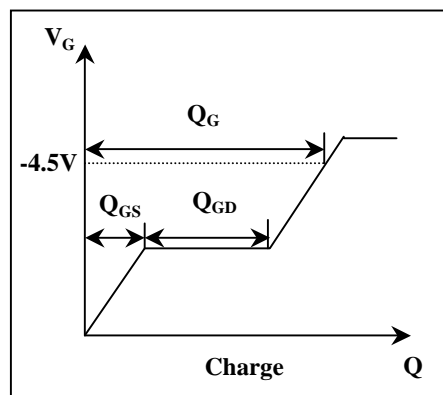


Fig 12. Gate Charge Waveform