AOU417
P-Channel Enhancement Mode Field Effect Transistor

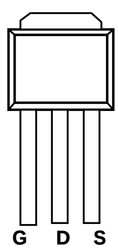
General Description

The AOU417 uses advanced trench technology to provide excellent RDS(ON), and low gate charge. This device is suitable for use as a load switch or in PWM applications. *Standard product AOU417 is Pb-free (meets ROHS & Sony 259 specifications). AOU417L is a Green Product ordering option. AOU417 and AOU417L are electrically identical .*

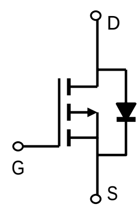
Features

V_{DS} (V) = -30V
I_D = -18A (V_{GS} = -10V)
$R_{DS(ON)}$ < 22mΩ (V_{GS} = -10V)
$R_{DS(ON)}$ < 40mΩ (V_{GS} = -4.5V)

TO-251



Top View
Drain Connected
to Tab



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [B,G]	T_A=25°C [G]	I_D	-18	A
	T_A=100°C [G]		-18	
Pulsed Drain Current		I_{DM}	-40	
Avalanche Current [C]		I_{AR}	-18	A
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	16.2	mJ
Power Dissipation [B]	T_C=25°C	P_D	50	W
	T_C=100°C		25	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	Steady-State	$R_{\theta JA}$	105	125	°C/W
Maximum Junction-to-Case [C]	Steady-State	$R_{\theta JL}$	2.5	3	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V			-1	µA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-1.4	-2	-2.7	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	-40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-18A		18	22	mΩ
		T_J=125°C		25	30	
		V_{GS}=-4.5V, I_D=-10A		29	40	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-18A		21		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.7	-1	V
I_S	Maximum Body-Diode Continuous Current				-1.2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		1573	1900	pF
C_{oss}	Output Capacitance			319		pF
C_{rss}	Reverse Transfer Capacitance			211		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		6.7	10	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge (10V)	V_{GS}=-10V, V_{DS}=-15V, I_D=-18A		29.3	35	nC
Q_g(4.5V)	Total Gate Charge (4.5V)			15	18	nC
Q_{gs}	Gate Source Charge			6.1		nC
Q_{gd}	Gate Drain Charge			7		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=0.83Ω, R_{GEN}=3Ω		11.7		ns
t_r	Turn-On Rise Time			29		ns
$t_{D(off)}$	Turn-Off DelayTime			42		ns
t_f	Turn-Off Fall Time			32.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-18A, dI/dt=100A/µs		28.3	37	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-18A, dI/dt=100A/µs		20.5		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.
B. The power dissipation PD is based on TJ(MAX)=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C: Repetitive rating, pulse width limited by junction temperature TJ(MAX)=175°C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6,12,14 are obtained using 80 µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of TJ(MAX)=175°C.
G. The maximum current rating is limited by bond-wires.
Rev1: August 2005

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

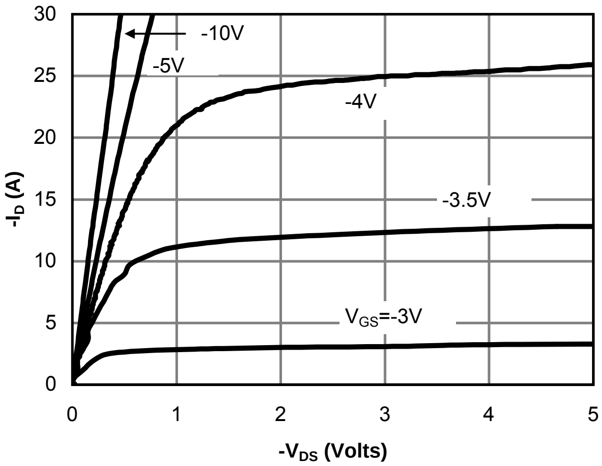


Fig 1: On-Region Characteristics

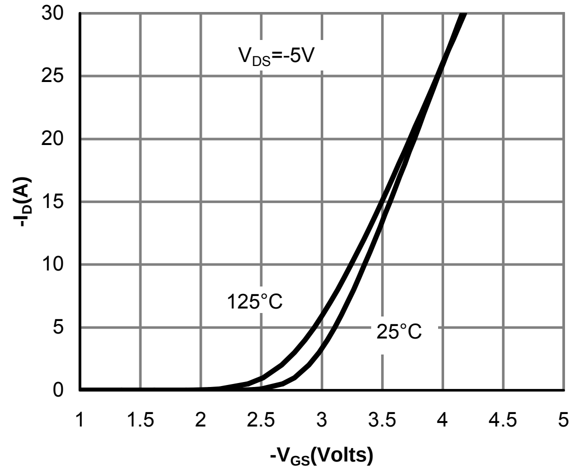


Figure 2: Transfer Characteristics

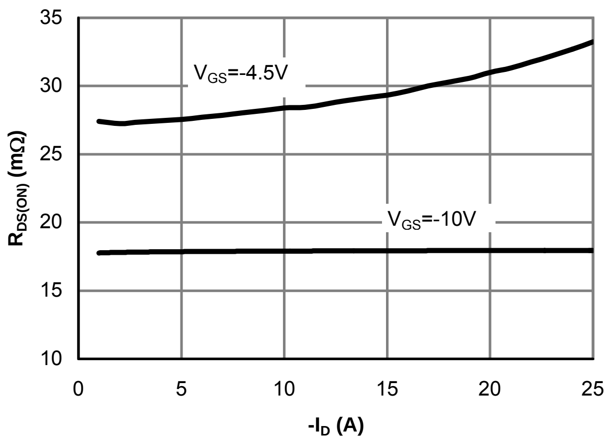


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

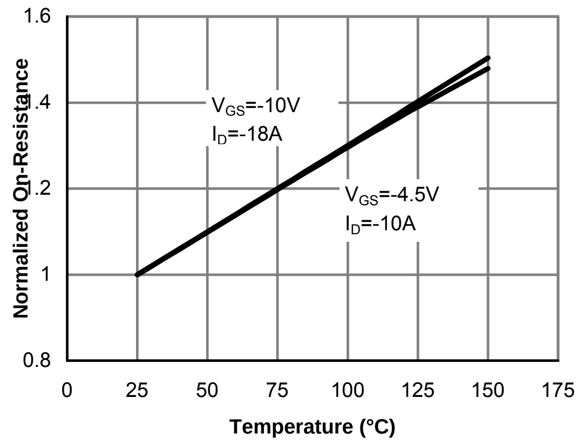


Figure 4: On-Resistance vs. Junction Temperature

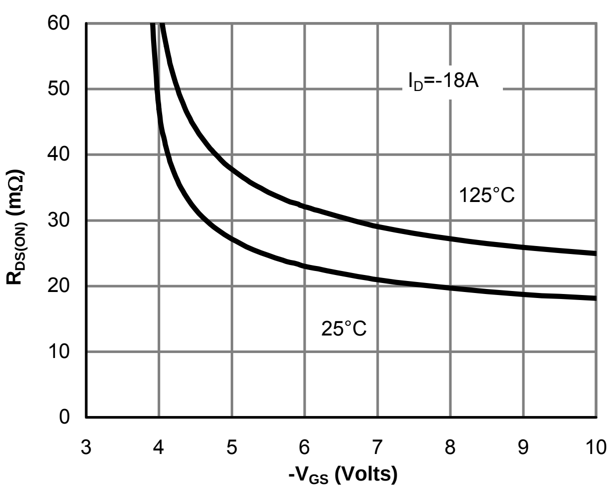


Figure 5: On-Resistance vs. Gate-Source Voltage

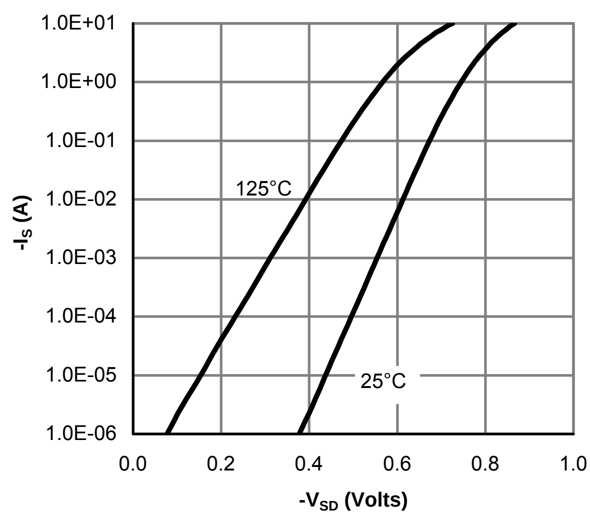


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

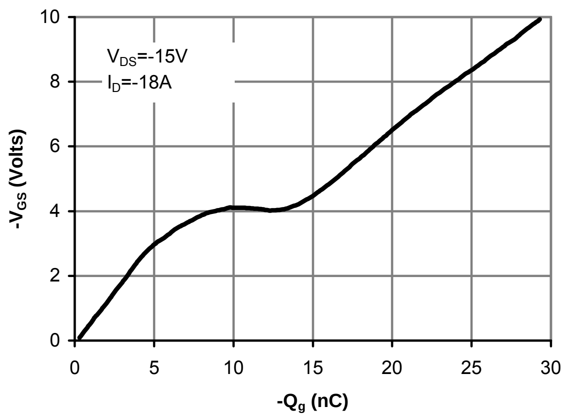


Figure 7: Gate-Charge Characteristics

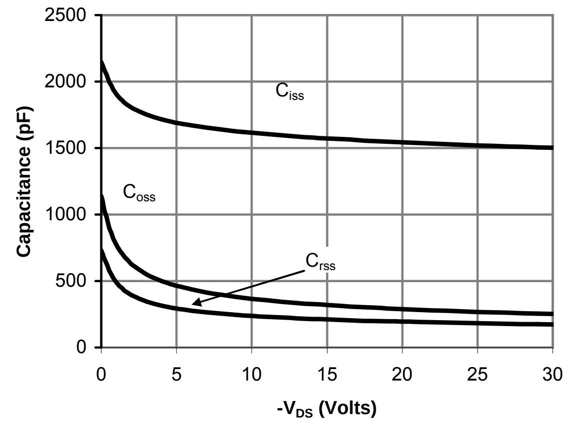


Figure 8: Capacitance Characteristics

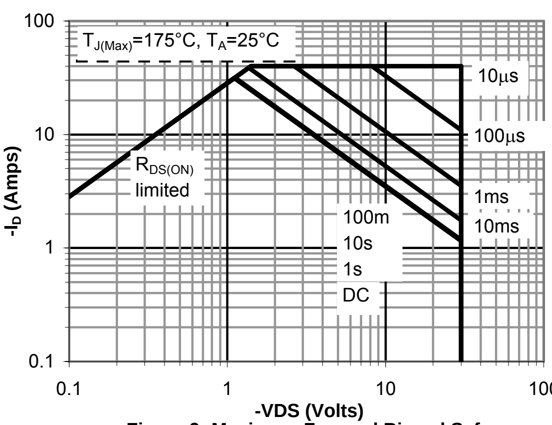


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

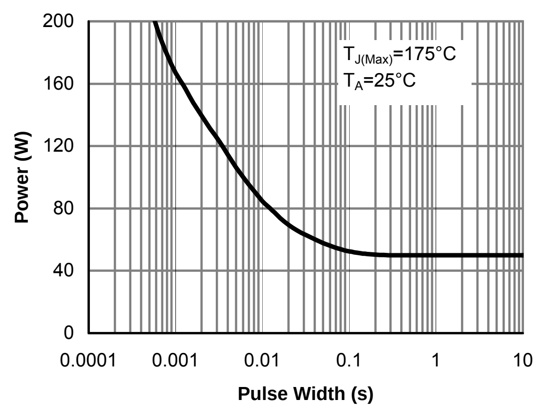


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

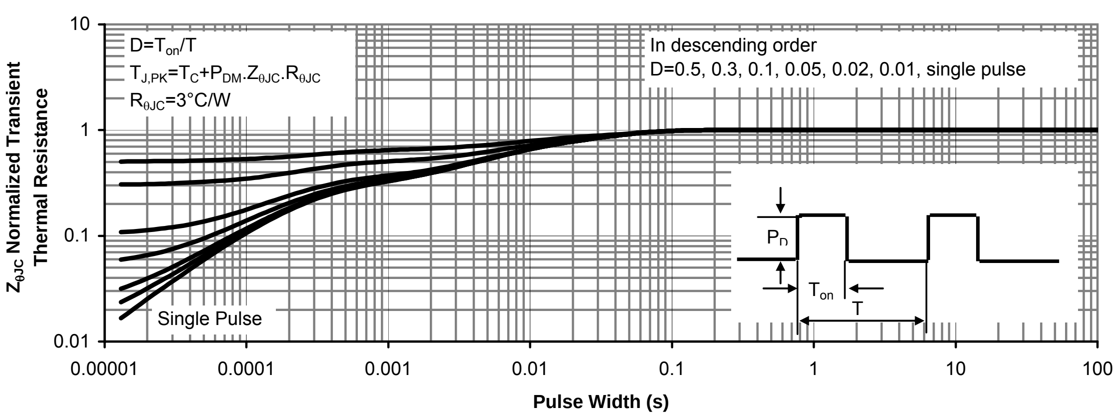


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

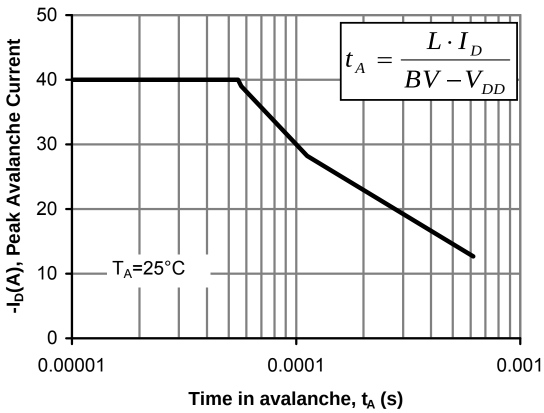


Figure 12: Single Pulse Avalanche capability

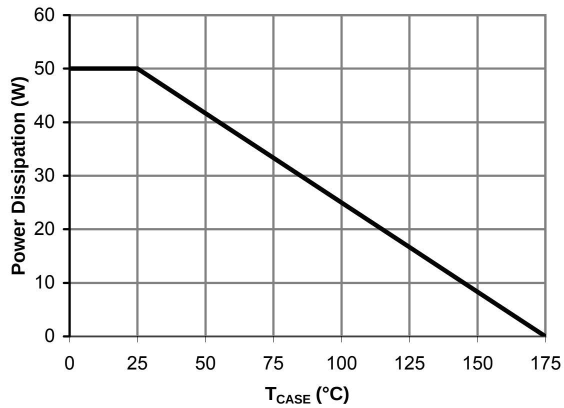


Figure 13: Power De-rating (Note B)

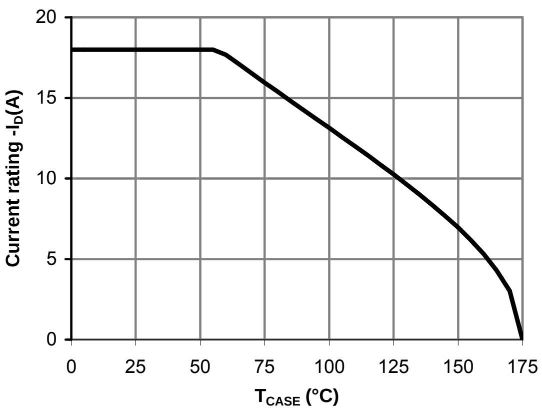


Figure 14: Current De-rating (Note B)