AKD4565
Evaluation board Rev.A for AK4565

GENERAL DESCRIPTION

AKD4565 is an evaluation board for the 20bit 2ch A/D and D/A converter, AK4565. The AKD4565 can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D → D/A). The A/D section can be evaluated by interfacing with AKM's DAC evaluation boards directly. The AKD4565 has the interface with AKM's ADC evaluation boards. Therefore, it's easy to evaluate the D/A section. The AKD4565 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4565 --- Evaluation board for AK4565
(Cable for connecting with printer port of IBM-AT, compatible PC and control software are packed with this.)

FUNCTION

- **Compatible with 2 types of interface**
  - **Direct interface with AKM's A/D & D/A converter evaluation boards**
  - **DIT/DIR with optical input/output**
- **BNC connector for an external clock input**
- **10pin Header for serial control mode**

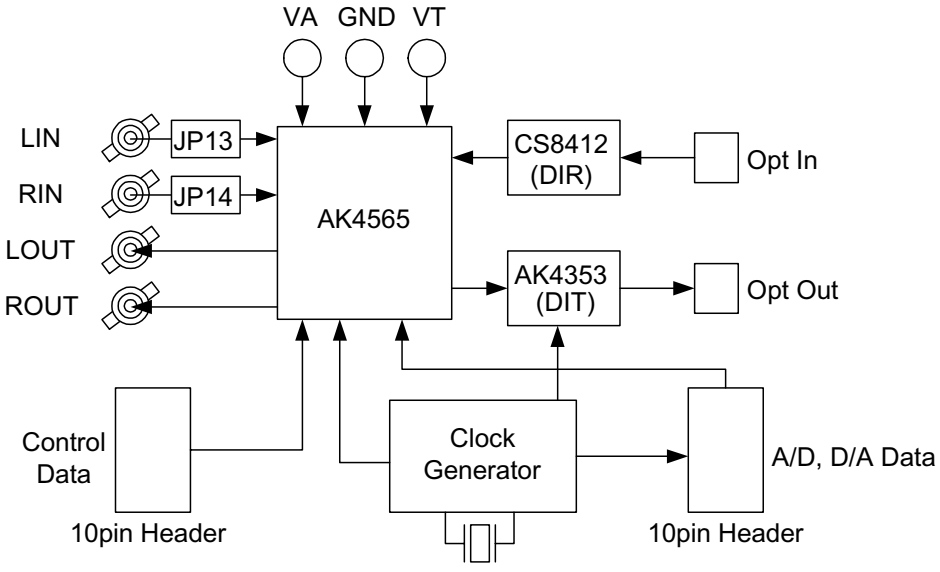


Figure 1. AKD4565 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

EVALATION BOARD MANUAL

■ Operation sequence

1) Set up the power supply lines.

[VA]	(orange)	= 2.3 ~ 3.6V	: for VA of AK4565 (typ. 2.5V)
[VT]	(orange)	= 1.5 ~ 3.6V	: for VT of AK4565 (typ. 2.5V)
[D2V]	(orange)	= 1.5 ~ 3.6V	: for 74LVC541 (typ. 2.5V)
[D5V]	(red)	= 3.6 ~ 5.0V	: for logic (typ. 5.0V)
[AGND]	(black)	= 0V	: for analog ground
[DGND]	(black)	= 0V	: for logic ground

Each supply line should be distributed from the power supply unit.
VT and D2V must be same voltage level.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.
The AK4565 and AK4353(DIT) should be reset once bringing SW1, 2 "L" upon power-up.

■ Evaluation mode

Applicable Evaluation Mode

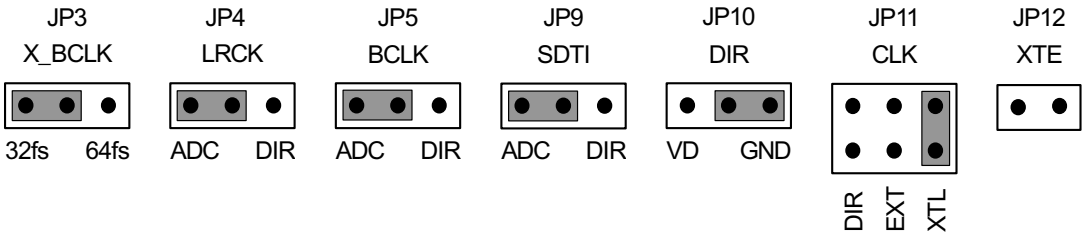
1) Evaluation of loopback mode <Default>
2) Evaluation of D/A using A/D converted data
3) Evaluation of D/A using DIR (Optical Link)
4) Evaluation of A/D using D/A converted data
5) Evaluation of A/D using DIT (Optical Link)
6) All interface signals including master clock are fed externally.

1) Evaluation of loopback mode. <Default>

Nothing should be connected to PORT3 and PORT4. In case of using external clock through a BNC connector (J1), select EXT on JP11 (CLK) and short JP12 (XTE). When SDTO0 is connected with SDTI, JP8 (SD0/1) selects SD0 side. When SDTO1 is connected with SDTI, JP8 (SD0/1) selects SD1 side.
Does not support DIF1-0 = "01".

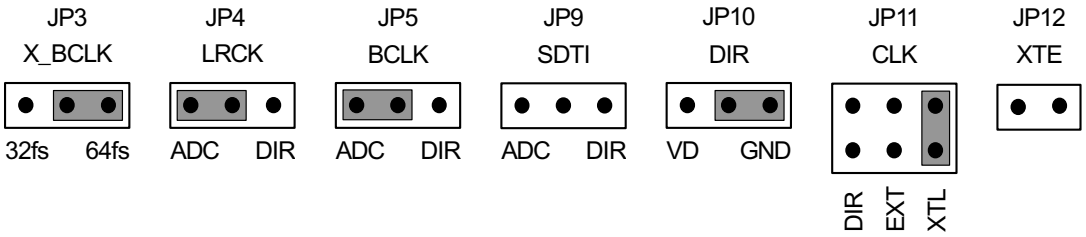
AK4565				JP3 (X_BCLK)
DIF1	DIF0	SDTO0/SDTO1 (ADC)	SDTI (DAC)	
0	0	20bit MSB justified	16bit LSB justified	32fs
1	0	20bit MSB justified	20bit MSB justified	64fs
1	1	I^2S Compatible	I^2S Compatible	32fs or 64fs

Table 1. AK4565 audio data I/F format and JP3 Setting



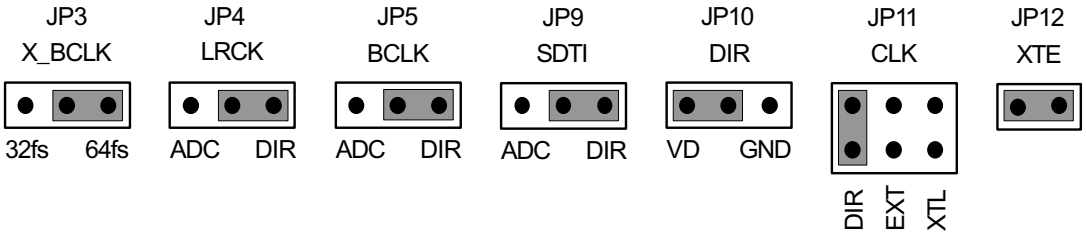
2) Evaluation of D/A using A/D converted data.

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's A/D evaluation boards with PORT3. MCLK, BCLK, LRCK and SDTO0/1 are sent from AKD4565 to AKM's D/A evaluation boards. Nothing should be connected to PORT1, PORT4. In case of using external clock through a BNC connector (J1), select EXT on JP11 (CLK) and short JP12 (XTE).



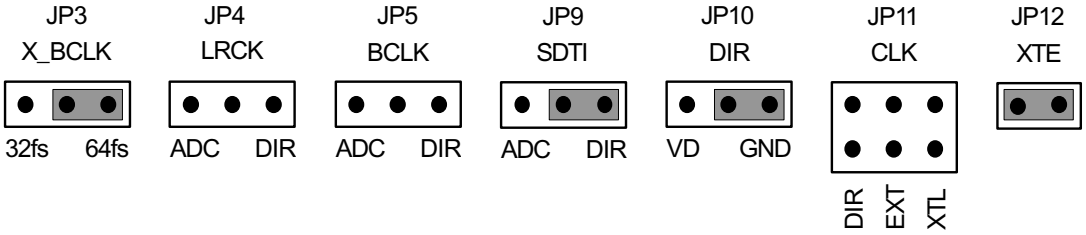
3) Evaluation of D/A using DIR. (Optical link)

PORT4 (DIR) is used. DIR generates MCLK, BCLK, LRCK and SDATA from the received data through optical connector (TORX176). Used for the evaluation using CD test disk. Nothing should be connected to PORT1 and PORT3.



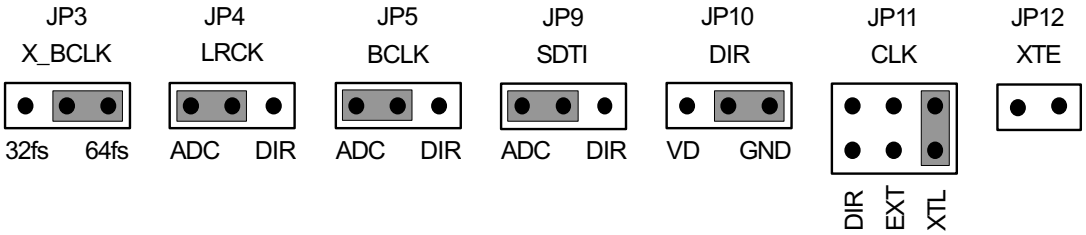
4) Evaluation of A/D using D/A converted data.

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's D/A evaluation boards with PORT3. MCLK, BCLK and LRCK are sent from AKM's D/A evaluation board to AKD4565. Nothing should be connected to PORT4. When SDTO0 is supplied via PORT1, JP8 (SD0/1) selects SD0 side. When SDTO1 is supplied via PORT1, JP8 (SD0/1) selects SD1 side.



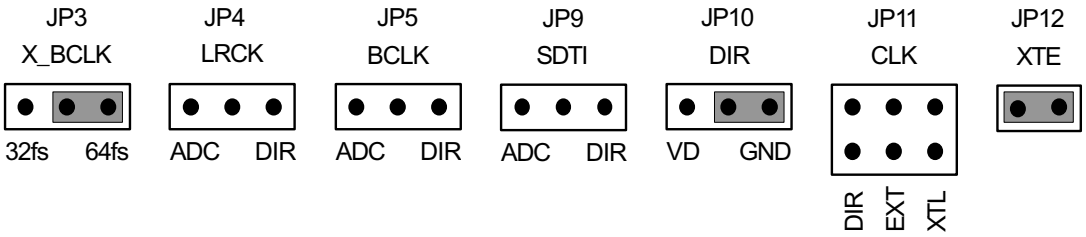
5) Evaluation of A/D using DIT. (Optical link)

PORT1 (DIT) is used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX176). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier which equips DIR input. Nothing should be connected PORT3 and PORT4. In case of using external clock through a BNC connector (J1), select EXT on JP11 (CLK) and short JP12 (XTE). When SDTO0 is supplied via PORT1, JP8 (SD0/1) selects SD0 side. When SDTO1 is supplied via PORT1, JP8 (SD0/1) selects SD1 side.



6) All interfacing signals (MCLK, BCLK, LRCK) are fed from the external circuit through PORT3.

Under the following set up, all external signals needed for the AK4565 to operate could be fed through PORT3. In case of interfacing external sources to D/A converter, JP7 (SDTO) should be open. And in case of using A/D data to externally, JP9 (SDTI) is set ADC side. When JP9 (SDTI) is open, the A/D data can be output from the PORT3, if JP7 (SDTO) is short.



■ DIP Switch set up

[SW3] (MODE): Setting evaluation mode of CS8412(DIR)
ON is "1", OFF is "0".

AK4565		MODE	SW3			JP6
DIF1	DIF0		M0	M1	M2	
0	0	16bit LSB justified	1	0	1	THR
0	1	20bit LSB justified	N/A			
1	0	20bit MSB justified	0	0	0	INV
1	1	I^2S Compatible	0	1	0	THR

Table 2. AK4565 audio data I/F format and SW3 and JP6 Setting

SW3 and AK4565 format must be the same audio data format.

■ Other jumper pins set up

1. JP1 (GND) : Analog ground and Digital ground
   OPEN : Separated.
   SHORT : Common. (The connector "DGND" can be open.) <Default>

2. JP2 (VT) : D2V and VT
   OPEN : Separated. <Default>
   SHORT : Common. (The connector "VT" can be open.)

3. JP6 (PHASE) : Phase of BCLK using DIR
   THR : BCLK is coincides with AK4565. (16bit LSB justified and I^2S compatible for DAC.)
   INV : BCLK is inverted. (20bit MSB justified for DAC.)

4. JP7 (SDTO) : When JP9 (SDTI) is open, the A/D data can be output from the PORT3.
   *Always open. When evaluation mode is "6)", JP7 can be short.

5. JP8 (SD0/1) : Select SDTO0 or SDTO1
   SD0 : Select SDTO0.
   SD1 : Select SDTO1.

■ The function of the toggle SW

Upper-side is "H" and lower-side is "L".

[SW1] (PDN): Power down of the AK4565. Keep "H" during normal operation.

[SW2] (DIT): Power down of the AK4353. Keep "H" during normal operation.

■ Indication for LED

[LED1] (VERF): Monitor VERF pin of the CS8412. LED turns on when some error has occurred to the CS8412.

[LED2] (PREM): Indicate whether the input data of the CS8412 is pre-emphasized or not.

■ Serial Control

The AK4565 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT2 (CTRL) with PC by 10 wire flat cable packed with the AKD4565.

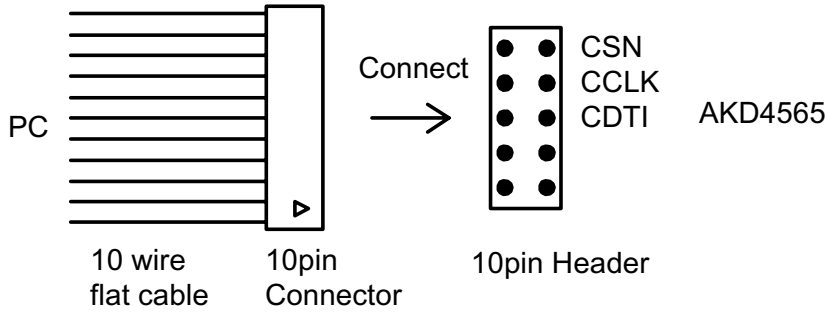


Figure 2. Connect of 10-wire flat cable

■ Input / Output circuits & Set-up jumper pin for Input / Output circuits

(1) Input circuits

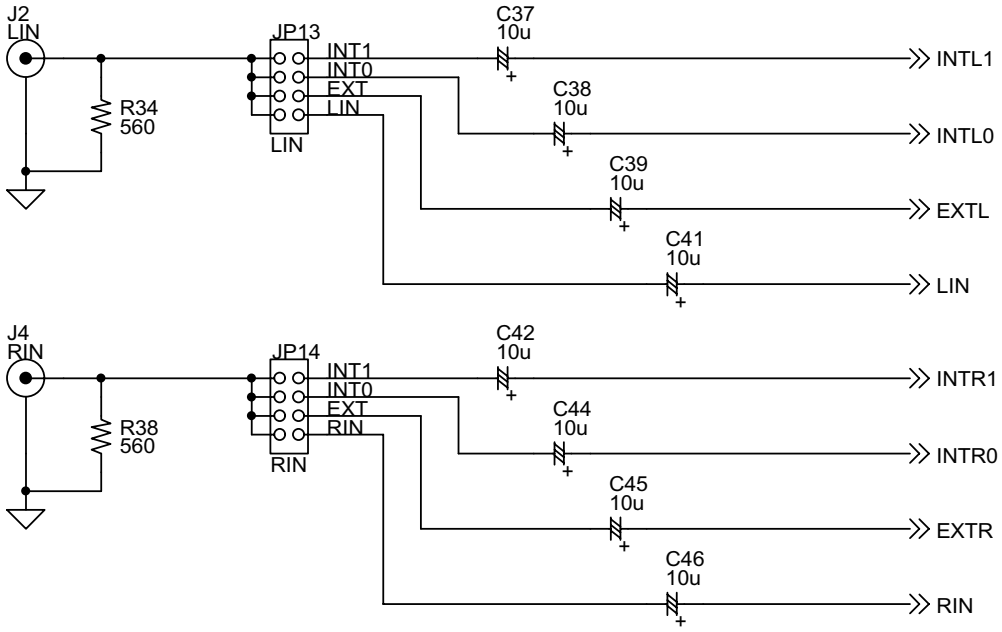
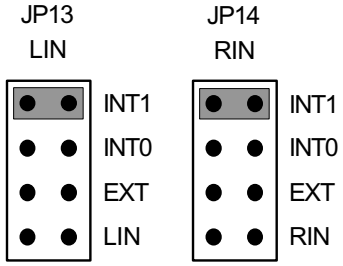
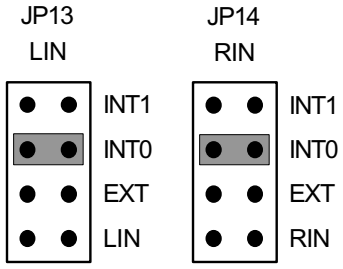


Figure 3. LIN/RIN Input circuits

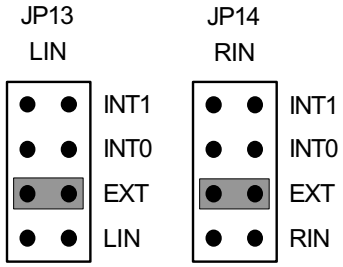
1. Analog signal is input to INTL1 and INTR1 pins via J2 and J4 connectors.



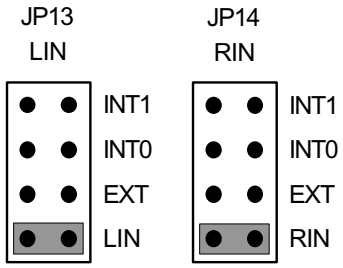
2. Analog signal is input to INTL0 and INTR0 pins via J2 and J4 connectors.



3. Analog signal is input to EXTL and EXTR pins via J2 and J4 connectors.



4. Analog signal is input to LIN and RIN pins via J2 and J4 connectors.



(2) Output circuits

Analog signal is output to LOUT and ROUT pins via J3 and J5 connectors.

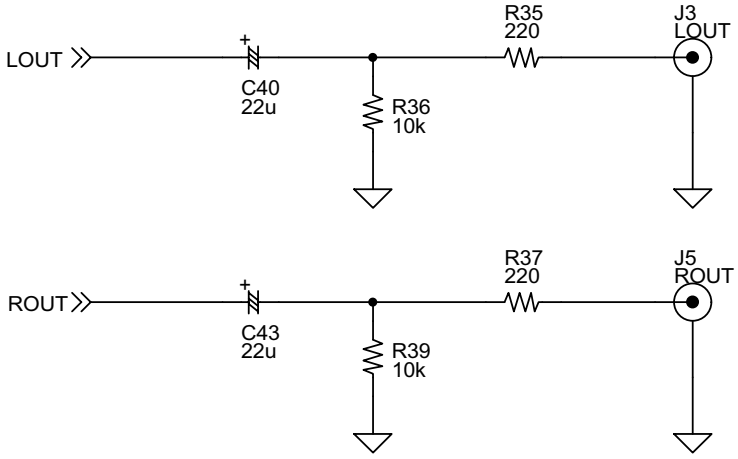


Figure 4. LOUT/ROUT output circuits

* AKM assumes no responsibility for the trouble when using the above circuit examples.

CONTROL SOFTWARE MANUAL

■ Set-up of evaluation board and control software

1. Set up the AKD4565 according to previous term.

2. Connect IBM-AT compatible PC with AKD4565 by 10-line type flat cable (packed with AKD4565). Take care of the direction of 10pin header. (This control software does not operate on Windows NT, therefore please operate it on Windows95/98.)

3. Insert the floppy-disk labeled "AKD4565 Control Program ver 1.0" into the floppy-disk drive.

4. Access the floppy-disk drive and double-click the icon of "akd4565.exe" to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following operation flow.

1. Set up the control program according to explanation above.
2. Click "Port Setup" button.
3. Click "Write default" button.
4. Set up evaluation mode of AK4353.
5. Then set up the dialog and input data.

■ Explanation of each buttons

(1) AK4565 control

1. [Port Setup] : Set up the printer port.
2. [Write default] : Initialize the register of AK4565.
3. [Read]: Dialog to read data by keyboard operation.
4. [Function1] : Dialog to write data by keyboard operation.
5. [Function2] : Dialog to evaluate IPGA.
6. [Write] : Dialog to write data by mouse operation.

(2) AK4353 control

1. [MSB] : MSB justified for DIT mode in AK4353.
2. [LSB] : LSB justified for DIT mode in AK4353.
   When the AK4565 is selected to 20bit MSB justified and BICK=32fs, this mode is used.
3. [I2S] : I^2S compatible for DIT mode in AK4353.

Note 1. Evaluation mode of AK4353 and AK4565 is the same mode. For example, when the AK4565 is evaluated by I^2S compatible mode in audio data I/F format, please click "I2S" button.

Note 2. The default of AK4353 is MCLK=256fs and I^2S compatible mode.

Note 3. MCLK of AK4353 is fixed to 256fs.

■ Explanation of each dialog

1. [Read Dialog] : Dialog to write data by keyboard operation

   Address Box: Input register address in 2 figures of hexadecimal.

   If you want to write the input data to AK4565, click “OK” button. If not, click “Cancel” button.

2. [Function1 Dialog] : Dialog to write data by keyboard operation

   Address Box: Input register address in 2 figures of hexadecimal.
   Data Box: Input register data in 2 figures of hexadecimal.

   If you want to write the input data to AK4565, click “OK” button. If not, click “Cancel” button.

3. [Function2 Dialog] : Dialog to evaluate IPGA

   This dialog corresponds to only addr=07H.

   Address Box: Input register address in 2 figures of hexadecimal.
   Start Data Box: Input start data in 2 figures of hexadecimal.
   End Data Box: Input end data in 2 figures of hexadecimal.
   Interval Box: Data is written to AK4565 by this interval.
   Step Box: Data changes by this step.
   Mode Select Box:
   If you check this check box, data reaches end data, and returns to start data.
   [Example] Start Data = 00, End Data = 09
   Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

   If you do not check this check box, data reaches end data, but does not return to start data.
   [Example] Start Data = 00, End Data = 09
   Data flow: 00 01 02 03 04 05 06 07 08 09

   If you want to write the input data to AK4565, click “OK” button. If not, click “Cancel” button.

4. [Write Dialog] : Dialog to write data by mouse operation

   There are dialogs corresponding to each register.

   Click the “Write” button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

   If you want to write the input data to AK4565, click “OK” button. If not, click “Cancel” button.

■ Indication of data

Input data is indicated on the register map. Red letter indicates “H” or “1” and blue one indicates “L” or “0”. Blank is the part that is not defined in the datasheet.

■ Attention on the operation

If you set up Function1 or Function2 dialog, input data to all boxes. Attention dialog is indicated if you input data or address that is not specified in the datasheet or you click “OK” button before you input data. In that case set up the dialog and input data once more again. These operations does not need if you click “Cancel” button or check the check box.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit: Audio Precision, System Two
- MCLK : 256fs
- BCLK : 64fs
- fs : 48kHz
- Bit : 20bit
- Power Supply : VA=VD=VT=2.5V
- Interface : DIR/DIT
- Temperature : Room

[Measurement Results]

Parameter		Input Pin	Result (Lch / Rch)	Unit
ADC Analog Input Characteristics				
S/(N+D)	(-2.0dB Input)	INTL0 / INTR0	86.2 / 86.2	dB
		INTL1 / INTR1	86.1 / 86.2	dB
		EXTL / EXTR	86.2 / 86.1	dB
		LIN / RIN	85.7 / 85.7	dB
D-Range	(A-weighted)	INTL0 / INTR0	88.8 / 88.9	dB
		INTL1 / INTR1	88.8 / 88.9	dB
		EXTL / EXTR	88.7 / 88.8	dB
		LIN / RIN	88.3 / 88.3	dB
S/N	(A-weighted)	INTL0 / INTR0	88.8 / 88.9	dB
		INTL1 / INTR1	88.6 / 88.8	dB
		EXTL / EXTR	88.7 / 88.9	dB
		LIN / RIN	88.3 / 88.2	dB
Interchannel Isolation		INTL0 / INTR0	110.7 / 110.0	dB
		INTL1 / INTR1	110.2 / 110.3	dB
		EXTL / EXTR	110.4 / 110.5	dB
		LIN / RIN	107.0 / 108.0	dB
DAC Analog Output Characteristics				
S/(N+D)		-	88.5 / 88.5	dB
D-Range	(A-weighted)	-	91.9 / 91.5	dB
S/N	(A-weighted)	-	92.5 / 92.7	dB
Interchannel Isolation		-	108.1 / 107.9	dB

[ADC Plot]

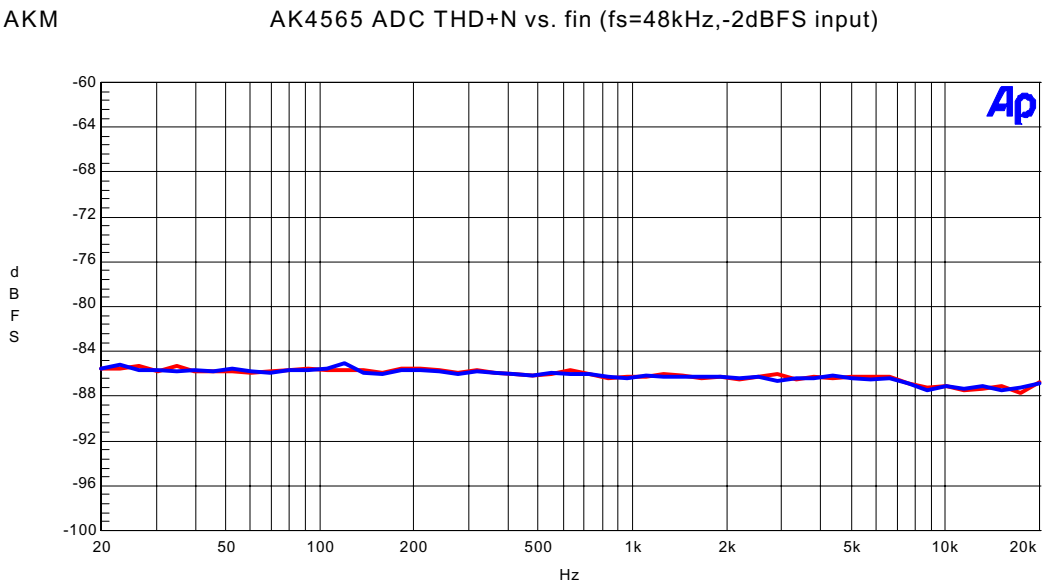


Figure 5. THD+N vs. Input Frequency

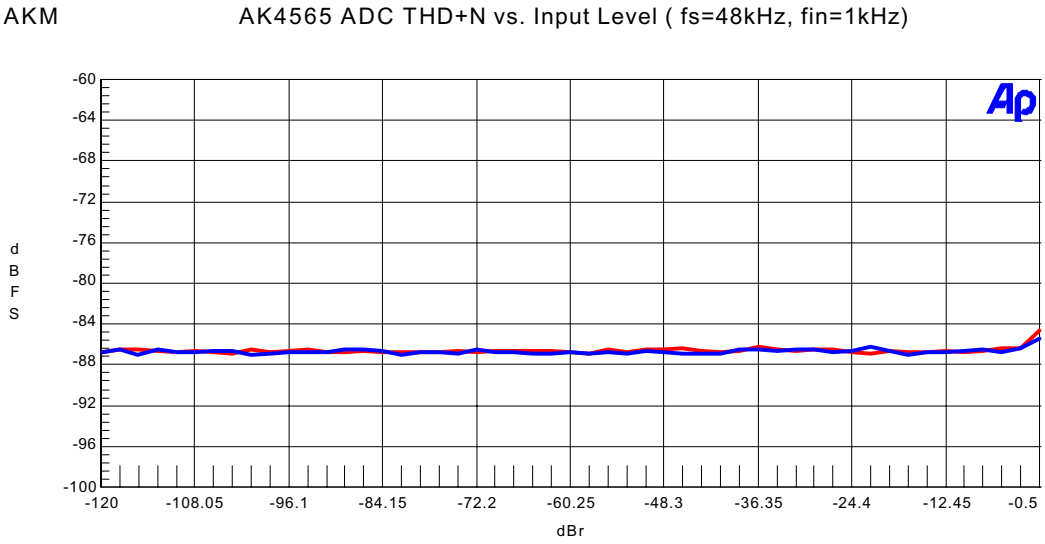


Figure 6. THD+N vs. Input Level

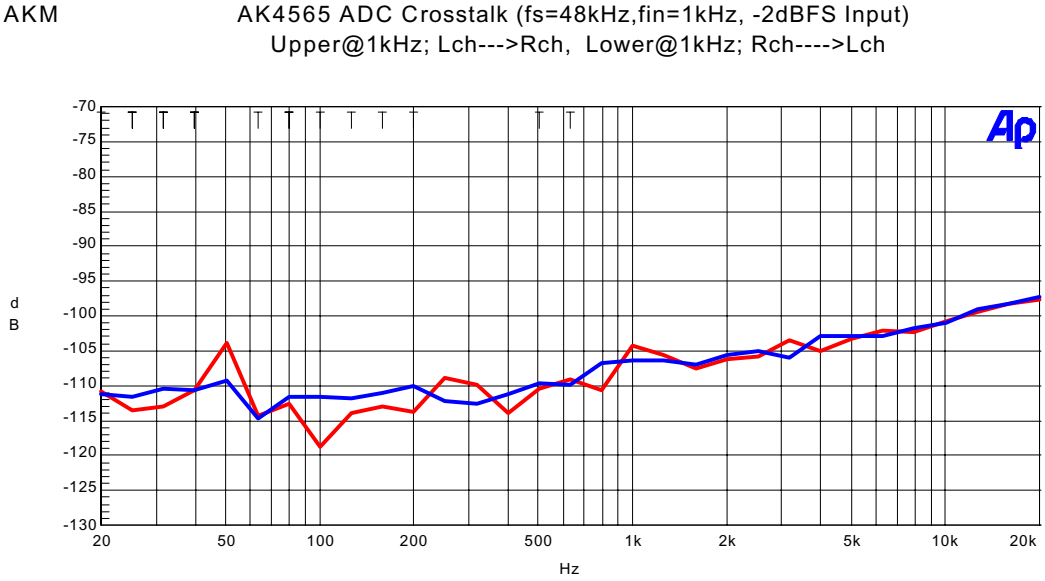


Figure 7. Crosstalk

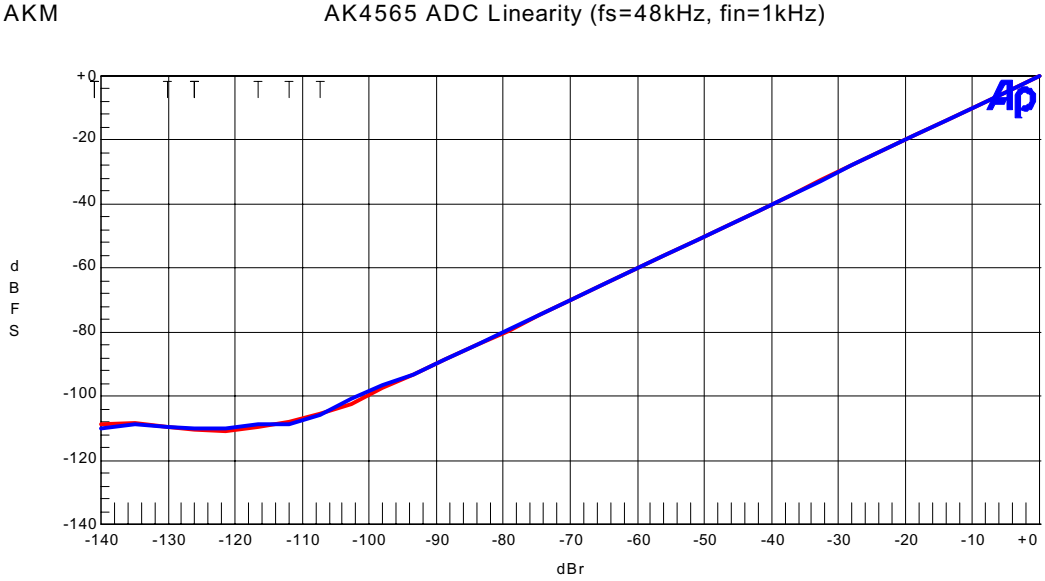


Figure 8. Linearity

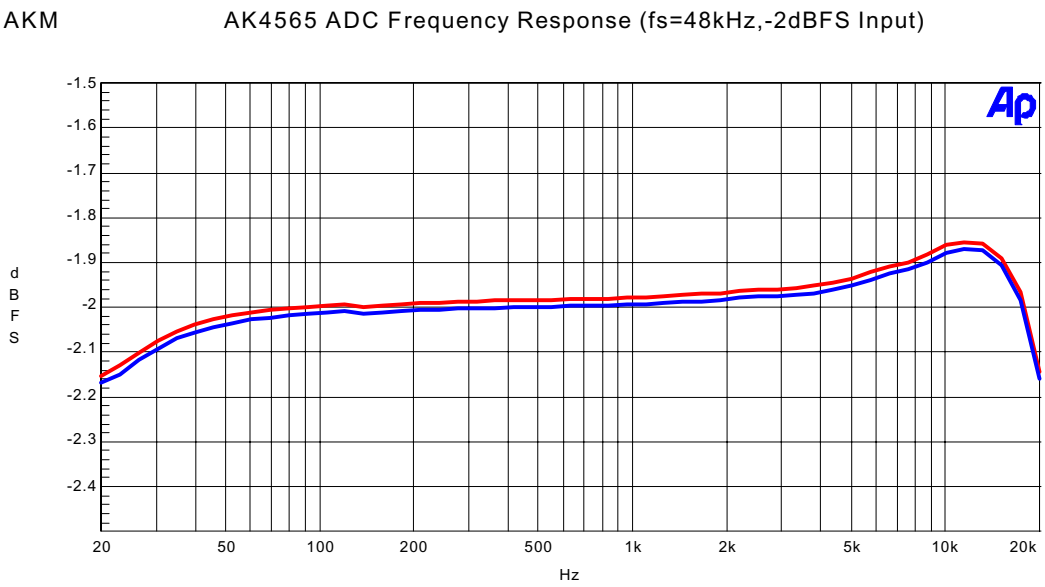


Figure 9. Frequency Response

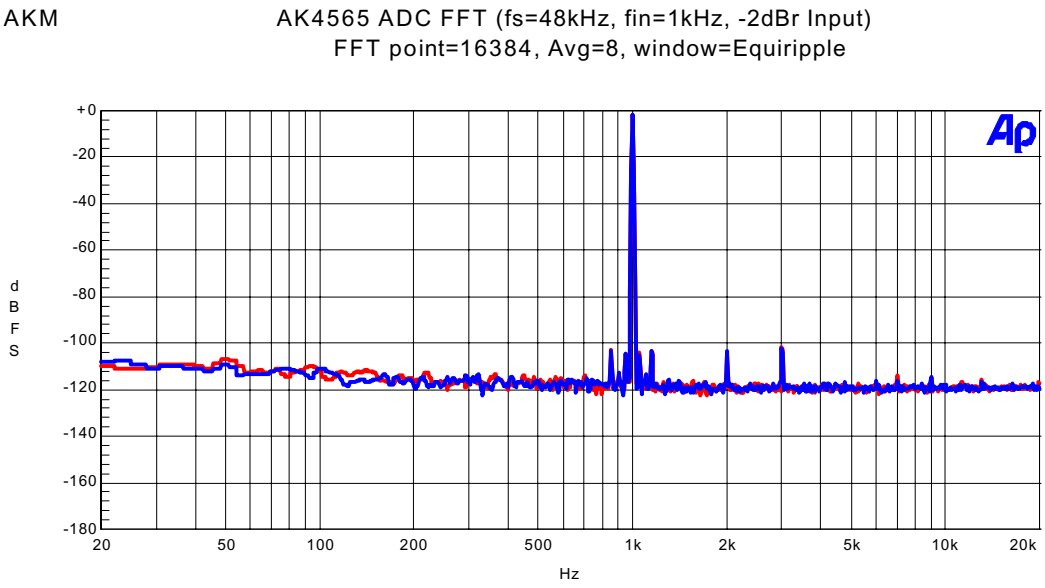


Figure 10. FFT plot

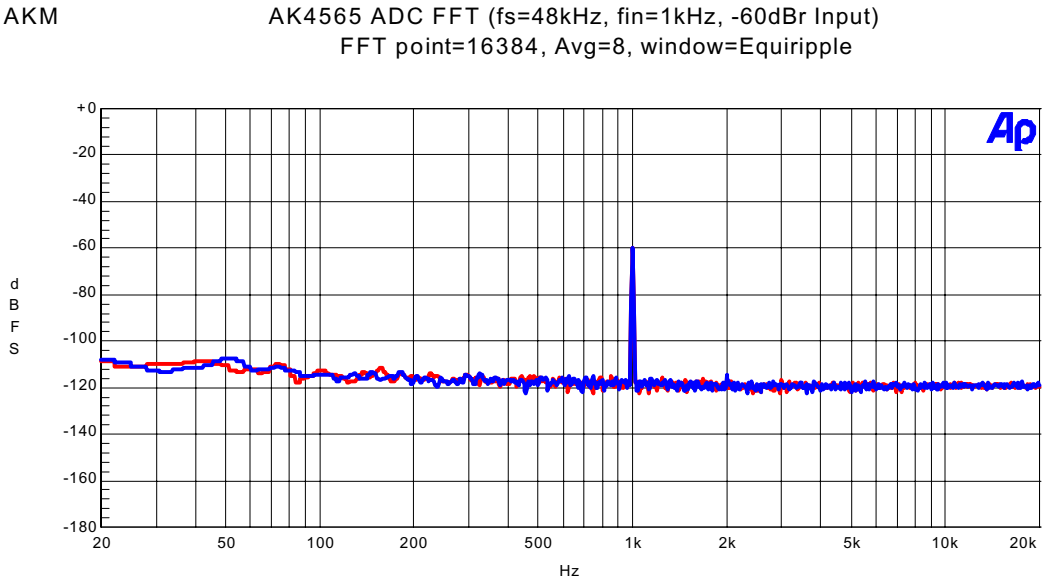


Figure 11. FFT plot

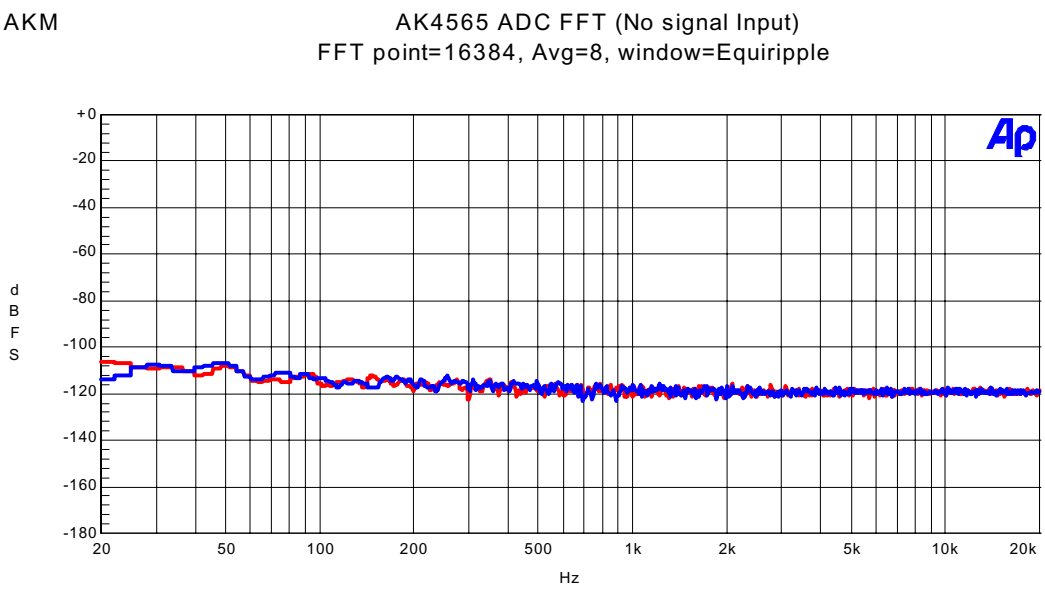


Figure 12. FFT plot

[DAC Plot]

AKM AK4565 DAC THD+N vs. Input Frequency (fs=48kHz, input level=0dBFS)

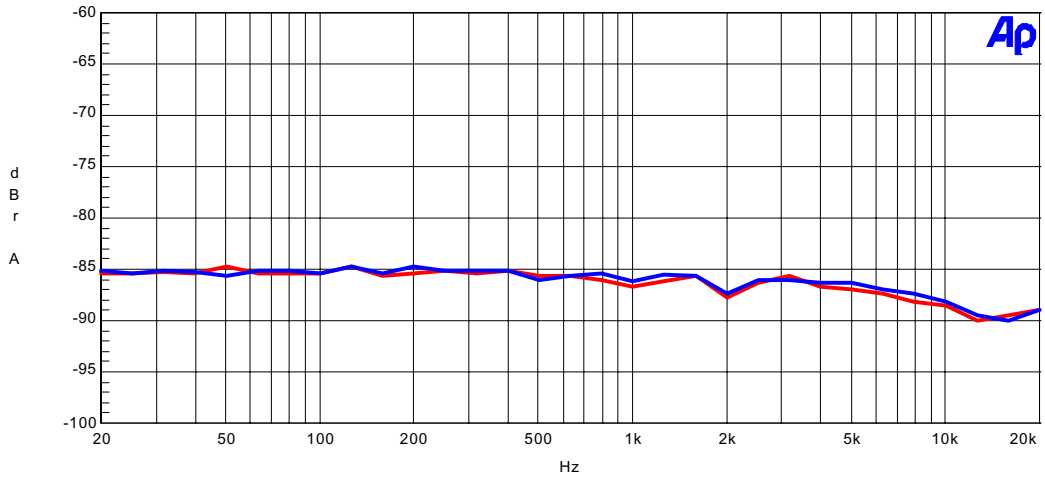


Figure 13. THD+N vs. Frequency

AKM AK4565 DAC THD+N vs. Input Lever (fs=48kHz, fin=1kHz)

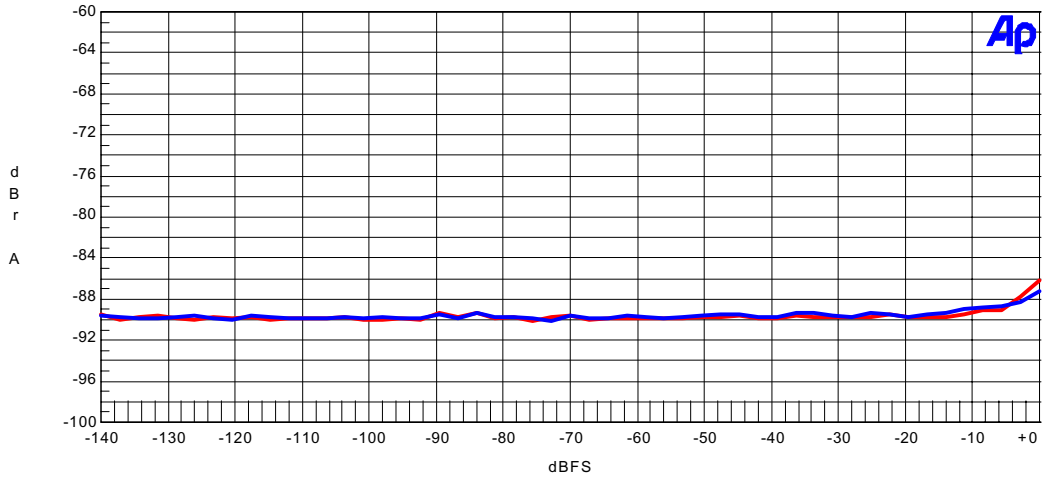


Figure 14. THD+N vs. Input Level

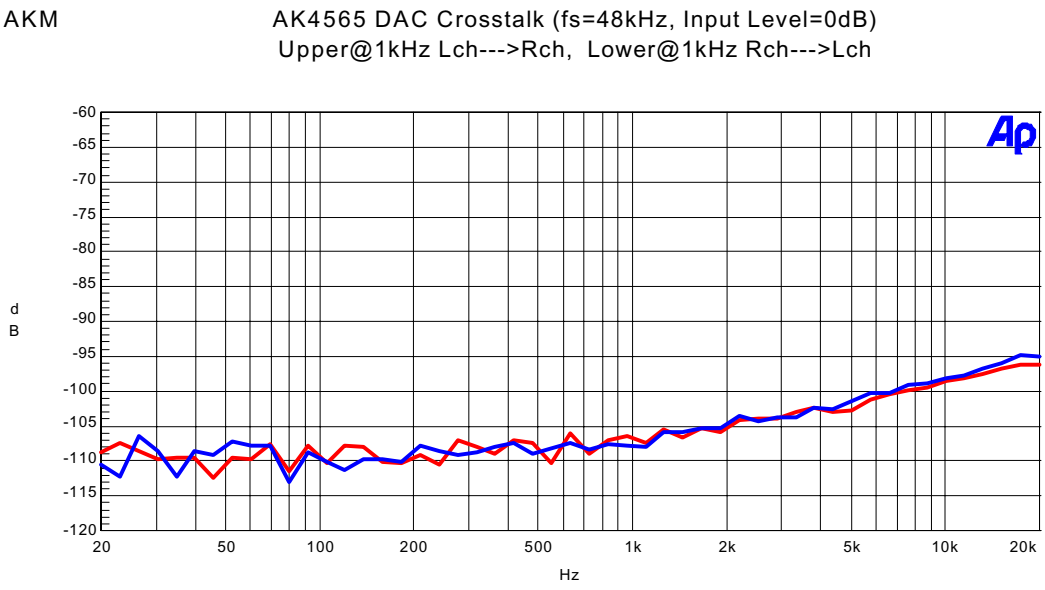


Figure 15. Crosstalk

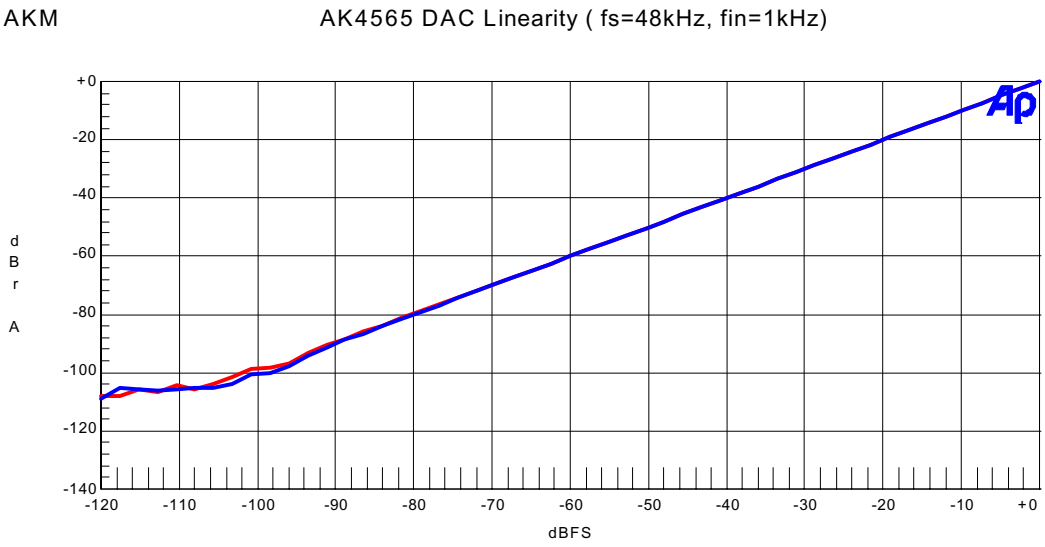


Figure 16. Linearity

AKM AK4565 DAC Frequency Response (fs=48kHz, Input Level=0dB)

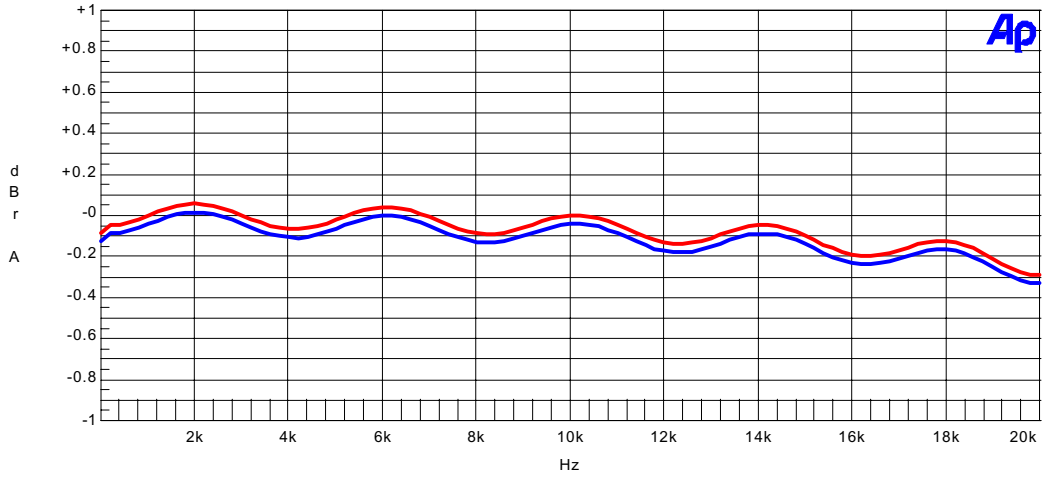


Figure 17. Frequency Response

AKM AK4565 DAC FFT (fs=48kHz, fin=1kHz, 0dBFS Input)
FFT point=16384, Avg=8, window=Equiripple

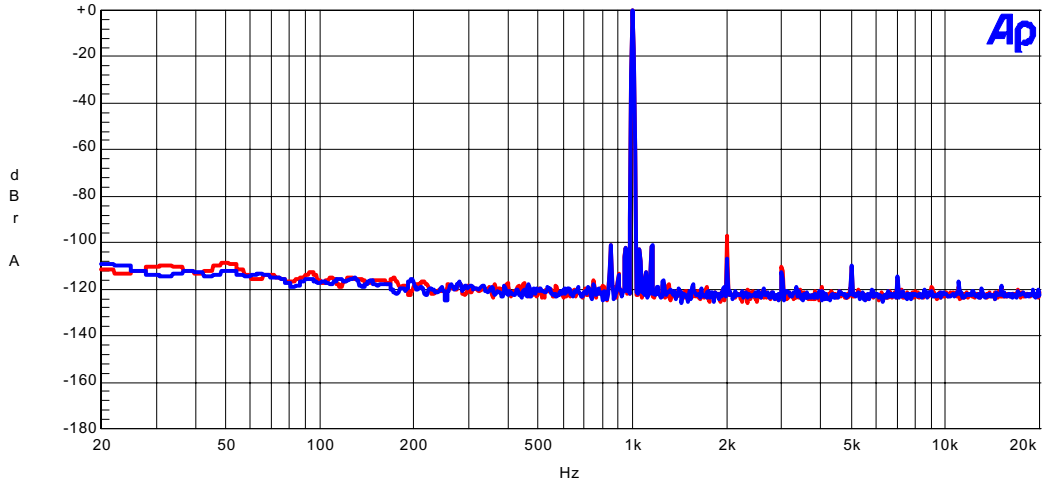


Figure 18. FFT plot

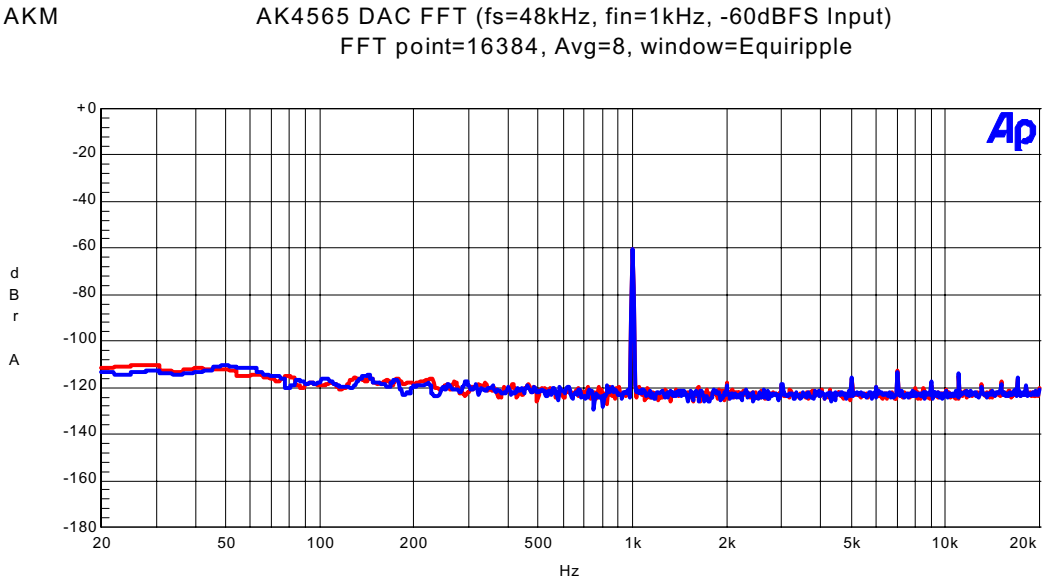


Figure 19. FFT plot

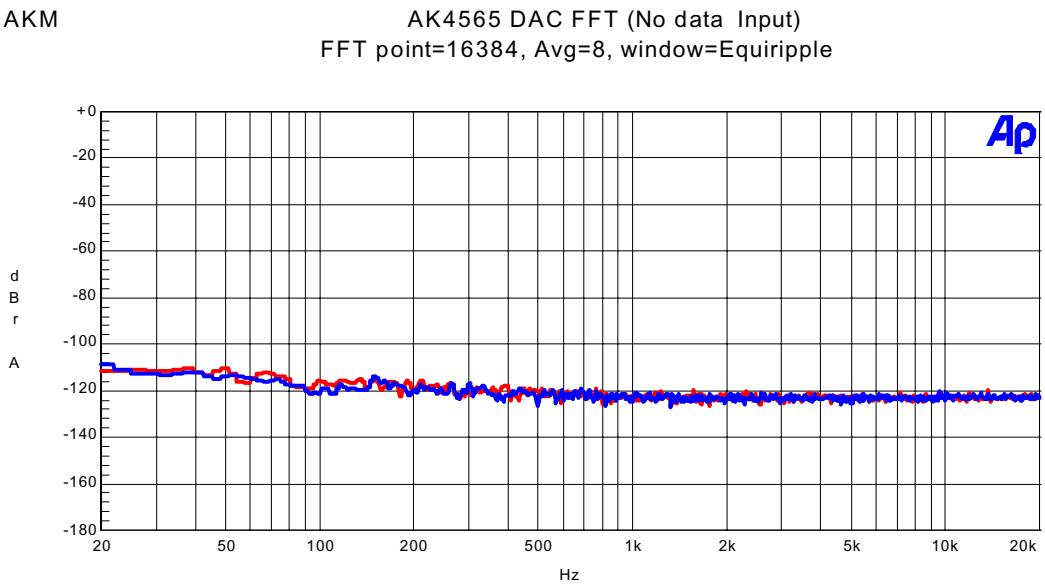


Figure 20. FFT plot

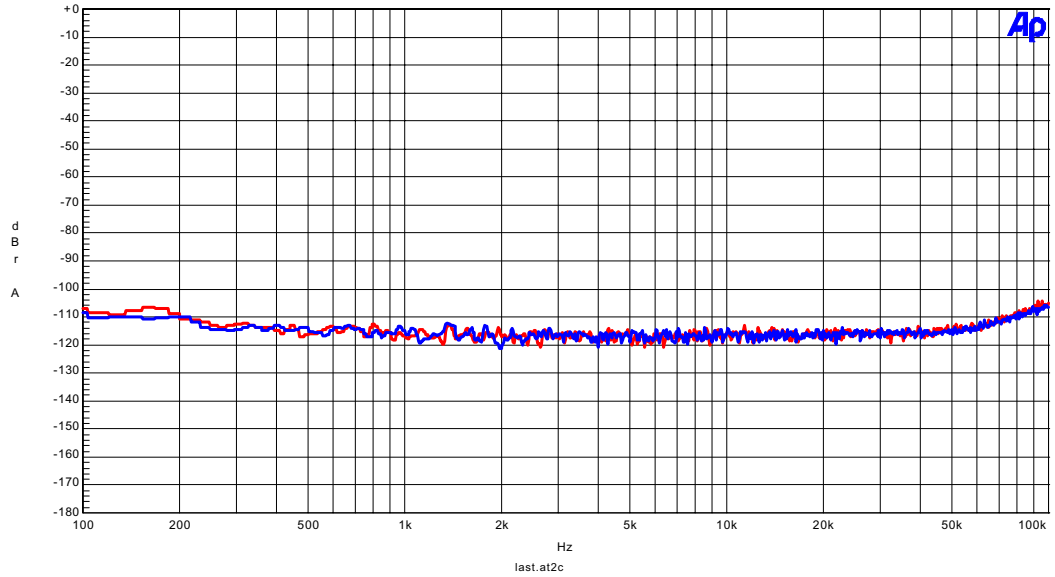
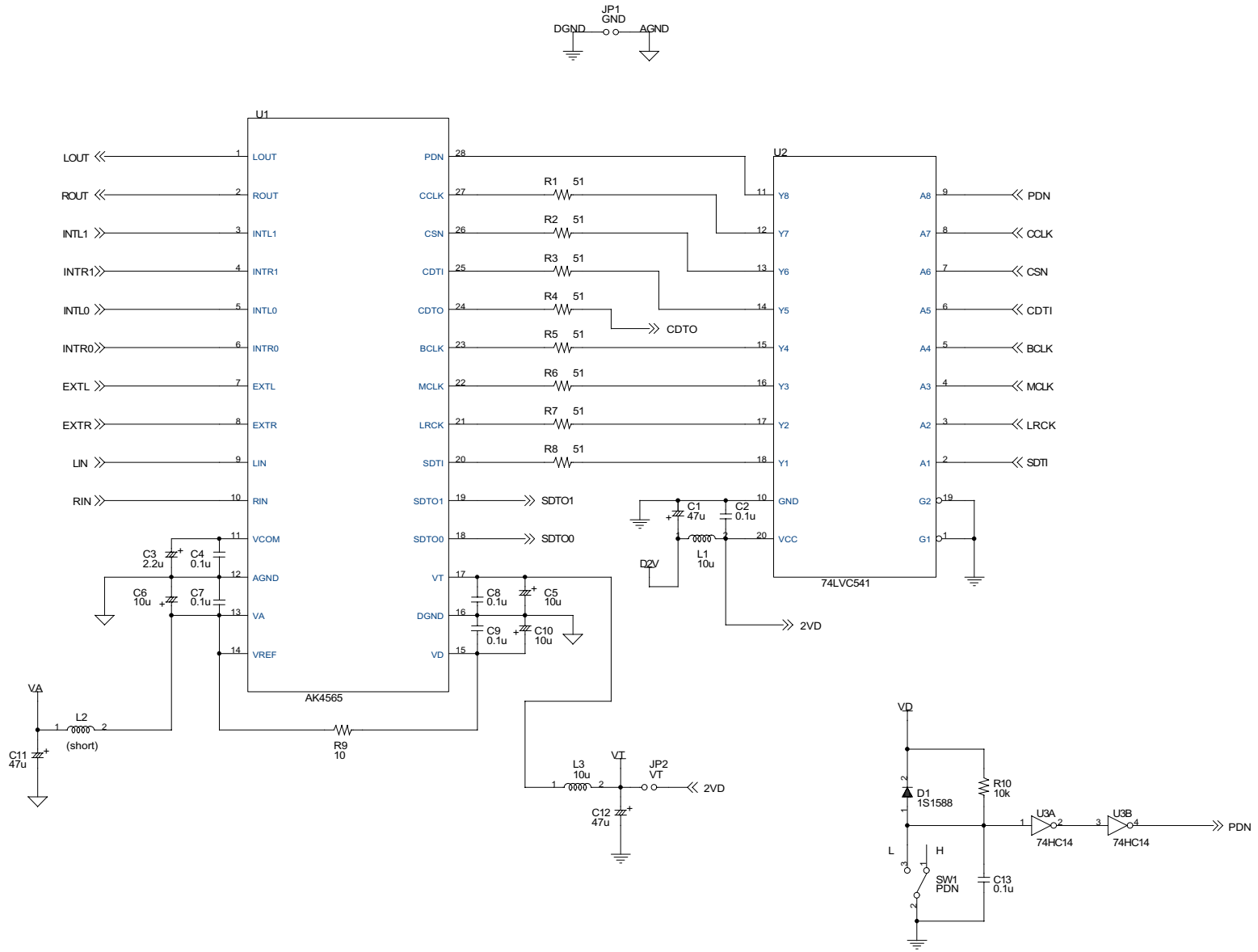
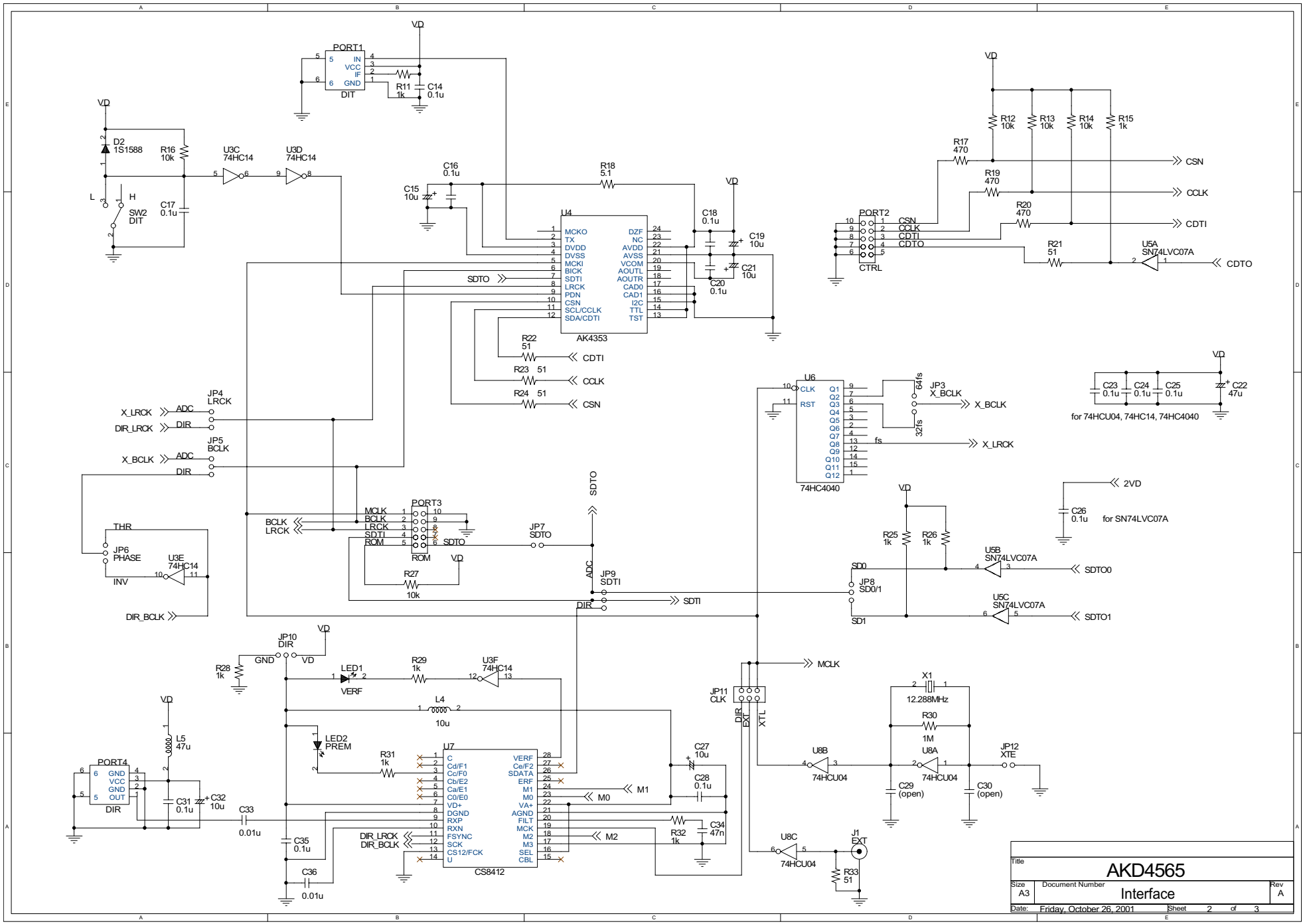
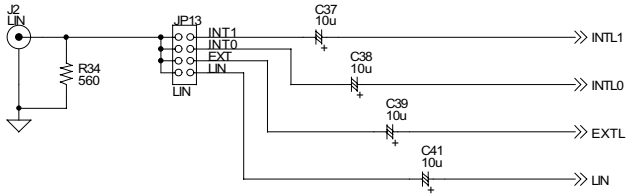
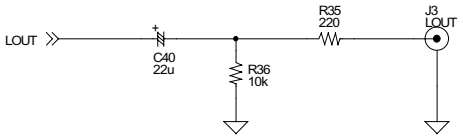


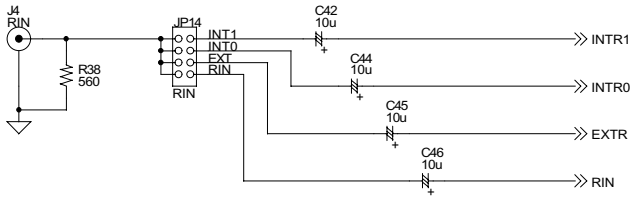
Figure 21. FFT plot (Out-of-band Noise)

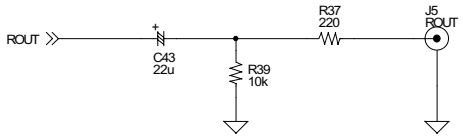

JP1
GND
DGND
AGND
U1
LOUT
ROUT
INTL1
INTR1
INTL0
INTR0
EXTL
EXTR
LIN
RIN
LOUT
ROUT
INTL1
INTR1
INTL0
INTR0
EXTL
EXTR
LIN
RIN
VCOM
AGND
VA
VREF
PDN
CCLK
CSN
CDTI
CDTO
BCLK
MCLK
LRCK
SDTI
SDTO1
SDTO0
VT
DGND
VD
AK4565
R1 51
R2 51
R3 51
R4 51
R5 51
R6 51
R7 51
R8 51
CDTO
SDTO1
SDTO0
U2
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
GND
VCC
A8
A7
A6
A5
A4
A3
A2
A1
G2
G1
PDN
CCLK
CSN
CDTI
BCLK
MCLK
LRCK
SDTI
74LVC541
C1 47u
C2 0.1u
L1 10u
D2V
2VD
C3 2.2u
C4 0.1u
C6 10u
C7 0.1u
C8 0.1u
C5 10u
C9 0.1u
C10 10u
VA
L2
(short)
C11 47u
R9 10
L3 10u
VT
JP2
VT
2VD
C12 47u
VD
D1 1S1588
R10 10k
U3A
U3B
74HC14
74HC14
PDN
L
H
SW1
PDN
C13 0.1u
Title
AKD4565
Size
A3
Document Number
AK4565
Rev
A
Date: Friday, October 26, 2001
Sheet 1 of 3

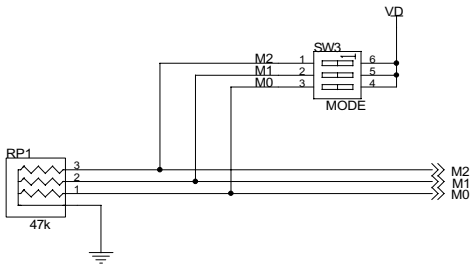

PORT1
DIT
R11 1k
C14 0.1u
D2 1S1588
R16 10k
U3C 74HC14
U3D 74HC14
SW2 DIT
C17 0.1u
C16 0.1u
C15 10u
R18 5.1
U4
AK4353
C18 0.1u
C19 10u
C21 10u
C20 0.1u
SDTO
R22 51
R23 51
R24 51
CDTI
CCLK
CSN
R12 10k
R13 10k
R14 10k
R15 1k
R17 470
R19 470
R20 470
PORT2
CTRL
R21 51
U5A SN74LVC07A
CDTO
JP4 LRCK
JP5 BCLK
X_LRCK
DIR_LRCK
X_BCLK
ADC
DIR
U6
74HC4040
64fs
32fs
fs
JP3 X_BCLK
X_LRCK
C23 0.1u
C24 0.1u
C25 0.1u
C22 47u
for 74HCU04, 74HC14, 74HC4040
THR
JP6 PHASE
INV
U3E 74HC14
DIR_BCLK
PORT3
ROM
R27 10k
JP7 SDTO
JP9 SDTI
ADC
DIR
SDTI
R25 1k
R26 1k
U5B SN74LVC07A
U5C SN74LVC07A
SD0
SD1
JP8 SD0/1
SDTO0
SDTO1
2VD
C26 0.1u
for SN74LVC07A
JP10 DIR
R28 1k
LED1 VERF
R29 1k
U3F 74HC14
L4 10u
LED2 PREM
R31 1k
L5 47u
PORT4
C31 0.1u
C32 10u
C33 0.01u
C35 0.1u
C36 0.01u
U7
CS8412
DIR_LRCK
DIR_BCLK
M0
M1
M2
C27 10u
C28 0.1u
C34 47n
R32 1k
JP11 CLK
DIR
EXT
XTL
MCLK
X1 12.288MHz
R30 1M
U8A 74HCU04
U8B 74HCU04
U8C 74HCU04
C29 (open)
C30 (open)
JP12 XTE
J1 EXT
R33 51
Title
AKD4565
Size A3
Document Number
Interface
Rev A
Date: Friday, October 26, 2001
Sheet 2 of 3

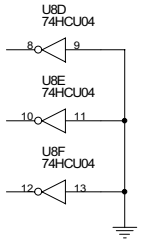


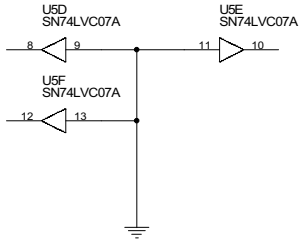




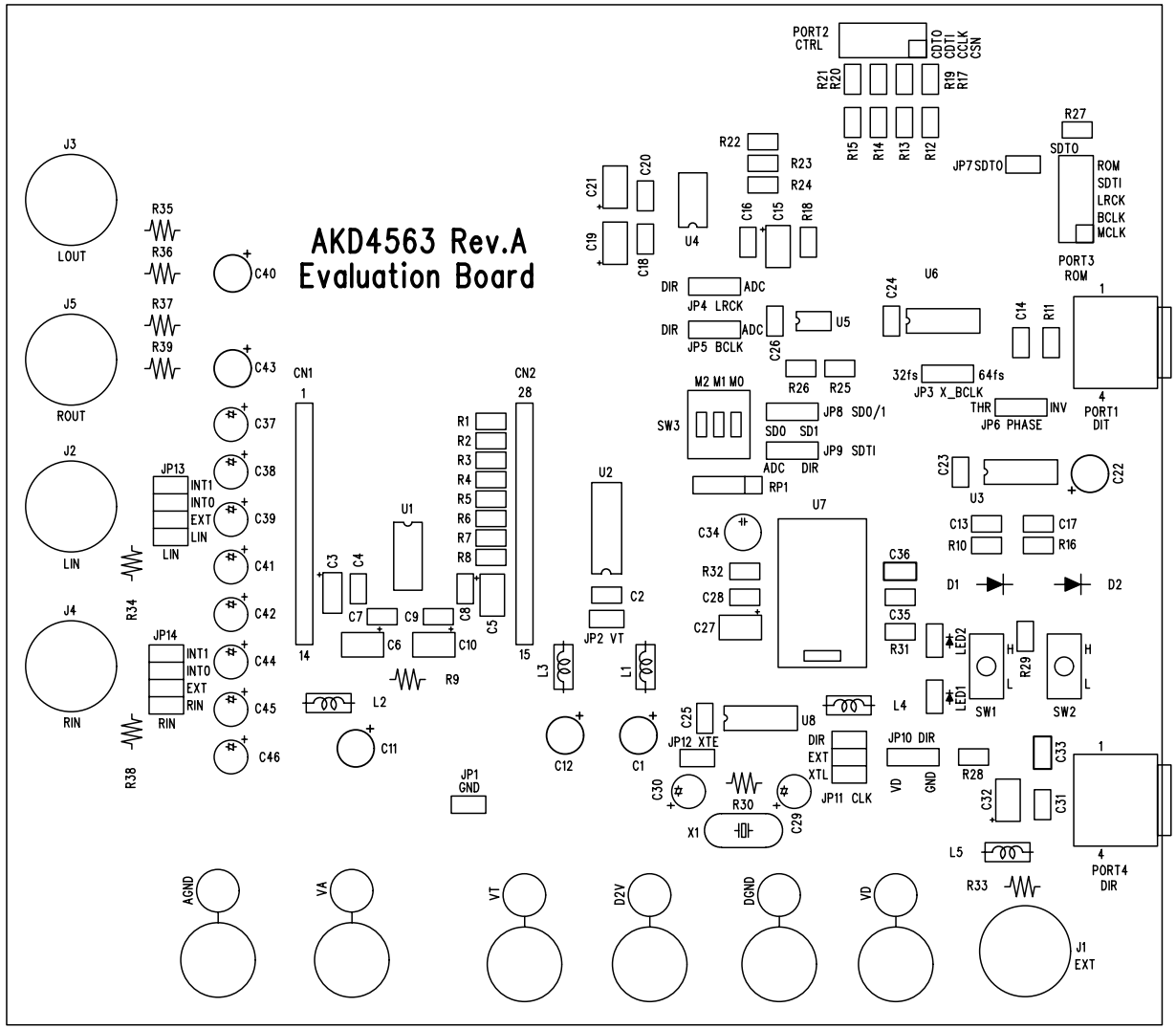




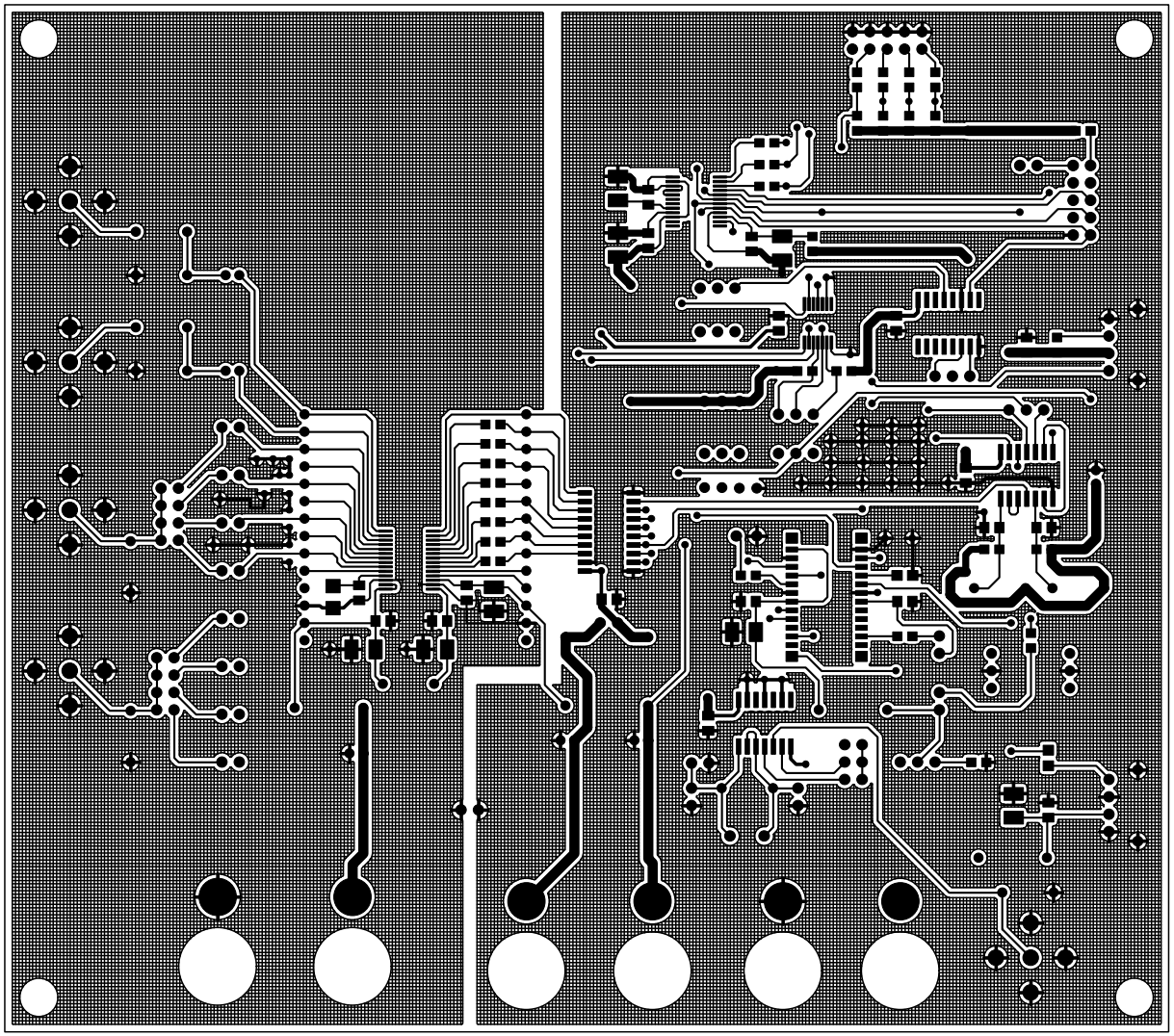




Title	AKD4565	
Size: A3	Document Number: Input/Output	Rev: A
Date: Friday, October 26, 2001	Sheet 3 of 3	



5A1495 部品面シルク



5A1495 部品面パターン

半田面パターン 2SA1962

IMPORTANT NOTICE

- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  a. A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  b. A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.