AKD4520A

Evaluation board Rev.B for AK4520A

General description

AKD4520A is an evaluation board for the digital stereo audio 20bit A/D and D/A converter, AK4520A. The A/D converter section includes the input buffer circuits. The AKD4520A can evaluate A/D converter and D/A converter separately in addition to loopback mode(A/D → D/A). The A/D section can be evaluated by interfacing with AKM's DAC evaluation boards(AKD4328, AKD4319, AKD4320 and AKD4321) directly. The AKD4520A has the interface with AKM's wave generator using ROM data and AKM's ADC evaluation boards (AKD5391, AKD5390, AKD5350 and AKD5352/1). Therefore, it is easy to evaluate the D/A section. The AKD4520A also has the digital audio interface and can achieve the interface with digital audio systems via opt-connecter.

■ Ordering guide

AKD4520A --- Evaluation board for AK4520A

Function

- ☐ On-Board analog input buffer circuit
- ☐ On-board clock generator
- ☐ Compatible with the following 2 types of interface
  - 1)Direct interface with AKM's A/D and D/A converter, and direct interface with a signal generator(AKD43XX) by 10pin Header
  - 2)DIT/DIR with optical input/output
- ☐ A BNC connector for an external clock input

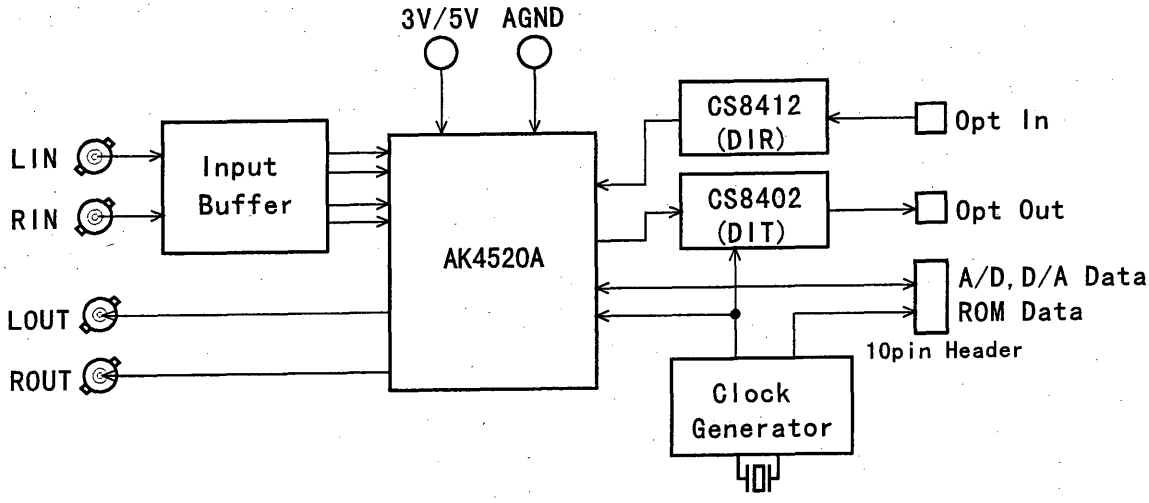
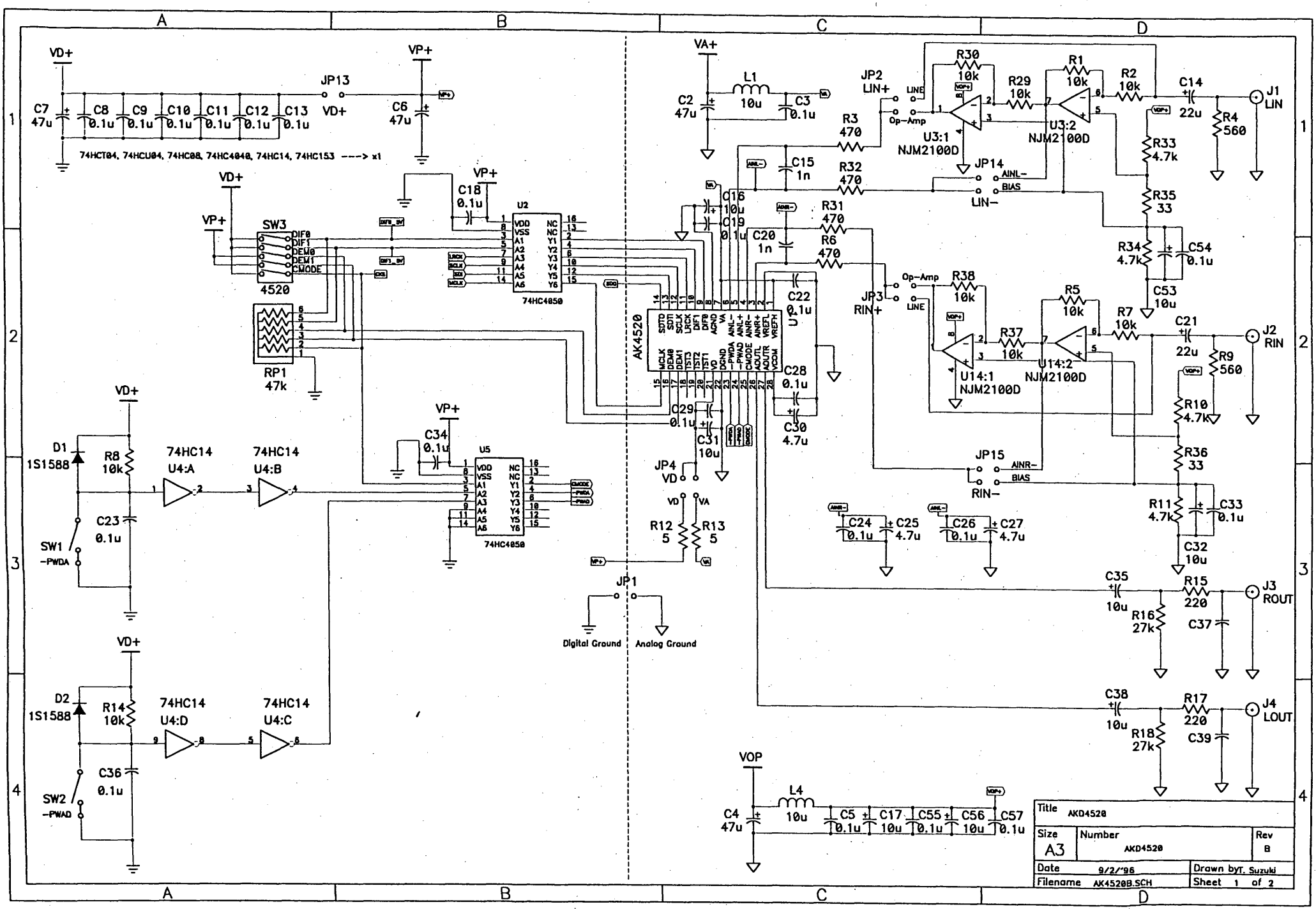
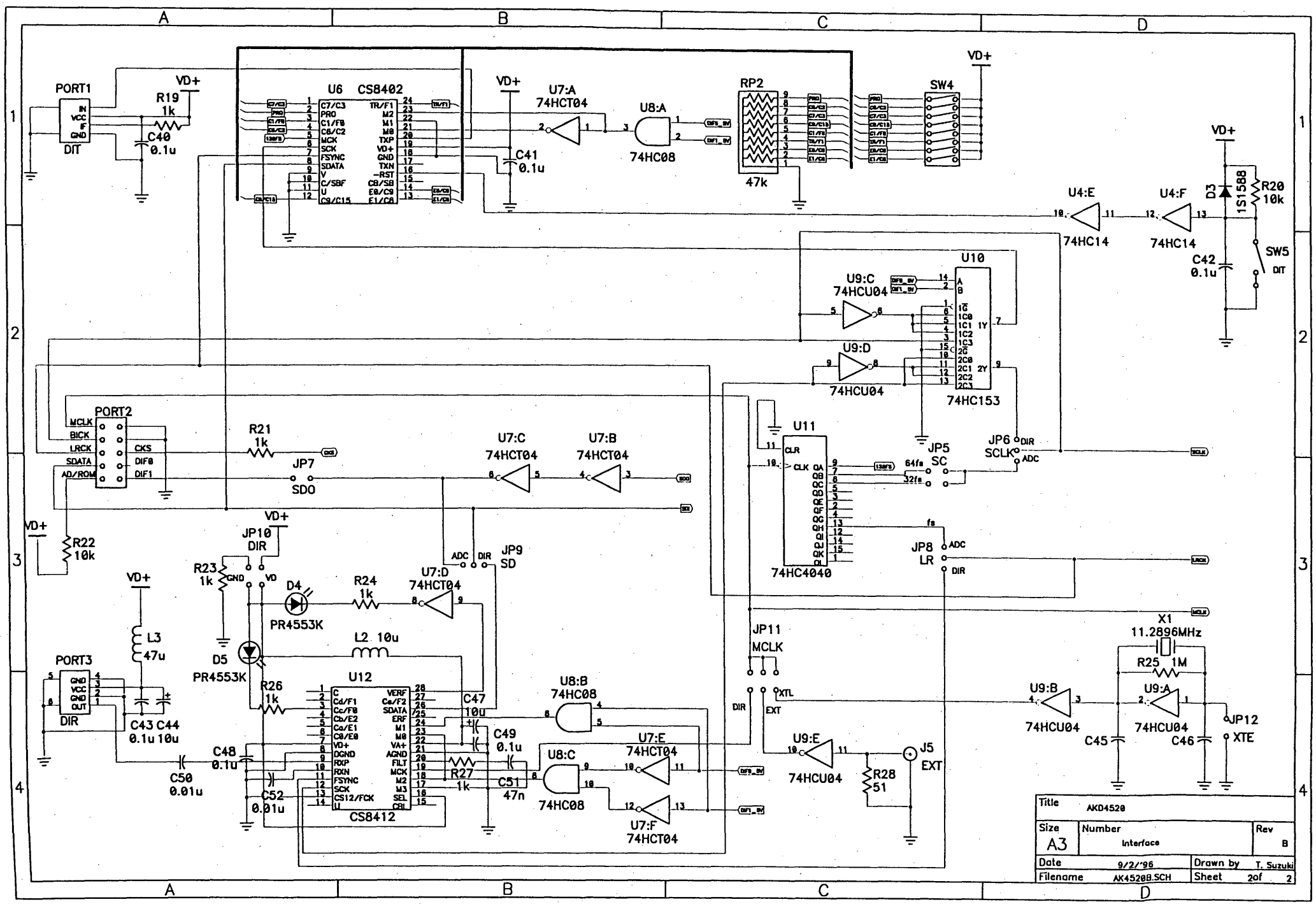


Figure 1. AKD4520A Block Diagram


VD+
VP+
VA+
JP13
C7 47u
C8 0.1u
C9 0.1u
C10 0.1u
C11 0.1u
C12 0.1u
C13 0.1u
C6 47u
74HCT04, 74HCU04, 74HC08, 74HC4040, 74HC14, 74HC153 ---> x1
L1 10u
C2 47u
C3 0.1u
JP2 LIN+
Op-Amp
LINE
R30 10k
R29 10k
R1 10k
R2 10k
C14 22u
J1 LIN
R4 560
U3:1 NJM2100D
U3:2 NJM2100D
R3 470
C15 1n
R32 470
JP14
AINL-
BIAS
LIN-
R33 4.7k
R35 33
R34 4.7k
C54 0.1u
C53 10u
SW3
DIF0
DIF1
DEM0
DEM1
CMODE
4520
RP1 47k
C18 0.1u
U2
74HC4050
C16 10u
C19 0.1u
C20 1n
R31 470
R6 470
JP3 RIN+
Op-Amp
LINE
R38 10k
R5 10k
R7 10k
C21 22u
J2 RIN
R9 560
U14:1 NJM2100D
U14:2 NJM2100D
R37 10k
R10 4.7k
C22 0.1u
U1
AK4520
C28 0.1u
C30 4.7u
C29 0.1u
C31 10u
JP4
VD
VA
R12 5
R13 5
JP15
AINR-
BIAS
RIN-
R36 33
R11 4.7k
C33 0.1u
C32 10u
C24 0.1u
C25 4.7u
C26 0.1u
C27 4.7u
C34 0.1u
U5
74HC4050
D1 1S1588
R8 10k
74HC14 U4:A
74HC14 U4:B
C23 0.1u
SW1 -PWDA
JP1
Digital Ground
Analog Ground
C35 10u
R15 220
J3 ROUT
R16 27k
C37
D2 1S1588
R14 10k
74HC14 U4:D
74HC14 U4:C
C36 0.1u
SW2 -PWAD
C38 10u
R17 220
J4 LOUT
R18 27k
C39
VOP
L4 10u
C4 47u
C5 0.1u
C17 10u
C55 0.1u
C56 10u
C57 0.1u
Title AKD4520
Size A3
Number AKD4520
Rev B
Date 9/2/'96
Drawn by T. Suzuki
Filename AK4520B.SCH
Sheet 1 of 2



Title	AKD4520		
Size A3	Number Interface		Rev B
Date	9/2/'96	Drawn by	T. Suzuki
Filename	AK4520B.SCH	Sheet	2of 2

■ Input Buffer Circuit

The ADC inputs are Full-differential and internally biased to the ADC voltage pins, VRADR & VRADL with 30k ohms(typ) resistance. The input signal range scales with the supply voltage and nominally 0.3V x (VREFH-VREFL) Vp-p. The signal is input from either positive or negative input and the input signal range scales with the supply voltage and nominally 0.6 x (VREFH-VREFL)Vpp. In case of Single-ended input, the distortion around full scale degrades compared with Full-differential input. The AK4520A can accept input voltages from AGND to VA.
The Input Buffer Circuit on the board is able to input Full-differential and Single-ended of gain 1. External analog signal fed through the BNC connector is terminated by a resistor of 560 ohms. The resistor value should be properly selected in order to meet the output impedance of the signal source. The 'Cin' is an important part in the buffer circuit design.(Example circuit: fc = 150kHz). A large 'Cin' can improve the distortion of the converter because it lowers the effect of feed through noise from the device. However, the larger 'Cin' becomes heavier load for the input buffer amp and increases its distortion. The actual value should be decided by taking a balance between both factors. And please consider the frequency response within audio band.

AK4520A has -110 ~ -115dB Tone Level. Idle Tone Level depends on digital noise coupling from external circuits and this noise can be reduced by application circuit. The Idle Tone Level can be reduced by which method.
First, there is method of dropping digital power supply voltage(VD). This can be reduced digital noise, as a result, Idle Tone Level is buried in noise floor.
Second, approximately -30mV(@VA=5.0V) offset is added at AIN pins of the AK4520A to move tone outside the audio band frequency. In the circuit example(Figure 2.), the bias voltage of Op-amp in the circuit is divided by the resistor as difference between BIAS+ and BIAS-, which is about 17mV at all times. -34mV offset is added at AIN pins of the AK4520A. On the board, bias voltages of left channel and right channel are distributed from differential source. In case of the common source bias voltage, the crosstalk occurs corresponding to the AC impedance of the bias circuit.

Adding offset as aforesaid, "pop" noise is generated by HPF(fc=1Hz, @fs=48kHz) in the AK4520A at reset. The offset of 34mV is -39dBFS against 3.0Vp-p input voltage.
For example, it takes "t = -170.46[ms] x ln(0.089) = 412[ms] (@fs=48kHz, VA=5.0V)" to decrease until -60dBFS (8.9% against -39dBFS).
External mute should consider above.

1. In case of Full-differential inputs (Default)

[JP2, JP3]	: Op-amp
[JP14]	: AINL-
[JP15]	: AINR-
C24,C25,C26,C27	: None
R35, R36	: 33Ù
C15, C20	: 1nF

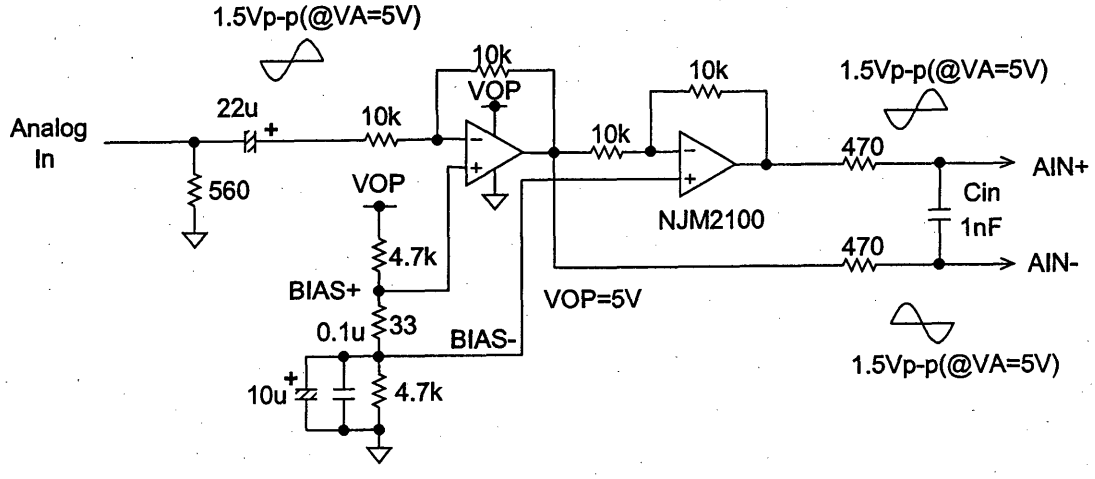


Figure 2.Full-differential Input Buffer Circuit Example

2. In case of Single-ended Input (bias voltage input)

In case of worrying Idle Tone Level, adds offset from external and moves it outside the audio band frequency.

Two inverted op-amps are connected on the evaluation board, however, do not need 2nd op-amp. In this case, if inverted op-amp is input to AIN- pin, can be corresponded with polarity.

[JP2, JP3]	: Op-amp
[JP14, JP15]	: BIAS
C24,C25,C26,C27	: None
R35, R36	: 68Ù
C15, C20	: 1nF

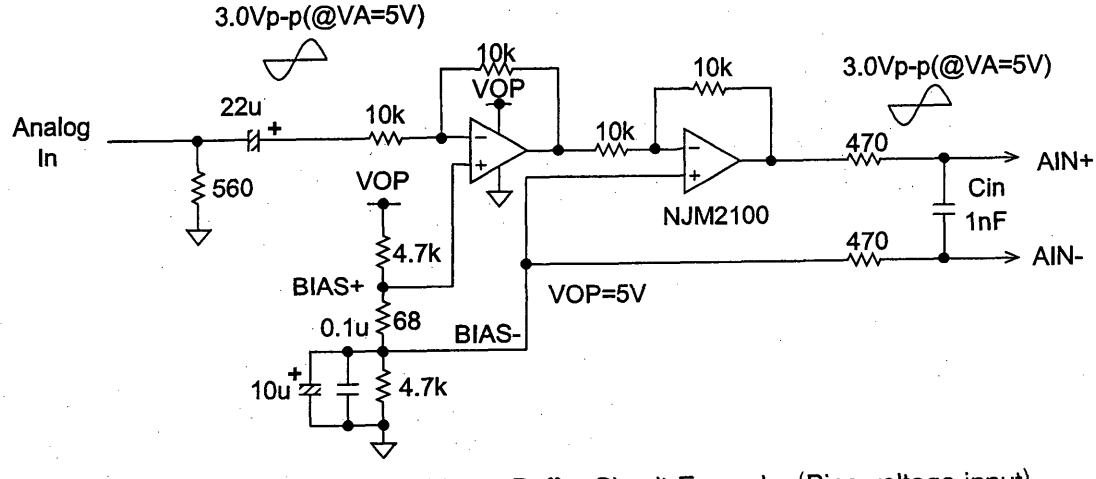


Figure 3. Single-ended Input Buffer Circuit Example (Bias voltage input)

3. In case of Single-ended Input (no input bias)

Analog signal is directly input from BNC connector and this case can reduce the part of input buffer circuit. In case of comparing Full-differential Input circuit(Figure 2.) or Single-ended Input circuit(Figure 3.) with no input buffer circuit shown in Figure 4., as "pop" noise is large at reset, external mute should be taken enough time.

[JP2, JP3]	: LINE: Analog signal is input via BNC connector directly. In this case, U3 and U14 of Op-amp should be taken off.
[JP14, JP15]	: Open
C24, C26	: 0.1uF
C25, C27	: 4.7uF
C15, C20	: 2.2nF
R31, R32	: none

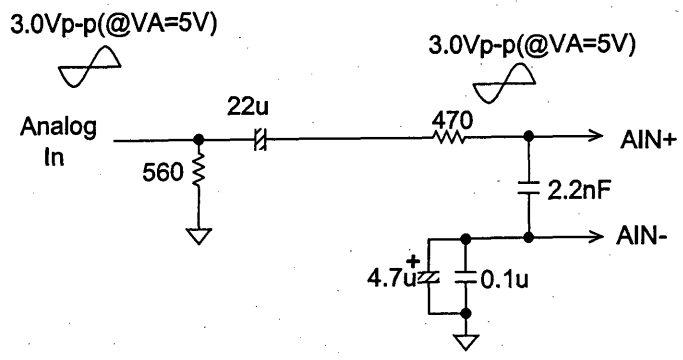


Figure 4. Single-ended Input Buffer Circuit Example (no input buffer)

※ AKM assumes no responsibility for the trouble when using the above circuit examples.

■ Analog Output

The analog outputs are also single-ended and centered the VCOM voltage. The input signal range scales with the supply voltage and nominally 0.6 x VA Vp-p. The DAC includes a combination of switched-capacitor filter(SCF) and continuous-time filter(CTF), so any external filters are not required. However, the DAC has DC offset about a few mV, it is usually eliminated by the capacitor. And the output level of DAC is about 3.1Vp-p at VREF=5V.

■ Grounding and Power Supply Decoupling

The AK4520A requires careful attenuation to power and grounding arrangements. VD should be supplied from analog power supply. AGND and DGND of the AK4520A should be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board.

Decoupling capacitors should be as near to the AK4520A as possible, with the small value ceramic capacitor being the nearest.

■ Operation sequence

① Set up the power supply lines.
VA+=VP+=VD+=2.7 ~ 3.6V or 4.5 ~ 5.5V, AGND=DGND=0V
Each supply line should be distributed from the power unit.
The only CS8402 and CS8412 on the board needs VD+≧ 3.2V.
When changing the voltages of VP+ and VD+, JP13 should be open.

② Set up the evaluation modes and jumper pins. (See the next item)
There are many jumper pins to cover many evaluation mode.
Please take care of setting.

③ Set up the DIP switch. (See the next item)
Set up the DIT. This does not affect AK4520A operation.

④ Power on.
The AK4520A are placed in the power-down mode by turning each power down pin, -PWAD(SW1) -PWDA(SW2) "off" independently.

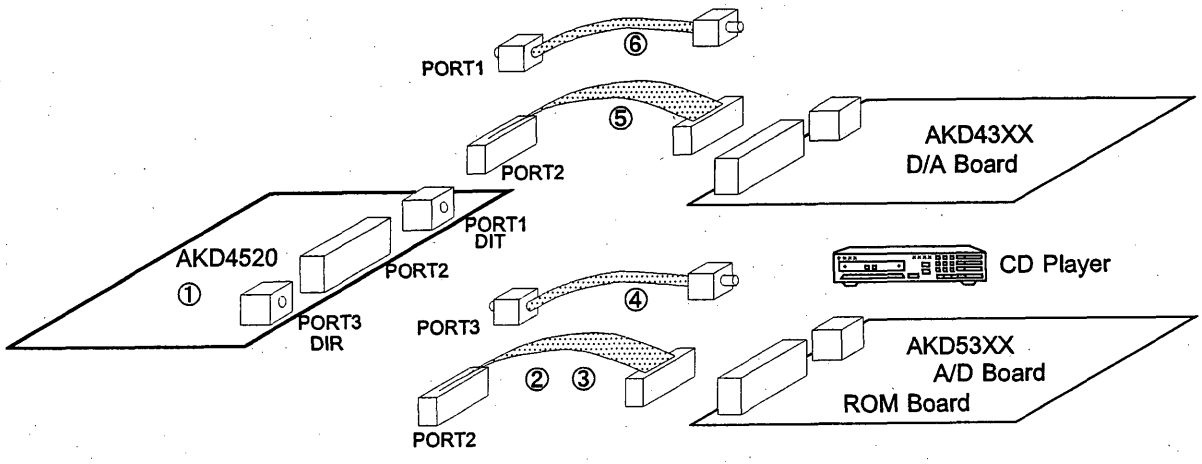
⑤ The AK4520A can be reset by SW1 and SW2 during operation.
"off" resets the device, "on" is for normal operation.

■ The evaluation modes and corresponding jumper pin setting.

1.Evaluation mode

Applicable Evaluation Mode

① Loopback mode (Default)
② Using A/D converted data from ideal sine wave generated by ROM data.
③ Using A/D converted data
④ DIR(Optical Link)
⑤ Using D/A converted data
⑥ DIT(Optical Link)
⑦ All interface signals including master clock are fed externally.



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ring cables corresponded some evaluation modes

① Loopback mode (Default)

Don't connect PORT2 and PORT3. In case of using external clock through a BNC connector,selects EXT on JP11(MCLK) and shorts JP12(XTE).
When SCLK is 64fs, Audio Serial Interface Format is not corresponded to Mode 0 and Mode1.
Mode 1 → ADC:16bit, MSB justified, DAC: 16bit, LSB justified.
Mode 2 → ADC:20bit, MSB justified, DAC: 20bit LSB justified.

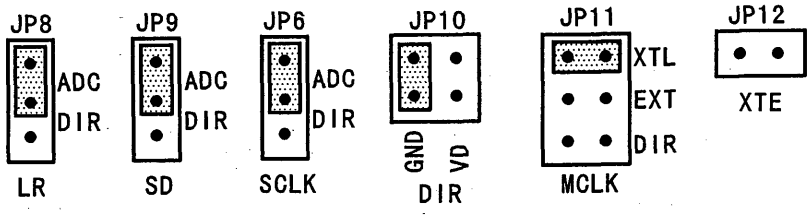


Figure 6. Jumper set up (Loopback mode)

② Using A/D converted data from ideal sine wave generated by ROM data

Digital signals generated by AKD43XX are used. PORT2 is used for the interface with AKD43XX. Master clock is sent from AKD4520A to AKD43XX and LRCK, SCLK, SDTO are done from AKD43XX to AKD4520A. In case of using external clock through a BNC connector, selects EXT on JP11(MCLK) ,shorts JP12(XTE) and opens JP7(SDO). Audio Serial Interface Format is not corresponded Mode 1.

Mode 1 → DAC: 20bit, LSB justified

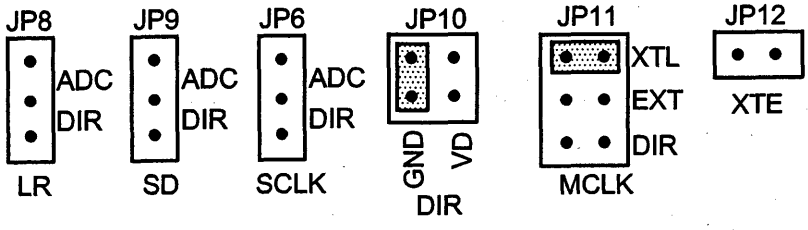


Figure 7. Jumper Set up (ROM)

③ Using A/D converted data

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's A/D evaluation boards (AKD5391, AKD5390, AKD5350 and AKD5352/1) with PORT2. In case of using external clock through a BNC connector, selects EXT JP11(MCLK) and shorts JP12(XTE). Then JP7(SDO) should be open.

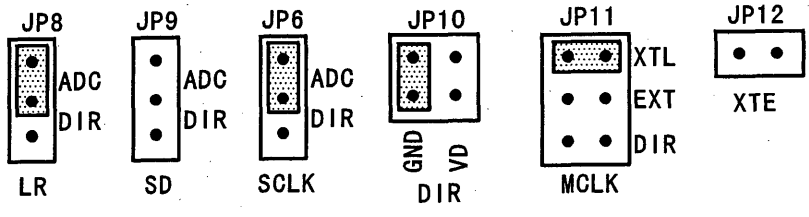


Figure 8. Jumper Set up (A/D)

④ DIR (Optical Link)

PORT3 is used. DIR generates MCLK, SCLK and LRCK from the received data through optical connector(TORX174). Used for the evaluation using CD test disk. Nothing should be connected to PORT1 and PORT2. CS8412(DIR) needs the operating voltage of VD+≧ 3.2V. Audio Serial Interface Format is not corresponded to Mode 1.

Mode → DAC: 20bit, LSB justified

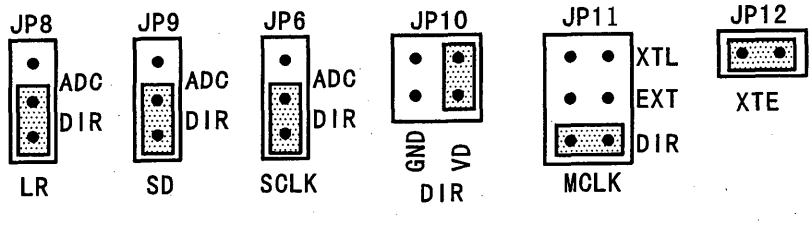


Figure 9. Jumper Set up (DIR)

⑤ Using D/A converted data

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's D/A evaluation boards (AKD4328, AKD4319, AKD4320 and AKD4321) with PORT2. Then JP7(SDO) should be open.

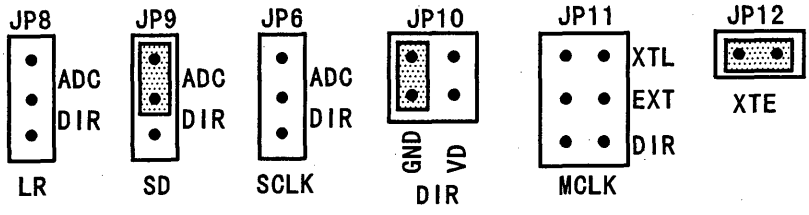


Figure 10. Jumper Set up (D/A)

⑥ DIT (Optical Link)

PORT1 is used. DIT generated SDATA from received data and which is output through optical connector(TOTX174). It is possible to connect AKM's evaluation boards (AKD4321, AKD4320, AKD4319 and AKD4328), digital-amplifier and etc. Nothing should be connected to PORT2 and PORT3. This set-up is the same ① as it. CS8402(DIT) needs the operating voltage of VD+≧ 3.2V .SW1 is kept the "off" during normal operation.

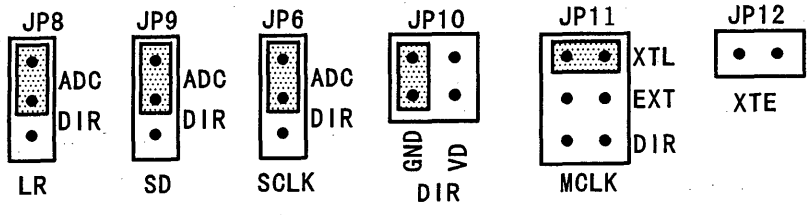


Figure 11. Jumper Set up (DIT)

⑦ All interfacing signals including master clock are fed externally.

Under the following set-up, all external signals needed for the AK4520A to operate could be fed through PORT2. In case of interfacing external sources to D/A converter, JP9(SD) should be open. And in case of using A/D data to externally, JP9(SD) is set ADC position. When JP9(SD) is open, the A/D data can be output from the DIF0 pin of PORT2 at the same time if JP12(XTE) is shortened.

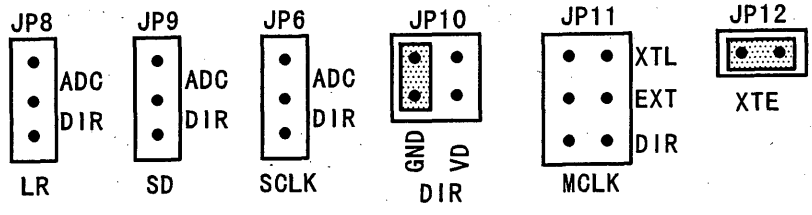
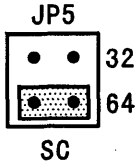


Figure 12. Jumper Set up (EXT)

2. BIT CLK (SC) set up



[JP5] The bit clock(SCLK) sets up
32: 32fs, 64: 64fs
Figure shows 64fs example.

3. Jumper-set up and explanation

[JP13] Shorts VD+ and VP+.
In case of separating VD+ and VP+ supplies, JP13 should be open.

■ The function of the toggle SW.

[SW1] Resets a part of the A/D. Keep "on" during normal operation.
[SW2] Resets a part of the D/A. Keep "on" during normal operation.
[SW5] Resets the CS8402."off" resets the internal counter of CS8402, then Bi-phase signal is not output. Keep "on" during normal operation.

■ The indication content for LED.

[D4] Monitors VERF pin of the CS8412. LED turns on when some error has occurred to CS8412.
[D5] Indicates whether the input data is pre-emphasized or not. LED turns on when the data is pre-emphasized.

■ DIP switch set up

1.SW3: This switch sets up the operation mode of the AK4520A.
Confirm the set up of the DIP-SW before evaluation starts. ON means "H" and OFF,"L".

No.	PIN	ON	OFF
1	DIF0	See the Table 3.	
2	DIF1	Serial Data Modes	
3	DEM0	See the Table 1.	
4	DEM1	De-emphasis Frequency	
5	CMODE	384fs	256fs

Table 2. DIP SW set-up the AK4520A

DEM1	DEM0	Frequency
OFF	OFF	0: 44.1kHz
OFF	ON	1: OFF
ON	OFF	2: 48kHz
ON	ON	3: 32kHz

Table 1. De-emphasis Frequency

DIF1	DIF0	MODE	SDTO (ADC)	SDTI (DAC)	L/R	SCLK
OFF	OFF	0	16bit, MSB justified	16bit, LSB justified	H/L	≧ 32fs
OFF	ON	1	20bit, MSB justified	20bit, LSB justified	H/L	≧ 32fs
ON	OFF	2	20bit, MSB justified	20bit, MSB justified	H/L	≧ 40fs
ON	ON	3	IIS (I2S)	IIS (I2S)	L/H	32fs or ≧ 40fs

Table 3. Serial Data Modes

2. SW4: This switch sets the C-bit of CS8402. (Default is the consumer mode)

This set up does not affect the evaluation of the AK4520A. In case of using DIT, need to set it up correctly. For more detailed configurations, please refer to the CS8402 data-sheet.

Switch	OFF=0,ON=1	Contents
1	$\overline{PRO}$=0	Professional mode, C0=1
2,3	$\overline{C6}$,$\overline{C7}$	C6,C7 - Sampling frequency
	1 1	00 - Not indicated. Receiver default to 48kHz.
	1 0	01 - 48kHz
	0 1	10 - 44.1kHz
	0 0	11 - 32kHz
4	$\overline{C9}$	C8,C9,C10,C11 - 1bit of channel mode
	1	0000 - Mode not indicated. Receiver default to 2-channel mode.
	0	0100 - Stereophonic.
5	$\overline{C1}$	C1 - Audio mode
	1	0 - Normal audio
	0	1 - Not audio
6	TRNPT	Transparent mode *CS8402 is CRE
	0	Normal mode
	1	Transparent mode
8,7	EM1,EM0	C2,C3,C4 - Encoded audio signal emphasis
	1 1	000 - Emphasis not indicated. Receiver defaults to no emphasis with manual override enable.
	1 0	100 - None
	0 1	110 - 50/15usec
	0 0	111 - CCITT J.17

Table 4. DIP switch set up of CS8402

Switch	OFF=0,ON=1	Contents
1	$\overline{PRO}$=1	Consumer mode, C0=0 (Default)
2	$\overline{C2}$	C2 - Copy
	1	0 - Copy inhibited
Default	0	1 - Copy permitted
3	$\overline{C3}$	C3,C4,C5 - Pre-emphasis
Default	1	000 - None
	0	100 - 50/15usec
4	$\overline{C15}$	C15 - Generation Status
	1	0 - See the standard
Default	0	1 - See the standard
6,5	FC1,FC0	C24,C25,C26,C27- Sampling frequency
	0 0	0000 - 44.1kHz
Default	0 1	0100 - 48kHz
	1 0	1100 - 32kHz
	1 1	0000 - 44.1kHz, CD mode
8,7	$\overline{C8}$,$\overline{C9}$	C8-C14 - Category code
Default	1 1	0000000 - General
	1 0	0100000 - PCM encoder/decoder
	0 1	1000000 - CD
	0 0	1100000 - DAT

Table 5. DIP switch set up of CS8402 (Consumer mode)

AK4520A Measurement Results

■ No.1 (RHODE & SCHWARZ, UPD04)

[Measurement condition]

- Measurement unit : ROHDE & SCHWARZ, UPD04
- MCLK : 256fs
- BICK : 64fs
- Bit : 20bit
- fs : 44.1kHz
- Power Supply : VA=VD=3V & 5V
- Interface : DIT/DIR
- Room temp.

1. A/D Output (Full-differential inputs, refer to Figure 2.)

Parameter	Input signal	Measurement Filter	Results	
			VA=VD=5V	VA=VD=3V
S/ (N+D)	1kHz,-0.5dB	20kLPF	91.6dB	88.7dB
Dynamic Range	1kHz,-20dB	20kLPF	96.5dB	93.0dB
		20kLPF,A-weight	100.5dB	96.7dB
Dynamic Range	1kHz,-60dB	20kLPF	96.7dB	93.1dB
		20kLPF,A-weight	100.4dB	96.5dB
S/N	1kHz,0dB/GND IN	20kLPF	96.2dB	92.6dB
		20kLPF,A-weight	100.5dB	96.7dB
		CCIR-ARM	96.2dB	92.3dB

2. A/D Output (Single-ended inputs, refer to Figure 3. or Figure 4.)

Parameter	Input signal	Measurement Filter	Results	
			VA=VD=5V	VA=VD=3V
S/ (N+D)	1kHz,-0.5dB	20kLPF	83.2dB	84.9dB
Dynamic Range	1kHz,-20dB	20kLPF	dB	94.3dB
		20kLPF,A-weight	dB	97.7dB
Dynamic Range	1kHz,-60dB	20kLPF	dB	94.5dB
		20kLPF,A-weight	dB	98.0dB
S/N	1kHz,0dB/GND IN	20kLPF	dB	94.1dB
		20kLPF,A-weight	dB	97.8dB
		CCIR-ARM	96.6dB	93.6dB

3. D/A Output

Parameter	Input signal	Measurement Filter	Results	
			VA=VD=5V	VA=VD=3V
S/ (N+D)	1kHz,0dB	20kLPF	90.6dB	92.0dB
Dynamic Range	1kHz,-20dB	20kLPF	97.1dB	93.0dB
		20kLPF,A-weight	100.5dB	96.4dB
Dynamic Range	1kHz,-60dB	20kLPF	97.3dB	93.0dB
		20kLPF,A-weight	100.3dB	96.1dB
S/N	1kHz,0dB/"0" IN	20kLPF	95.5dB	92.3dB
		20kLPF,A-weight	100.2dB	96.0dB
		CCIR-ARM	96.4dB	92.0dB

4. A/D → D/A Loopback Output (A/D: Full-differential inputs, refer to Figure 2.)

Parameter	Input signal	Measurement Filter	Results	
			VA=VD=5V	VA=VD=3V
S/ (N+D)	1kHz,-0.5dB	20kLPF	89.1dB	89.5dB
Dynamic Range	1kHz,-20dB	20kLPF	95.7dB	91.0dB
		20kLPF,A-weight	98.7dB	94.5dB
Dynamic Range	1kHz,-60dB	20kLPF	95.8dB	91.2dB
		20kLPF,A-weight	98.7dB	94.1dB
S/N	1kHz,0dB/GND IN	20kLPF	94.6dB	92.0dB
		20kLPF,A-weight	98.0dB	96.0dB
		CCIR-ARM	94.8dB	90.3dB

■ No.2 (Audio Precision, System One)

[Measurement condition]

- Measurement unit : Audio Precision, System One (RMS mode)
- MCLK : 256fs
- BICK : 64fs
- Bit : 20bit
- Bandwidth : 22kHz
- fs : 44.1kHz
- Power Supply : VA=VD=3V & 5V
- Interface : DIT/DIR
- Room temp.

1. A/D Output (Full-differential inputs,refer to Figure 2.)

Parameter	Input signal	Measurement Filter	Results	
			VA=VD=5V	VA=VD=3V
S/ (N+D)	1kHz,-0.5dB		91.7dB (90.7dB)	88.0dB
Dynamic Range	1kHz,-20dB		96.7dB (93.7dB)	93.0dB
Dynamic Range	1kHz,-60dB		95.6dB (93.3dB)	93.0dB
S/N	1kHz,0dB/GND IN	A-weight A-weight	100.3dB (97.9dB)	92.8dB

* () shows the performance with 16bit data.

2. A/D Output (Single-ended inputs, refer to Figure 3. or Figure 4.)

Parameter	Input signal	Measurement Filter	Results	
			VA=VD=5V	VA=VD=3V
S/ (N+D)	1kHz,-0.5dB		82.5dB	83.6dB
Dynamic Range	1kHz,-20dB		96.4dB	93.4dB
Dynamic Range	1kHz,-60dB		96.4dB	93.5dB
S/N	1kHz,0dB/GND IN		96.3dB	93.6dB
		A-weight	100.5dB	98.1dB

3. D/A Output

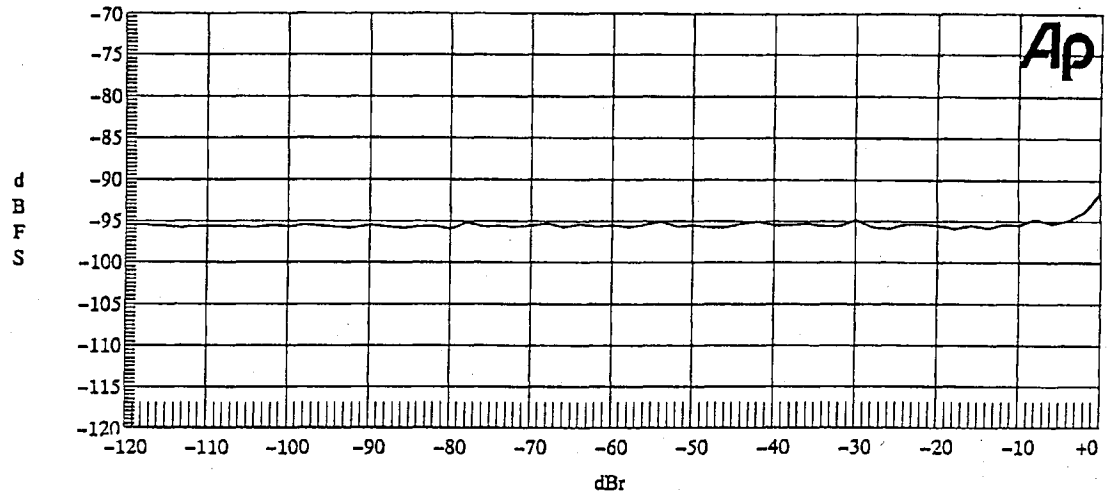
Parameter	Input signal	Measurement Filter	Results			
			VA=VD=5V			VA=VD=3V
			32kHz	44.1kHz	48kHz	44.1kHz
S/(N+D)	1kHz,0dB	20kLPF	91.2dB	90.8dB (89.0dB)	90.4dB	89.0dB
		22kHz	65.5dB	90.3dB	90.3dB	88.3dB
		30kHz	57.4dB	82.2dB	86.0dB	81.7dB
		A-Weight	69.1dB	88.8dB	89.9dB	88.7dB
		22kLPF, A-weight	81.1dB	91.3dB	91.0dB	91.4dB
Dynamic Range	1kHz,-20dB	20kLPF	93.0dB	93.8dB	93.4dB	89.5dB
		22kLPF	84.8dB	93.5dB	93.3dB	89.3dB
		30kLPF	76.8dB	90.9dB	91.4dB	87.5dB
		A-weight	87.4dB	95.3dB	95.3dB	91.9dB
		22kLPF, A-weight	95.1dB	96.4dB (93.2dB)	96.1dB	92.5dB
S/N	1kHz, 0dB/"0"data IN	20kLPF	92.5dB	94.0dB	93.6dB	89.5dB
		22kLPF	91.8dB	93.6dB	93.3dB	89.4dB
		30kLPF	86.1dB	91.5dB	91.6dB	87.8dB
		A-weight	91.5dB	95.6dB	95.4dB	92.0dB
		22kLPF, A-weight	95.0dB	96.7dB	96.0dB	92.5dB

4. A/D → D/A Loopback Output (A/D: Full-differential inputs, refer to Figure 2.)

Parameter	Input signal	Measurement Filter	Results	
			VA=VD=5V	VA=VD=3V
S/(N+D)	1kHz,-0.5dB	20kLPF	89.1dB	dB
		22kLPF	88.7dB	dB
		30kLPF	82.2dB	dB
		A-weight	88.8dB	dB
		22kLPF, A-weight	90.3dB	dB
Dynamic Range	1kHz,-20dB	20kLPF	91.0dB	dB
		22kLPF	91.1dB	dB
		30kLPF	89.6dB	dB
		A-weight	93.3dB	dB
		22kLPF,A-weight	94.0dB	dB
S/N	1kHz,0dB/GND IN	20kLPF	91.0dB	dB
		22kLPF	91.1dB	dB
		30kLPF	89.6dB	dB
		A-weight	93.6dB	dB
		22kLPF,A-weight	94.2dB	dB

AKM

THD+N vs. Input Level

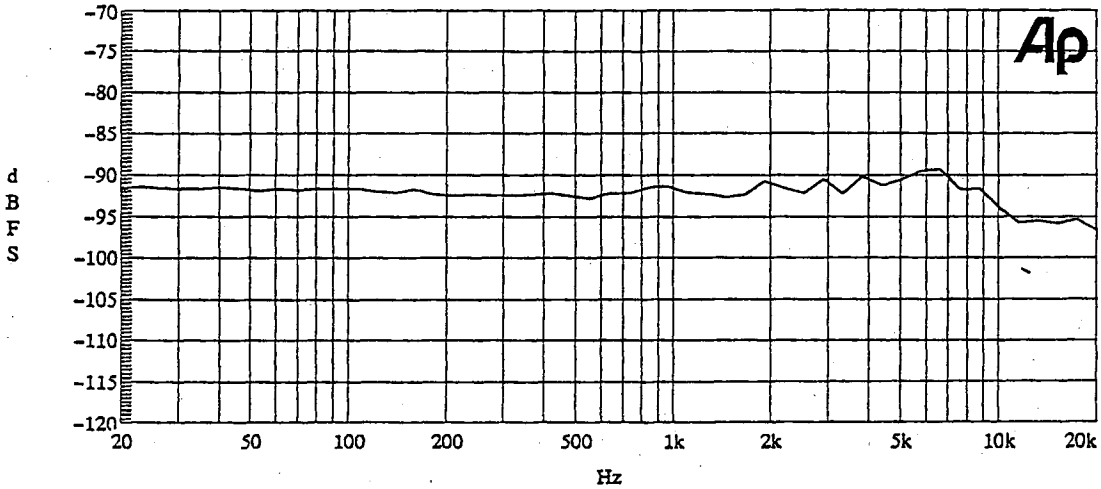


Line Style	Thick	Data	Axis
Solid	3	Genanlr.THD+N Abs.	Left

[Conditions]
Device: AK4520 (ADC)
Measurement Unit: Audio Precision, System One
Power supply: VA=VD=5V
MCLK: 256fs
BICK: 64fs
Interface: DIT
fs: 44.1kHz
Bandwidth: 22kHz
fin: 1kHz
Temperature: Room temperature
Full-Differential Inputs

AKM

THD+N vs. Frequency

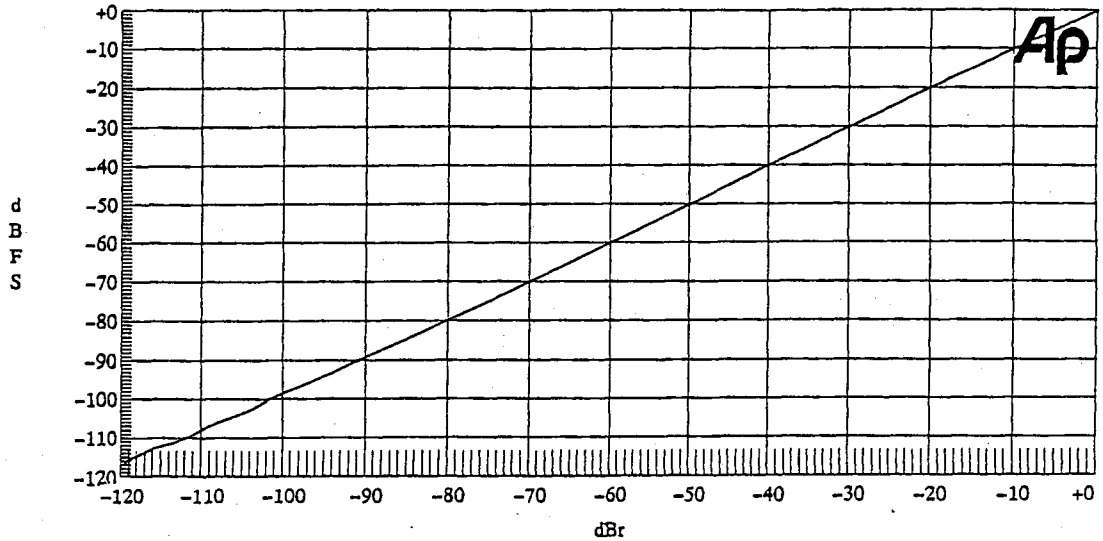


Line Style	Thick	Data	Axis
Solid	3	Genanlr.THD+N Abs.	Left

[Conditions]
Device: AK4520 (ADC)
Measurement Unit: Audio Precision, System One
Power supply: VA=VD=5V
MCLK: 256fs
BICK: 64fs
Interface: DIT
fs: 44.1kHz
Band width: 22kHz
Level: -0.5dBFS
Temperature: Room temperature
Full-Differential Inputs

AKM

Linearity

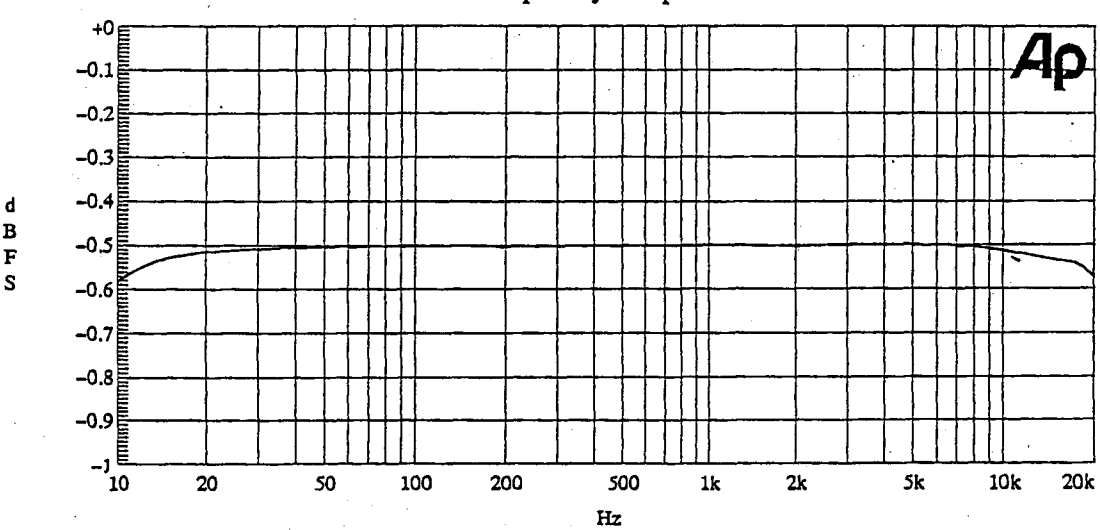


Line Style	Thick	Data	Axis
Solid	3	Genanlr.Bandpass	Left

[Conditions]
Device: AK4520 (ADC)
Measurement Unit: Audio Precision, System One
Power supply: VA=VD=5V
MCLK: 256fs
BICK: 64fs
Interface: DIT
fs: 44.1kHz
fin: 1kHz
Temperature: Room temperature
Full-Differential Inputs

AKM

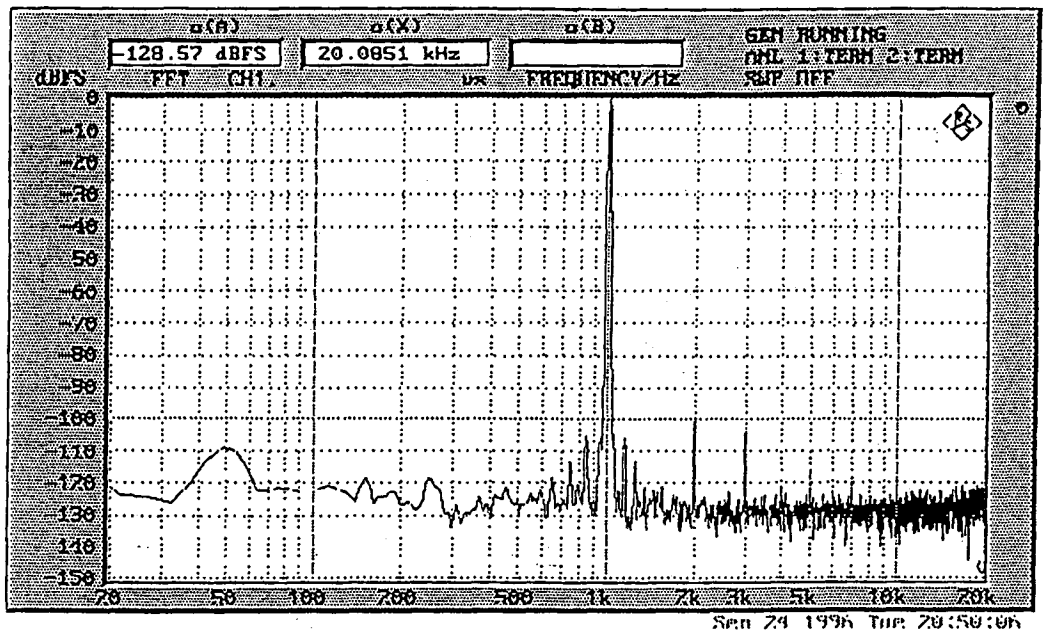
Frequency Response



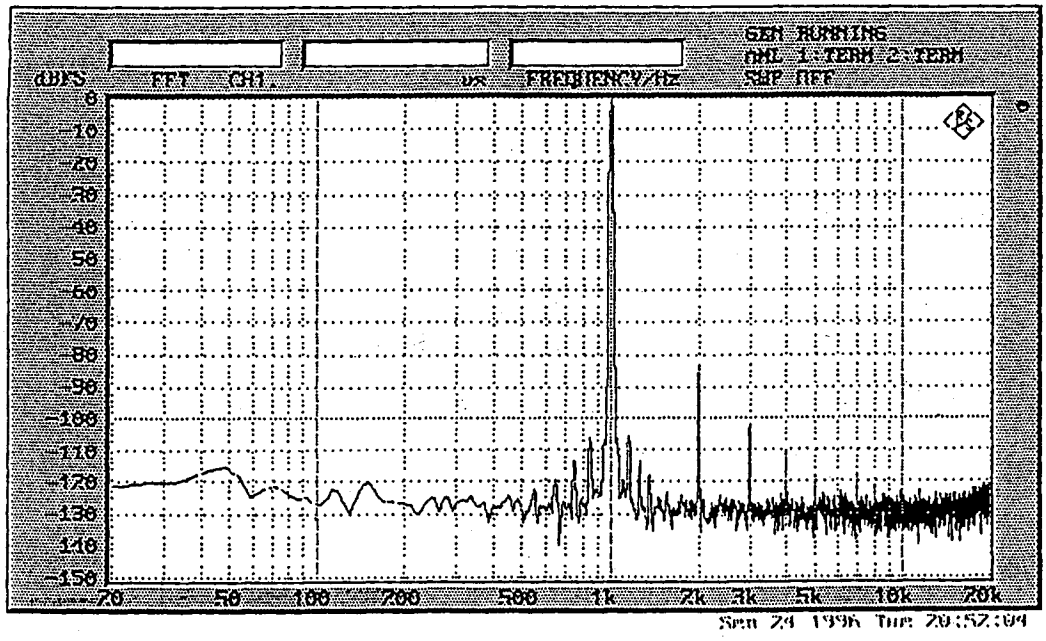
Line Style	Thick	Data	Axis
Solid	3	Genanlr.Level B	Left

[Conditions]
Device: AK4520 (ADC)
Measurement Unit: Audio Precision, System One
Power supply: VA=VD=5V
MCLK: 256fs
BICK: 64fs
Interface: DIT
fs: 44.1kHz
Level: -0.5dBFS@1kHz
Temperature: Room temperature
Full-Differential Inputs

* Total Frequency Response
Evaluation board's HPF: fc=0. 7Hz
AK4520's HPF: fc=0. 9Hz(@fs=44. 1kHz)



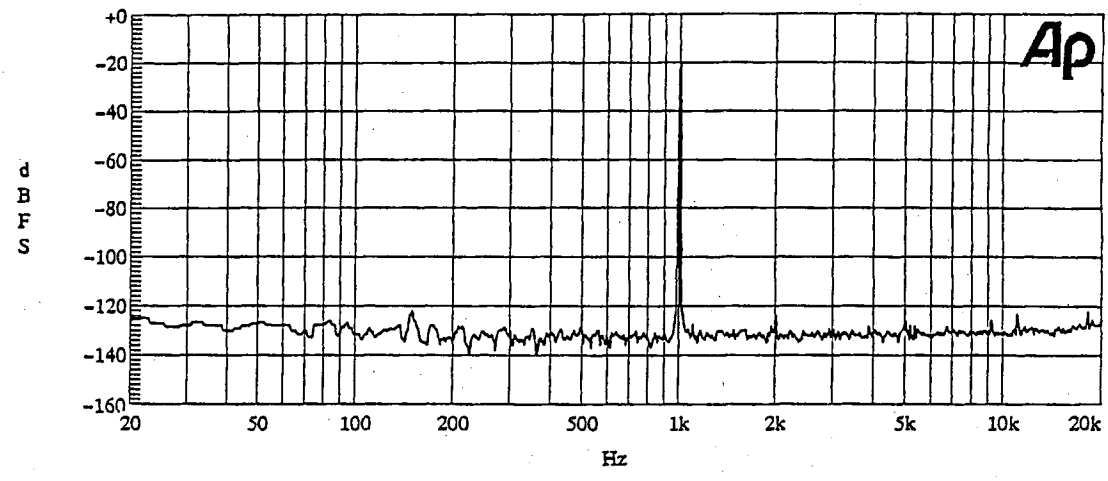
[Conditions]
Device: AK4520 (ADC)
Measurement Unit: ROHDE & SCHWARZ, UPD04
Power Supply: VA=VD=5V
MCLK: 256fs
BICK: 64fs
Interface: DIT
fs: 44. 1kHz
Points: 8192
Averageing: 4
fin: 1kHz@-0. 5dBFS
Temperature: Room temperature
Full-differential inputs



[Conditions]
Device: AK4520 (ADC)
Measurement Unit: ROHDE & SCHWARZ, UPD04
Power Supply: VA=VD=5V
MCLK: 256fs
BICK: 64fs
Interface: DIT
fs: 44. 1kHz
Points: 8192
Averageing: 4
fin: 1kHz@-0. 5dBFS
Temperature: Room temperature
Single-ended inputs

AKM

FFT plot

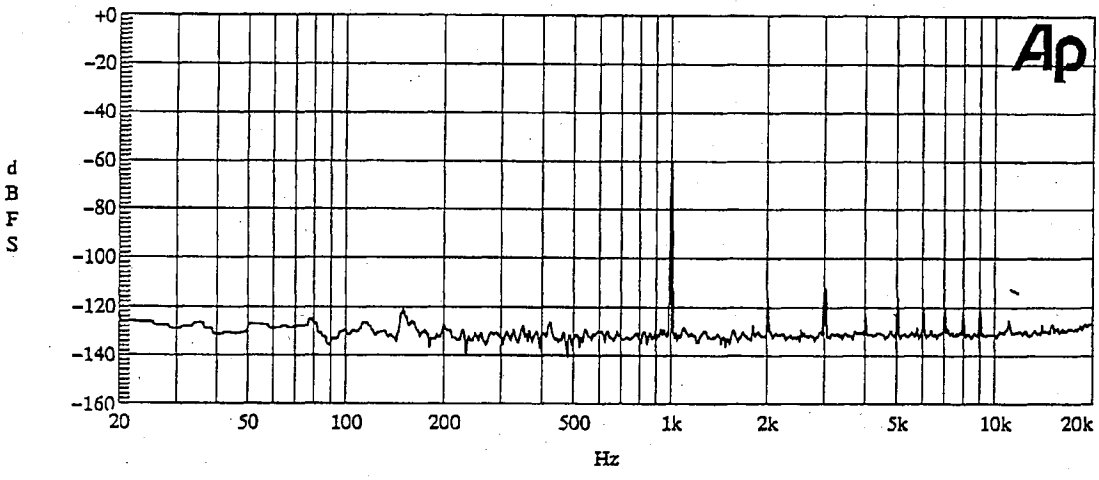


Line Style	Thick	Data	Axis
Solid	3	Fftgen.Ch.1 Ampl	Left

[Conditions]
Device: AK4520 (ADC)
Measurement Unit: Audio Precision, System One
Power supply: VA=VD=5V
MCLK: 256fs
BICK: 64fs
Interface: DIT
fs: 44.1kHz
Points: 8192
Averaging: 4
fin: 1kHz@-20dBFS
Temperature: Room temperature
Full-Differential Inputs

AKM

FFT plot

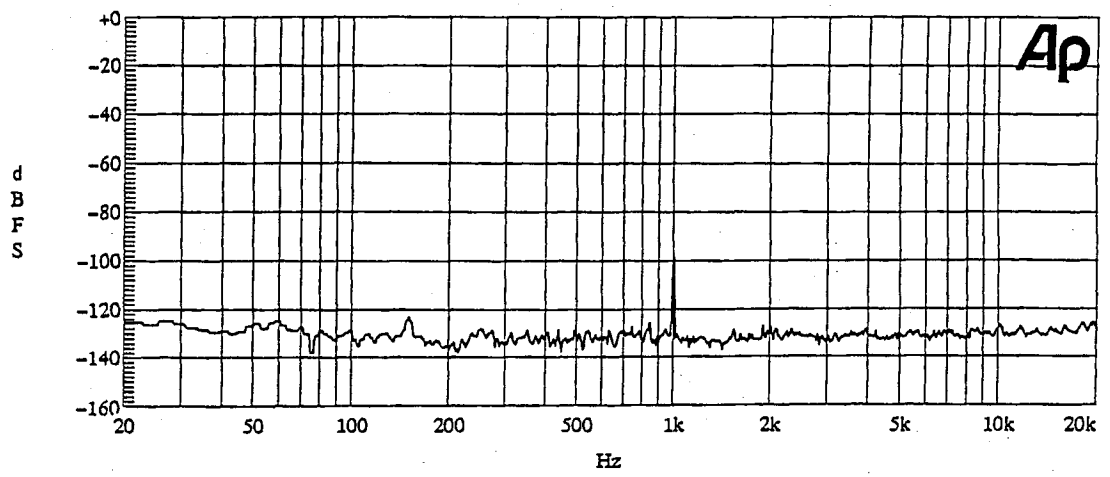


Line Style	Thick	Data	Axis
Solid	3	Fftgen.Ch.1 Ampl	Left

[Conditions]
Device: AK4520 (ADC)
Measurement Unit: Audio Precision, System One
Power supply: VA=VD=5V
MCLK: 256fs
BICK: 64fs
Interface: DIT
fs: 44.1kHz
Points: 8192
Averaging: 4
fin: 1kHz@-60dBFS
Temperature: Room temperature
Full-Differential Inputs

AKM

FFT plot

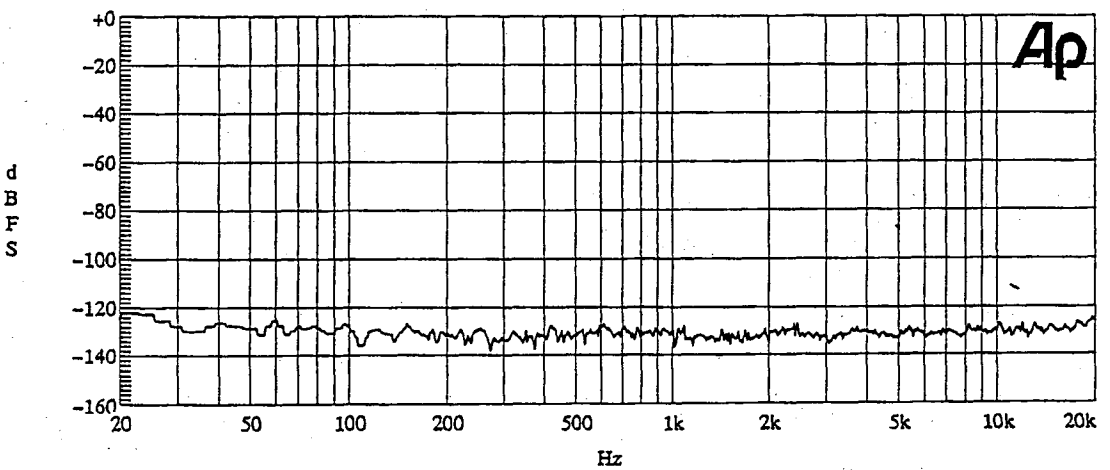


Line Style	Thick	Data	Axis
Solid	3	Fftgen.Ch.1 Ampl	Left

[Conditions]
Device: AK4520 (ADC)
Measurement Unit: Audio Precision, System One
Power supply: VA=VD=5V
MCLK: 256fs
BICK: 64fs
Interface: DIT
fs: 44.1kHz
Points: 8192
Averaging: 4
fin: 1kHz@-100dBFS
Temperature: Room temperature
Full-Differential Inputs

AKM

FFT plot



Line Style	Thick	Data	Axis
Solid	3	Fftgen.Ch.1 Ampl	Left

[Conditions]
Device: AK4520 (ADC)
Measurement Unit: Audio Precision, System One
Power supply: VA=VD=5V
MCLK: 256fs
BICK: 64fs
Interface: DIT
fs: 44.1kHz
Points: 8192
Averaging: 4
Noise floor
Temperature: Room temperature
Full-Differential Inputs

AK4520A DAC part

Conditions :

AVDD = DVDD = 5.0V or 3.0V,
fs = 44.1kHz, MCLK = 256fs, BICK = 64fs,
Measurement unit = ROHDE & SCHWARZ UPD04
Interface = DIR

Contents :

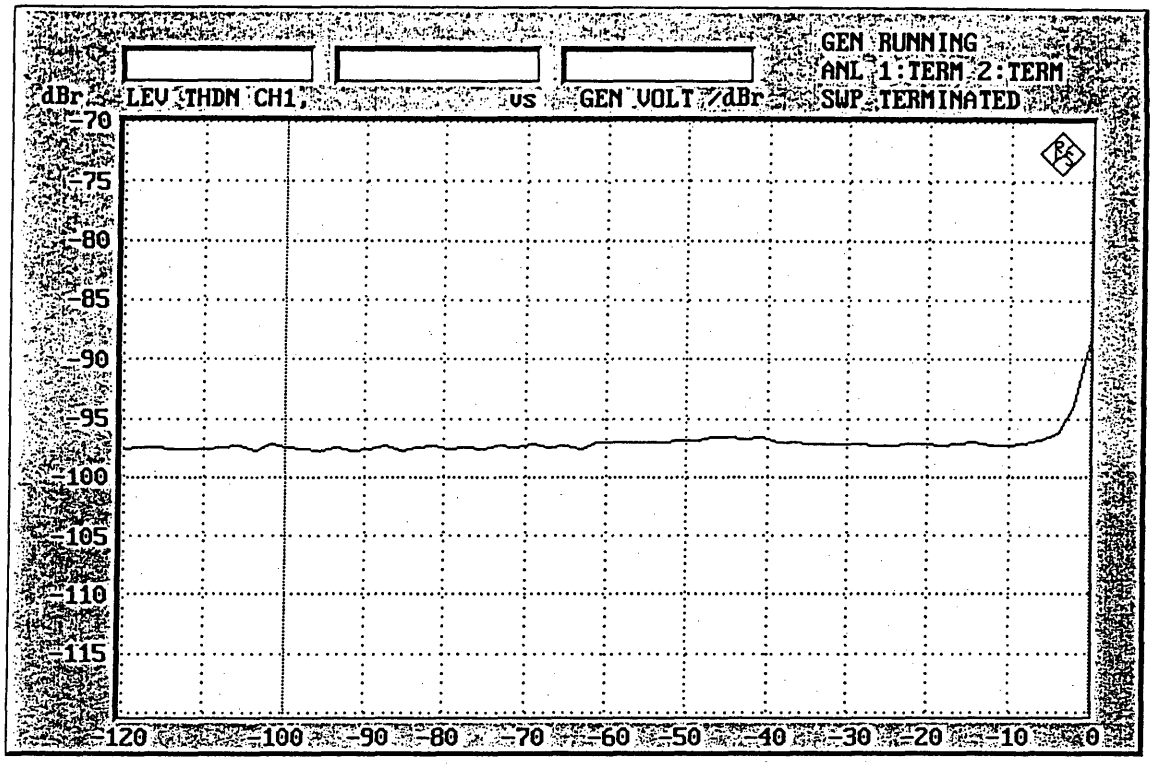


Fig.1 : THD+N vs. Input level (fin: 1kHz)

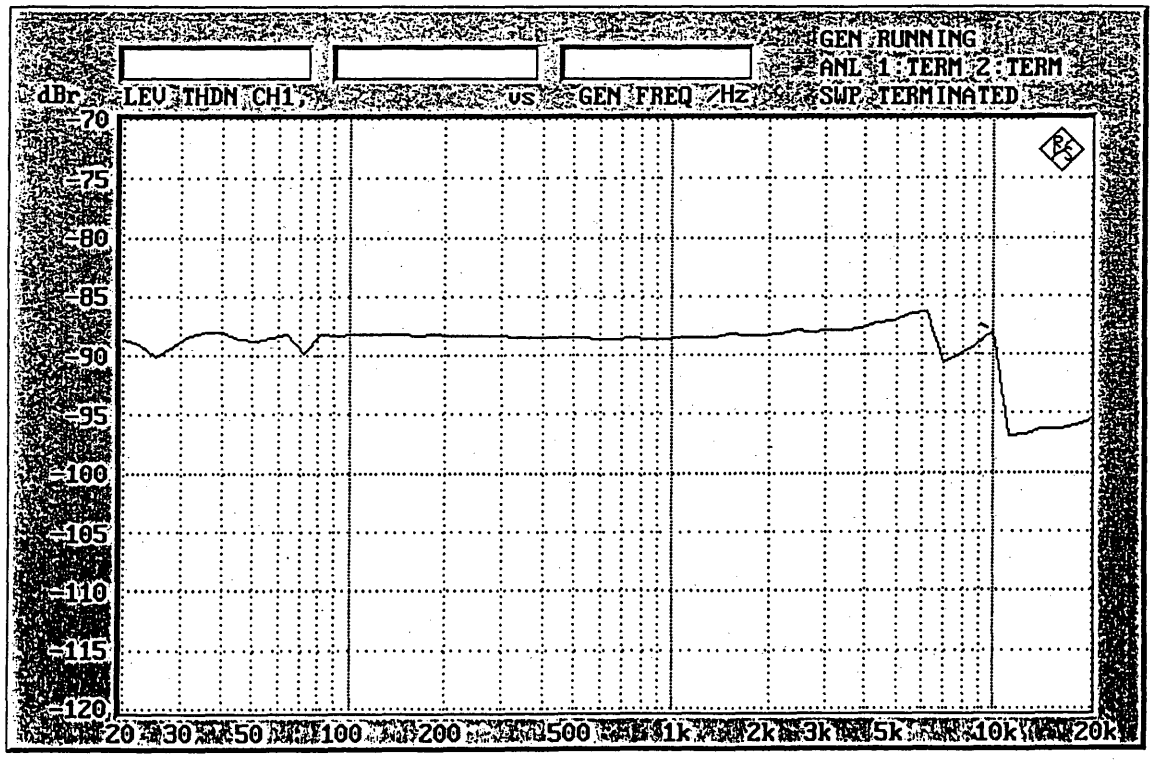


Fig.2 : THD+N vs. Input frequency (input level: 0dBFS)

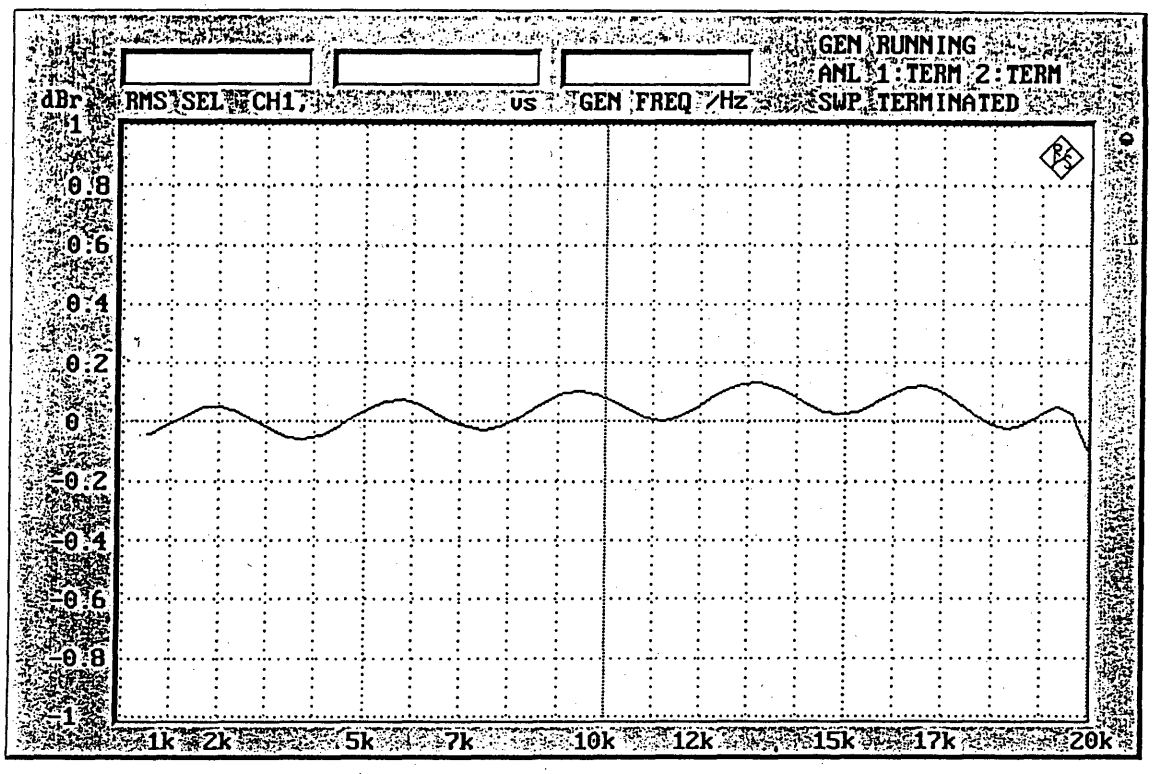


Fig.3 : Frequency response (level: 0dBr @1kHz)

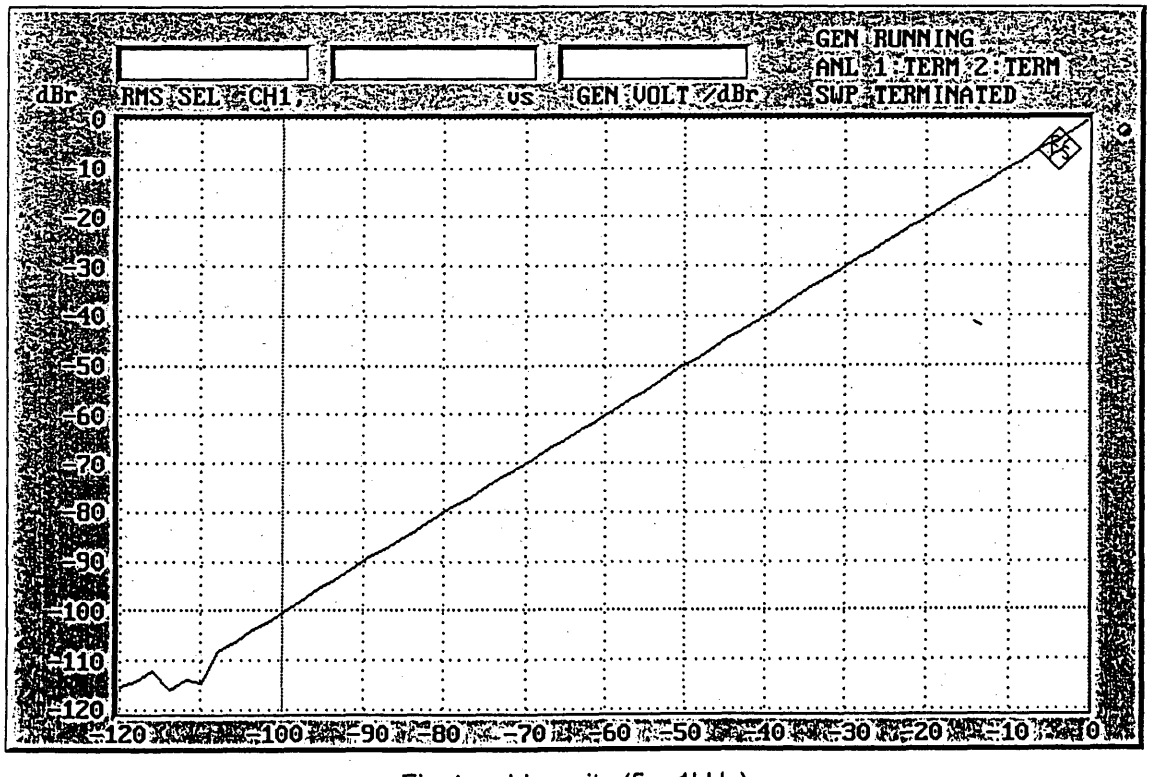


Fig.4 : Linearity (fin: 1kHz)

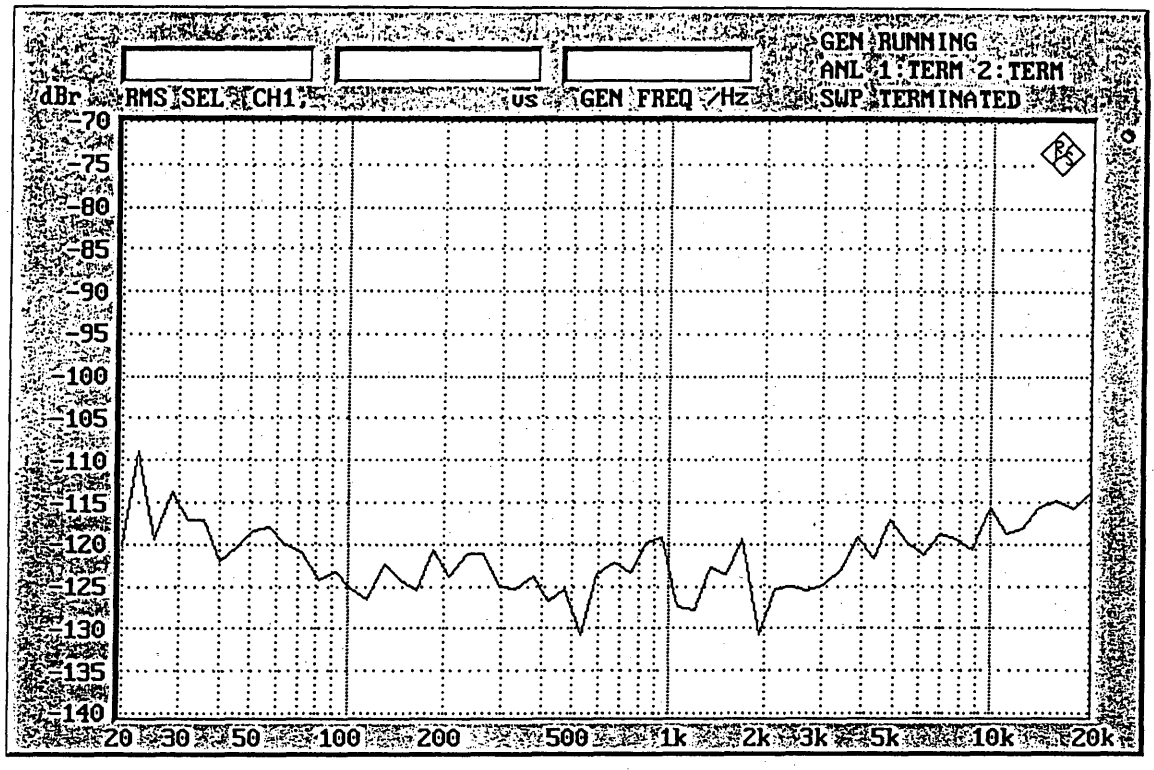


Fig.5 : Cross talk

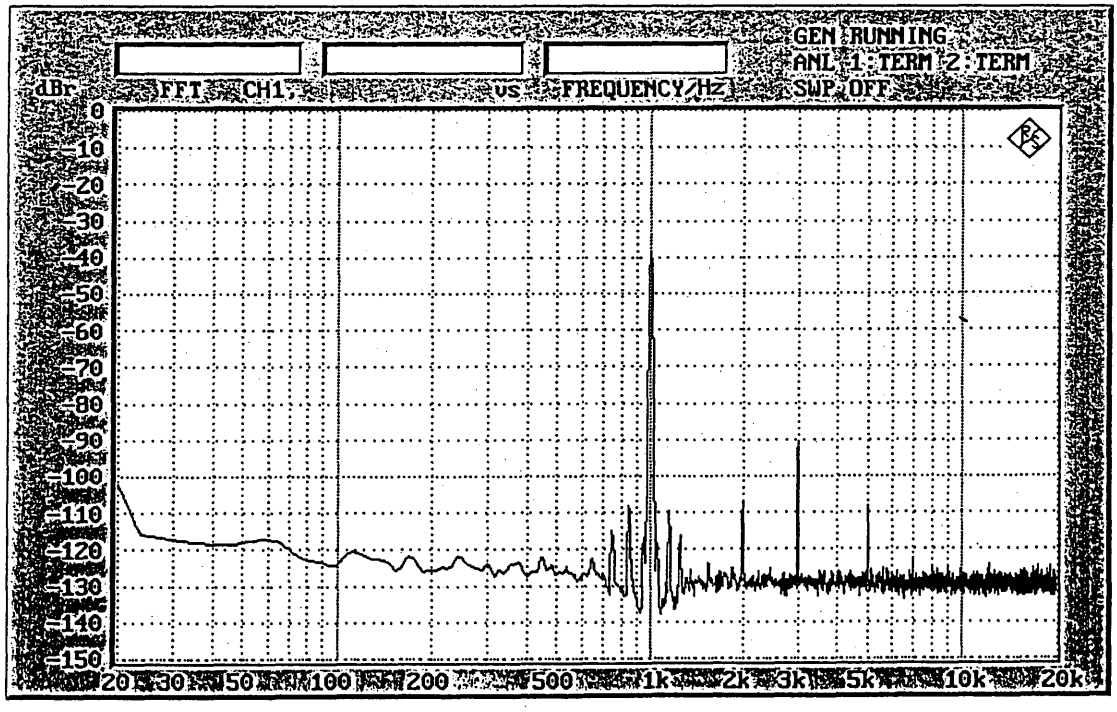


Fig.6 : FFT (input signal: 1kHz,0dBFS, FFT points: 8192, averaging: 16, 30dB Notch filter: on)

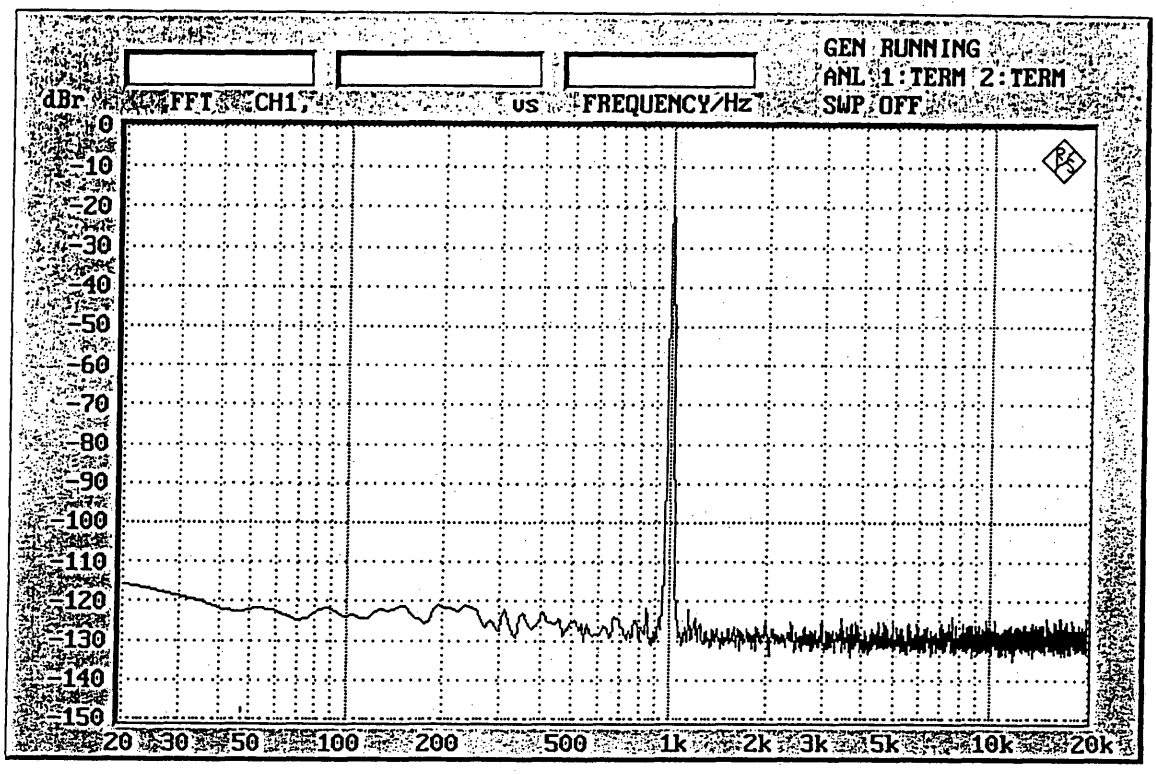


Fig.7 : FFT (input signal: 1kHz,-20dBFS, FFT points: 8192, averaging: 16)

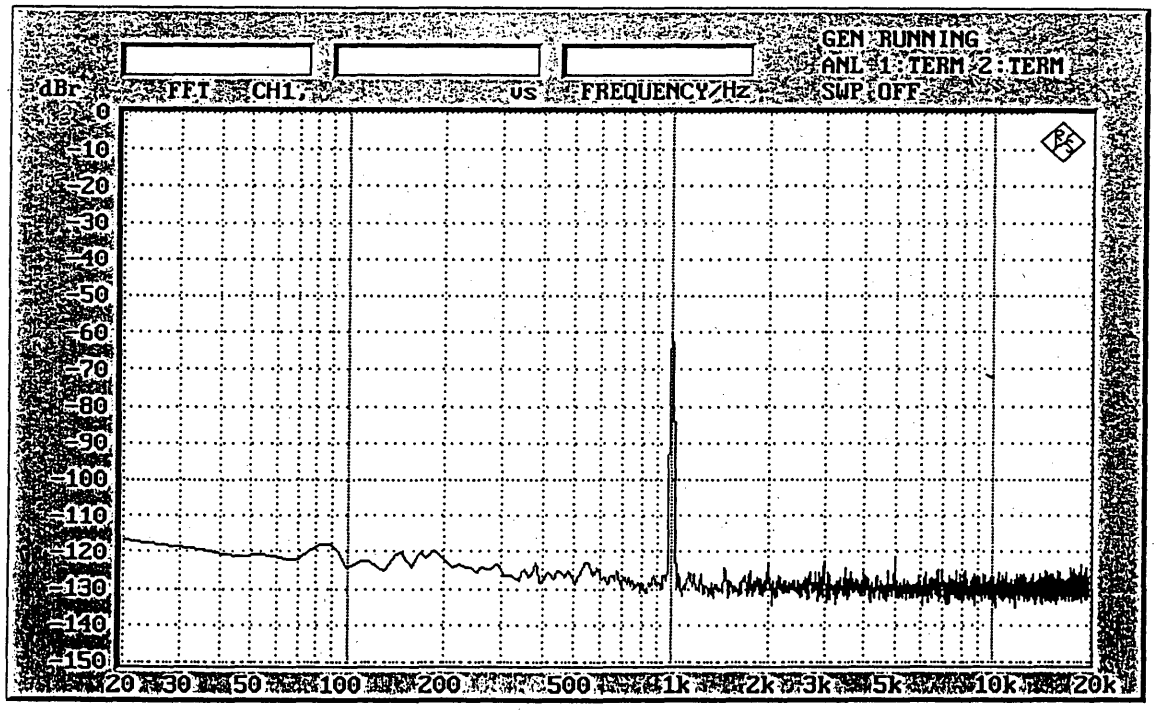


Fig.8 : FFT (input signal: 1kHz,-60dBFS, FFT points: 8192, averaging: 16)

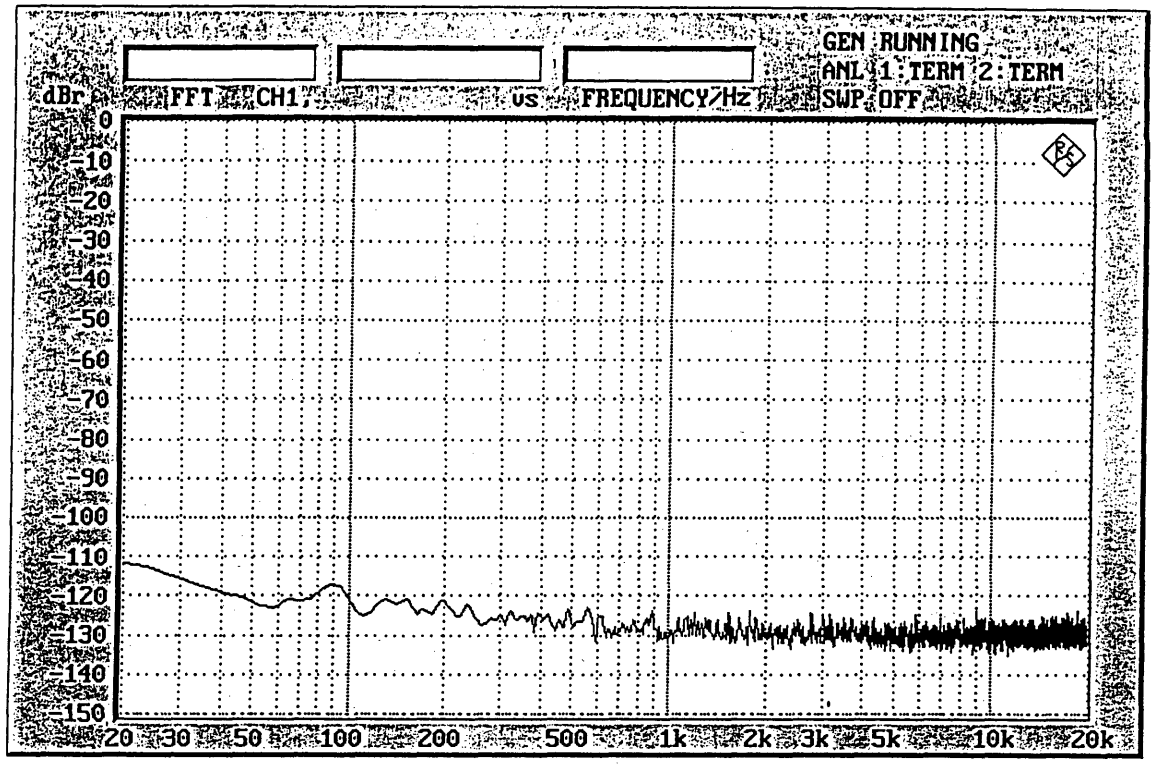


Fig.9 : FFT (noise floor. FFT points: 8192, averaging: 16)

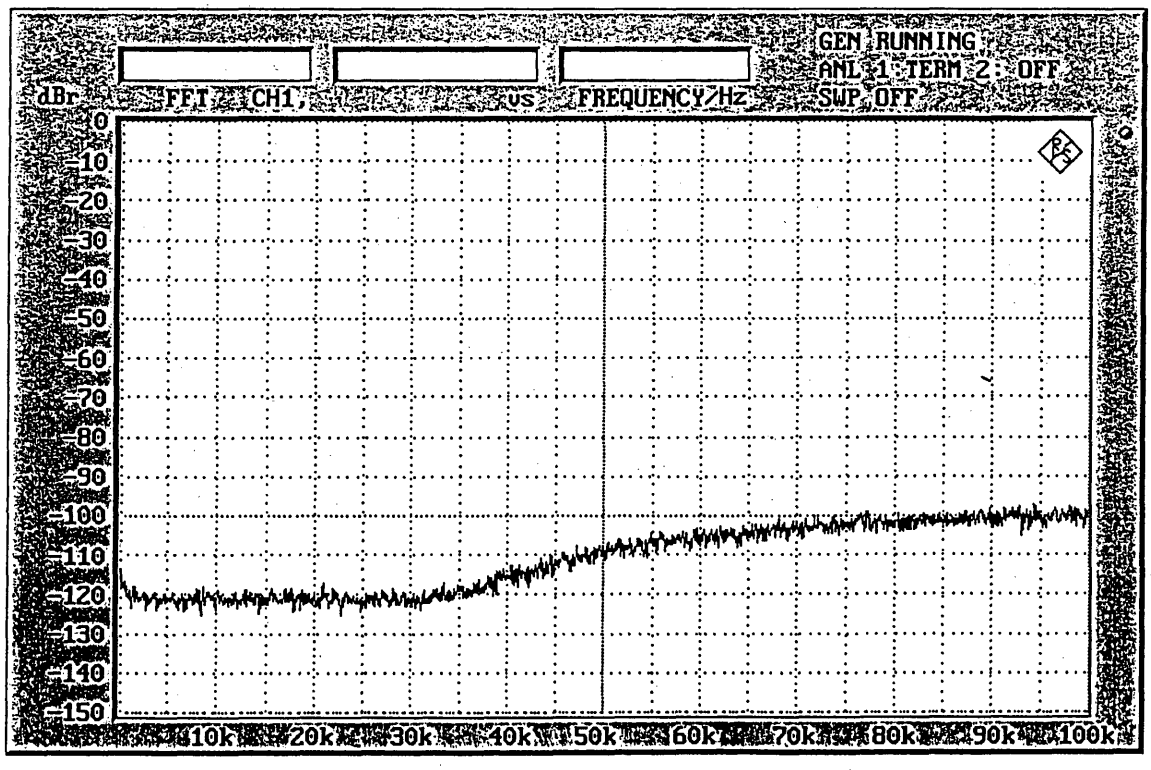


Fig.10 : FFT (outband noise. FFT points: 8192, averaging: 16, ～100kHz)

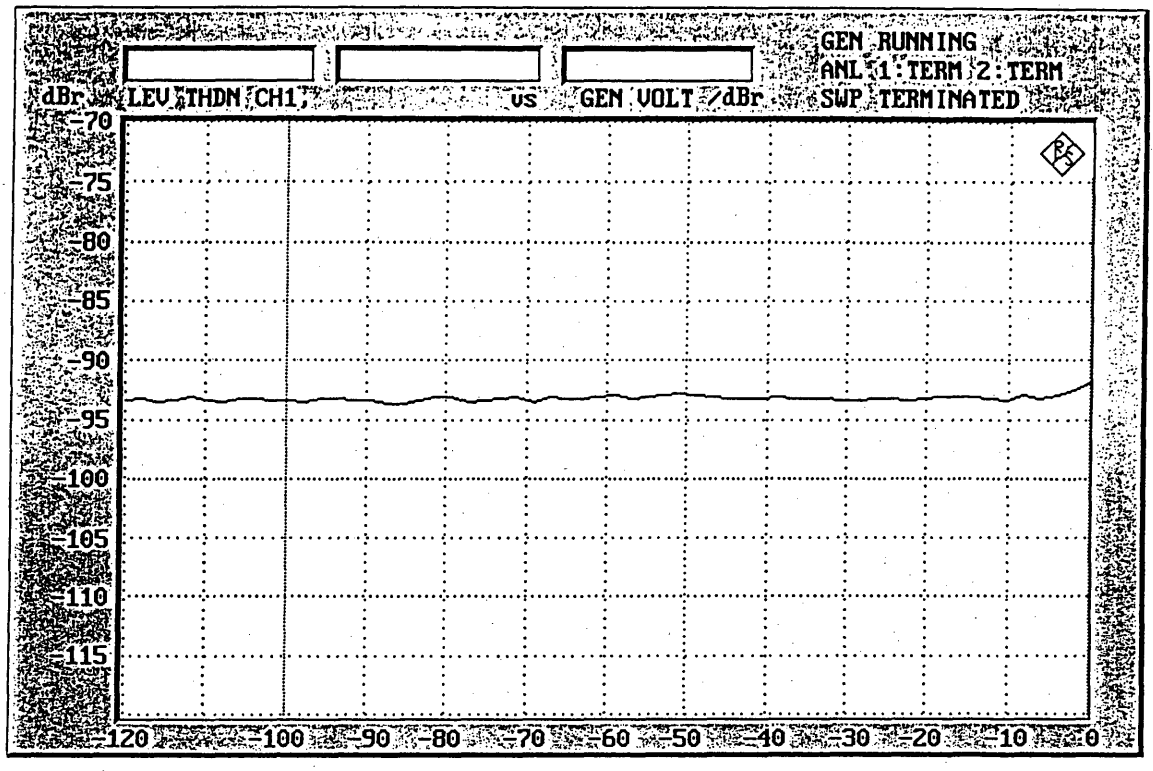


Fig.11 : THD+N vs. Input level (fin: 1kHz)

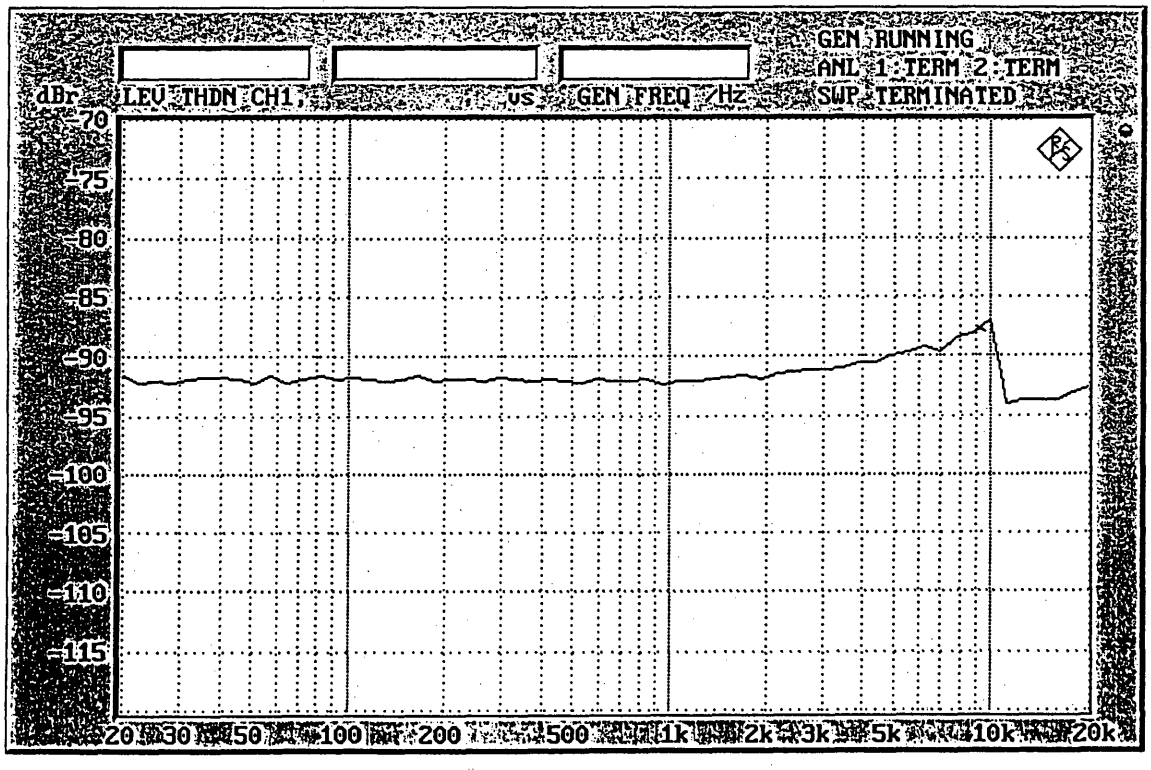


Fig.12 : THD+N vs. Input frequency (input level: 0dBFS)

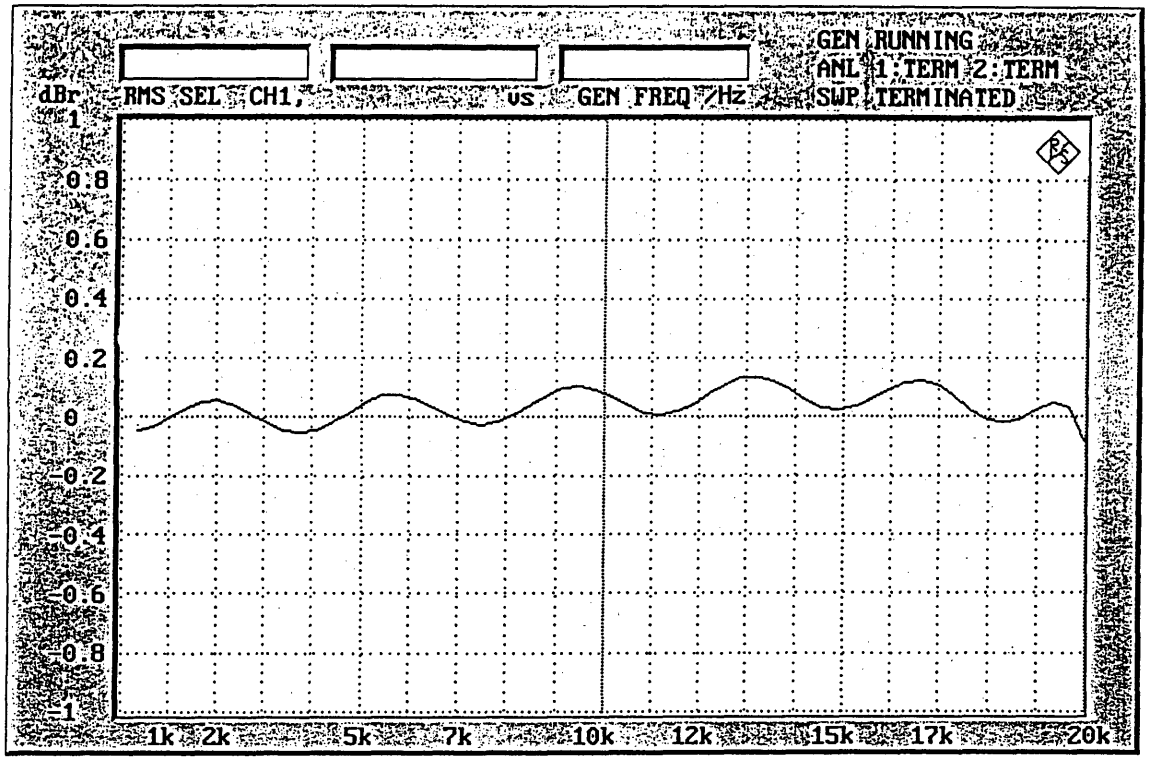


Fig.13 : Frequency response (level: 0dBr @1kHz)

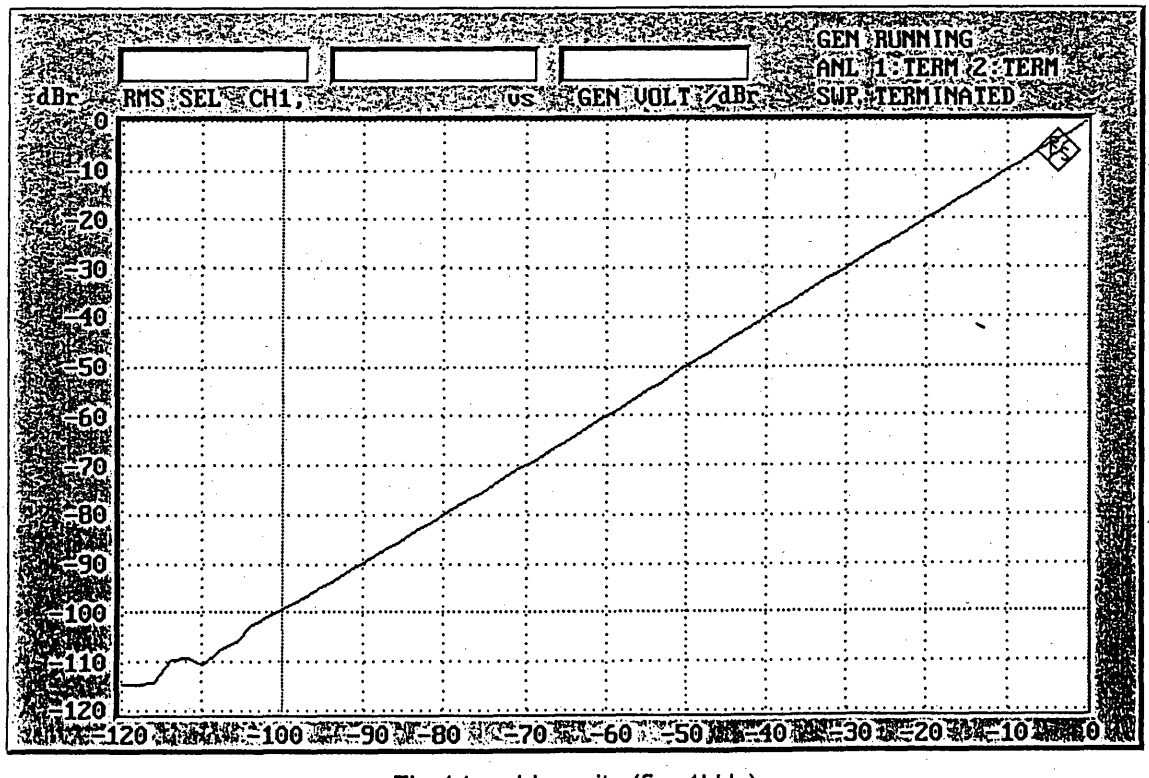


Fig.14 : Linearity (fin: 1kHz)

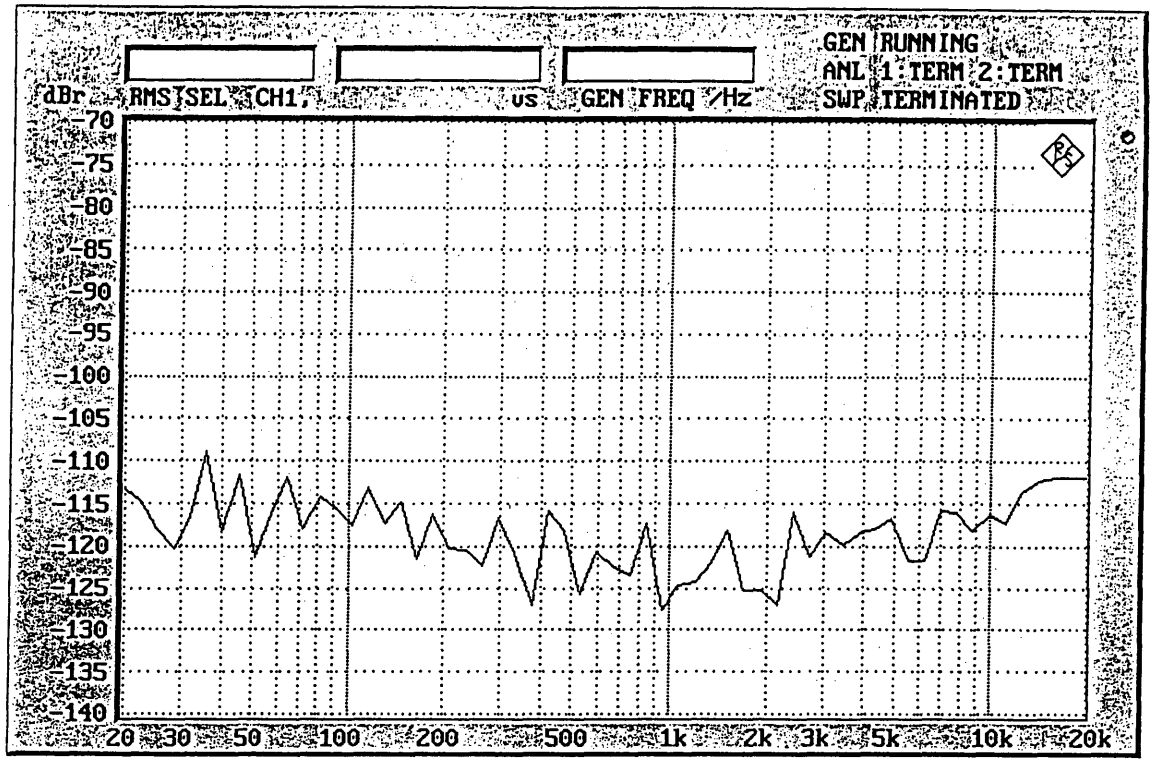


Fig.15 : Cross talk

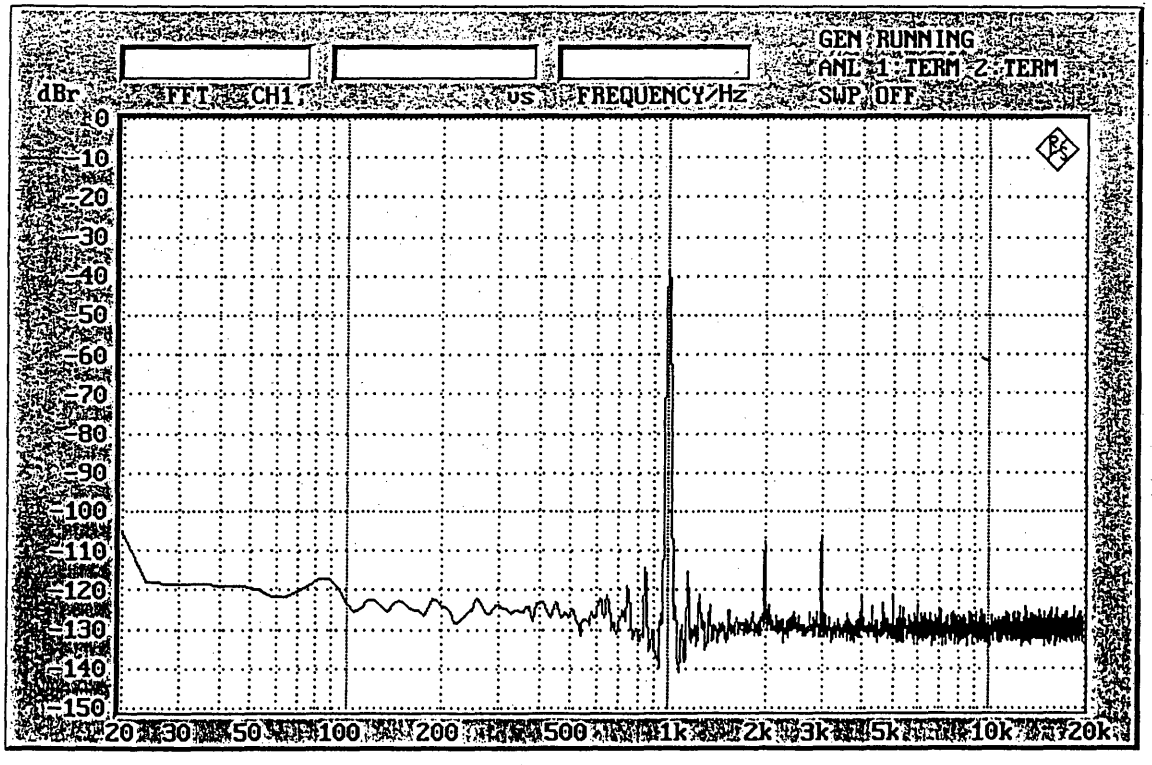


Fig.16 : FFT (input signal: 1kHz,0dBFS, FFT points: 8192,
averaging: 16, 30dB Notch filter: on)

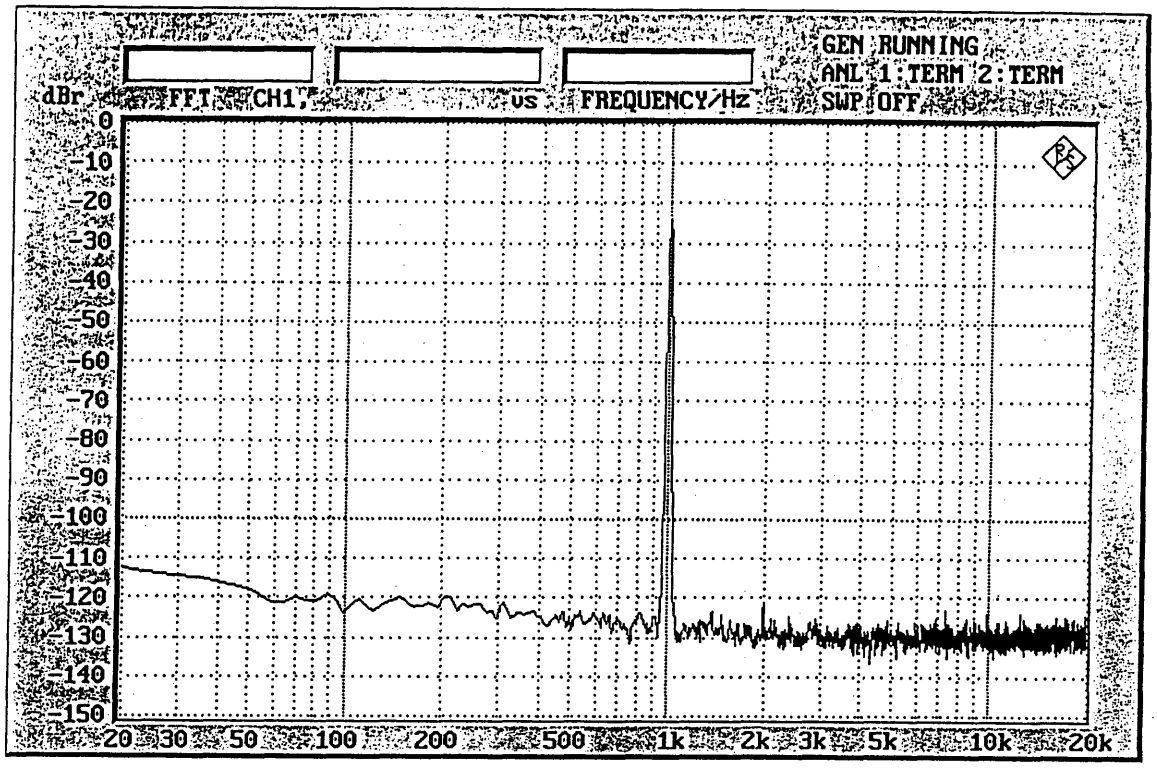


Fig.17 : FFT (input signal: 1kHz,-20dBFS, FFT points: 8192, averaging: 16)

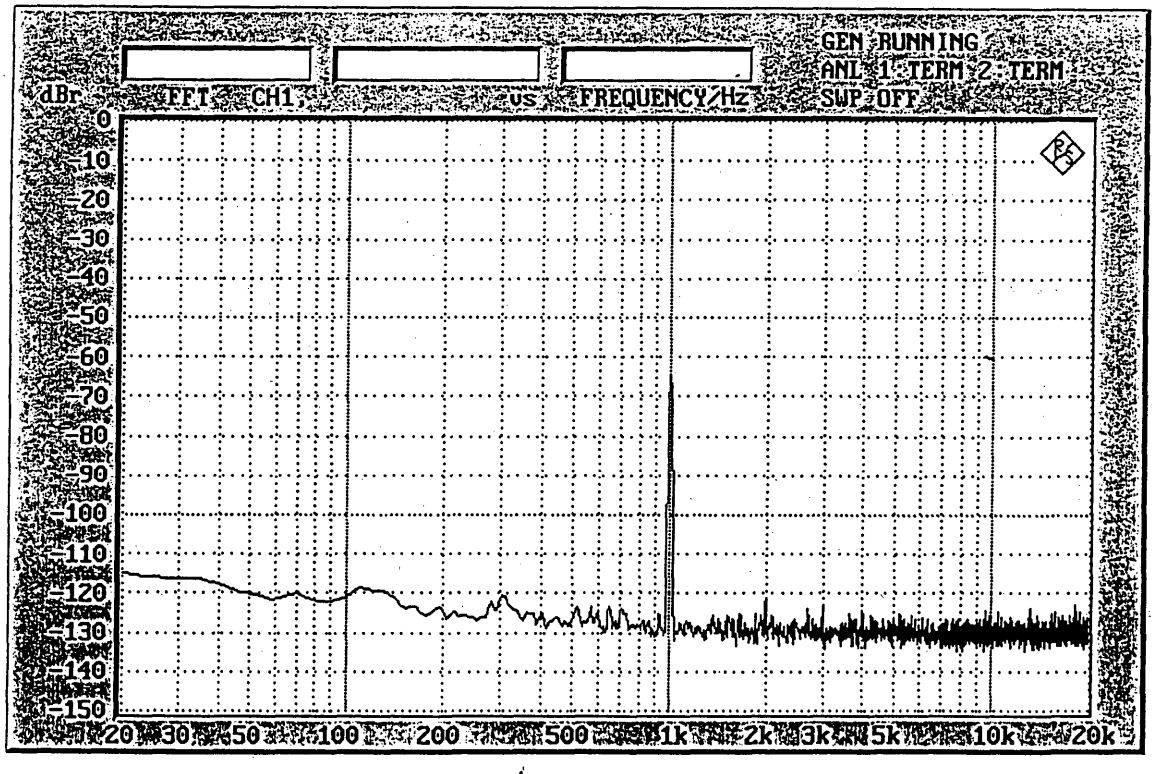


Fig.18 : FFT (input signal: 1kHz,-60dBFS, FFT points: 8192, averaging: 16)

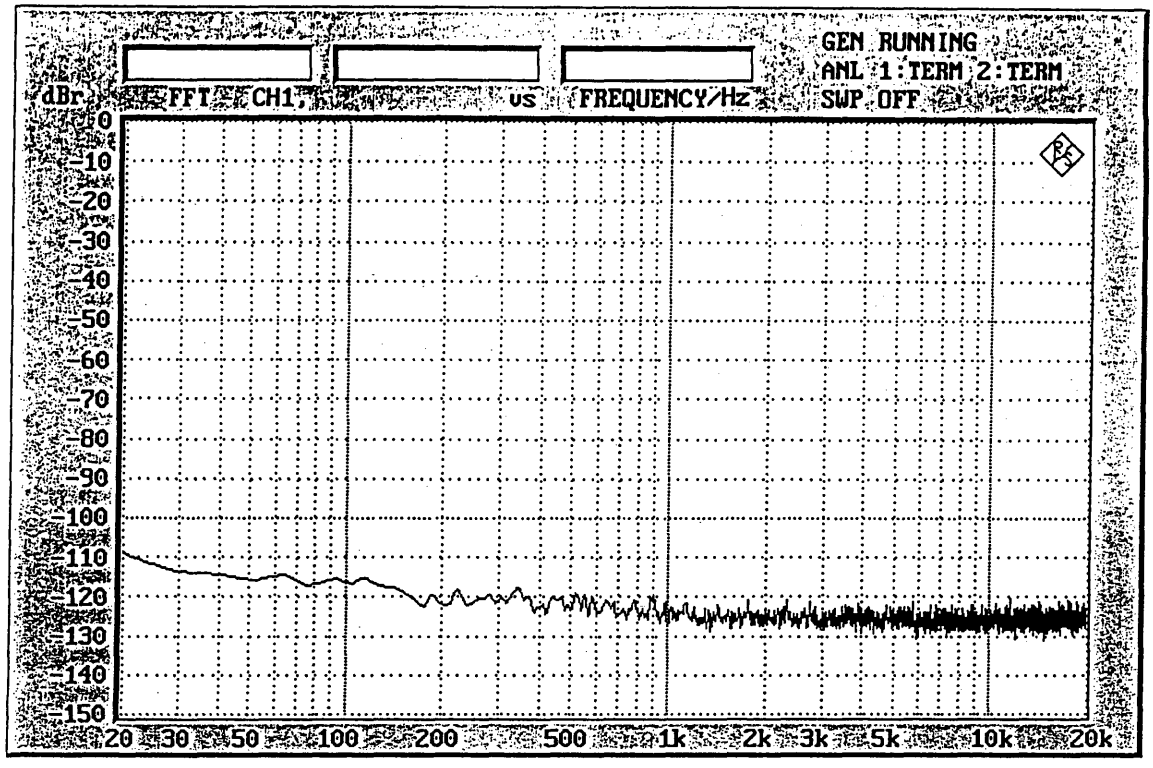


Fig.19 : FFT (noise floor. FFT points: 8192, averaging: 16)

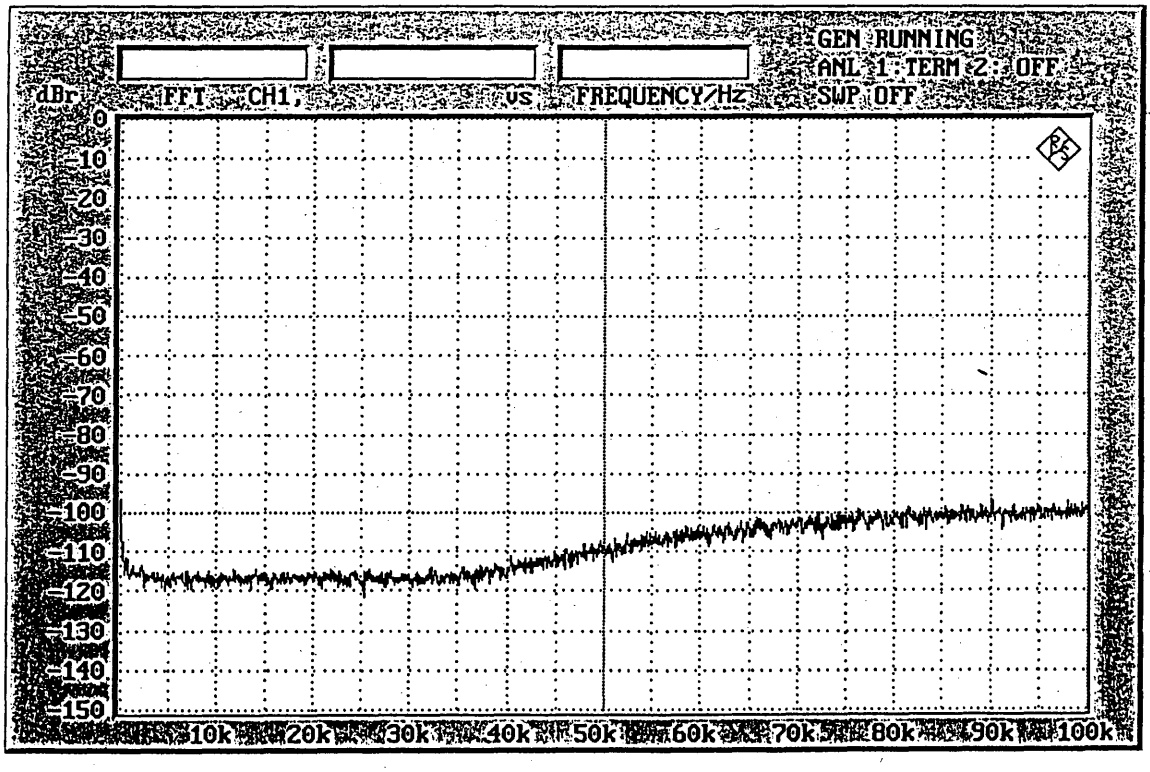
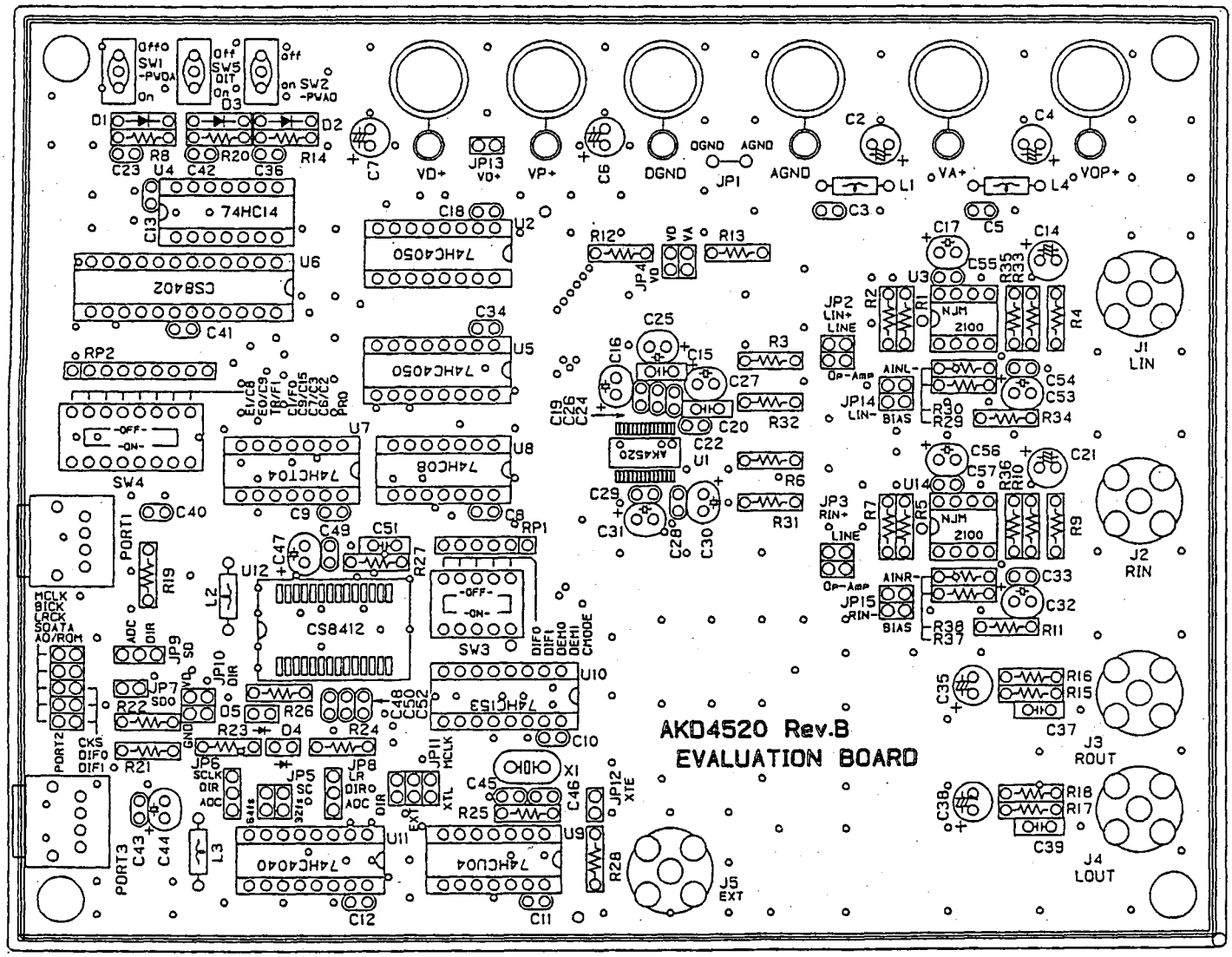
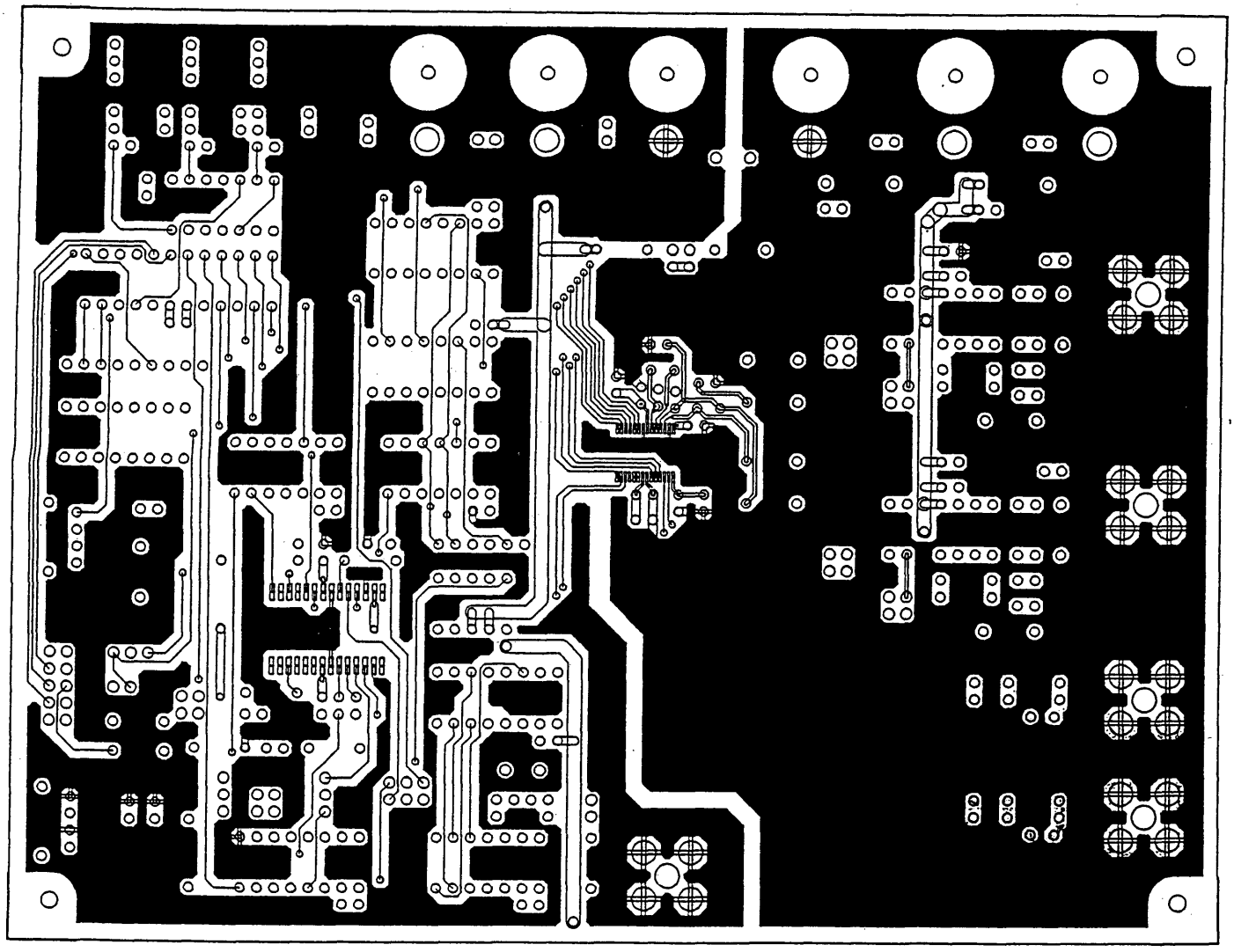
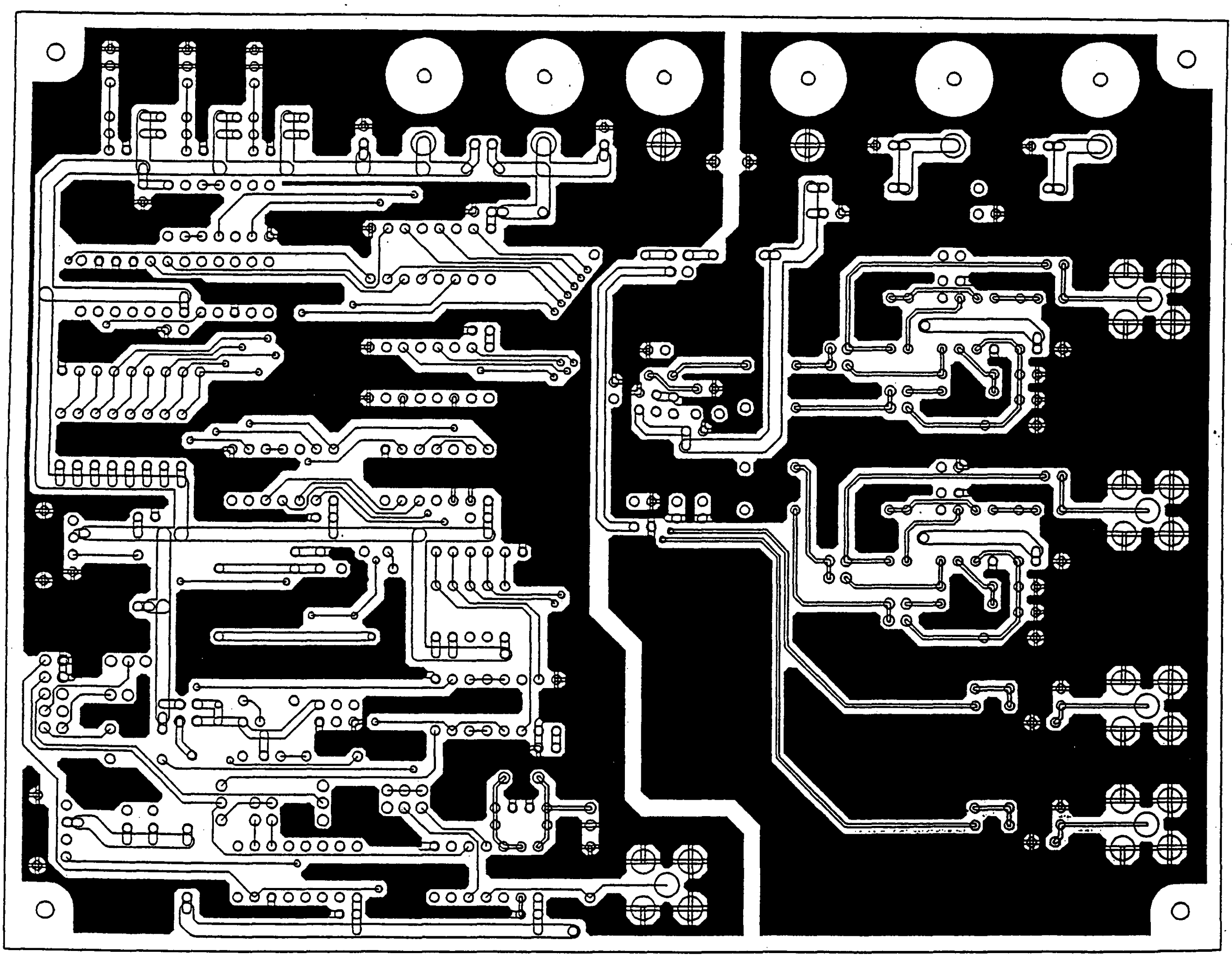


Fig.20 : FFT (outband noise. FFT points: 8192, averaging: 16, ~100kHz)


AKD4520 Rev.B
EVALUATION BOARD
AKD4520 Rev.B L1 SRK



AKD4520 Rev.B L1



AKD4520 Rev.B L2

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  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.