# 8-BIT MCU WITH VOICE SYNTHESIZER (*PowerSpeech*™ Series)

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## 1. GENERAL DESCRIPTION

The W588Bxxx is a 8-bit microcontroller-based speech synthesizer with PWM mode output to drive speaker directly. It is suitable for multi-tasking toy application.

The W588Bxxx family contains several items with different playback duration as shown below:

| Item | W588B003 | W588B006 | W588B009 | W588B012 | W588B015 |
|---|---|---|---|---|---|
| *Duration | 4 sec. | 7 sec. | 12 sec. | 16 sec. | 19 sec. |
| **Item** | **W588B020** | **W588B025** | **W588S030** | **W588B040** | **W588B050** |
| Duration | 25 sec. | 29 sec. | 32 sec. | 50 sec. | 58 sec. |
| **Item** | **W588B060** | **W588B080** | **W588B100** | **W588B120** | |
| Duration | 66 sec. | 100 sec. | 118 sec. | 133 sec. | |

Note:

*: The duration time is based on 5-bit MDPCM at 6KHz sampling rate. The firmware library and program code have been excluded from user's ROM space for the duration estimation.

## 2. FEATURES

- Wide Operating voltage: 2.4 ~ 5.5 volt
- System clock
  - 4 MHz at 2.4 ~ 5.5 volt
  - 8 MHz at 3.6 ~ 5.5 volt
- F/W speech synthesis
  - 5-bit MDPCM algorithm can be used
  - Programmable sample rate
- Provides DAC and/or PWM output to drive speaker (W588B003/006 only PWM)
- Built-in 1~2 timer (Timer0/1) for speech synthesis, tone melody and IR application
- Provide power management to save current consumption:
  - 4 ~ 8 MHz system clock, with Ring type oscillator
  - Stop mode for stopping all IC operations
- Provides 4 I/O and 4 Out in W588B003~B015 and 8I/O in W588B020~B120
- Provides IR carrier generation
- Provides watch dog timer
- Shared ROM for voice and program storage
- Support ***PowerScript***$^{TM}$ for developing codes in easy way
- Full-fledged development system
  - Source-level ICE debugger (Assembly and ***PowerScript***$^{TM}$ format)
  - Event synchronization mechanism
  - Compatible with W566B/C, W567S, W588S system
  - User-friendly GUI environment

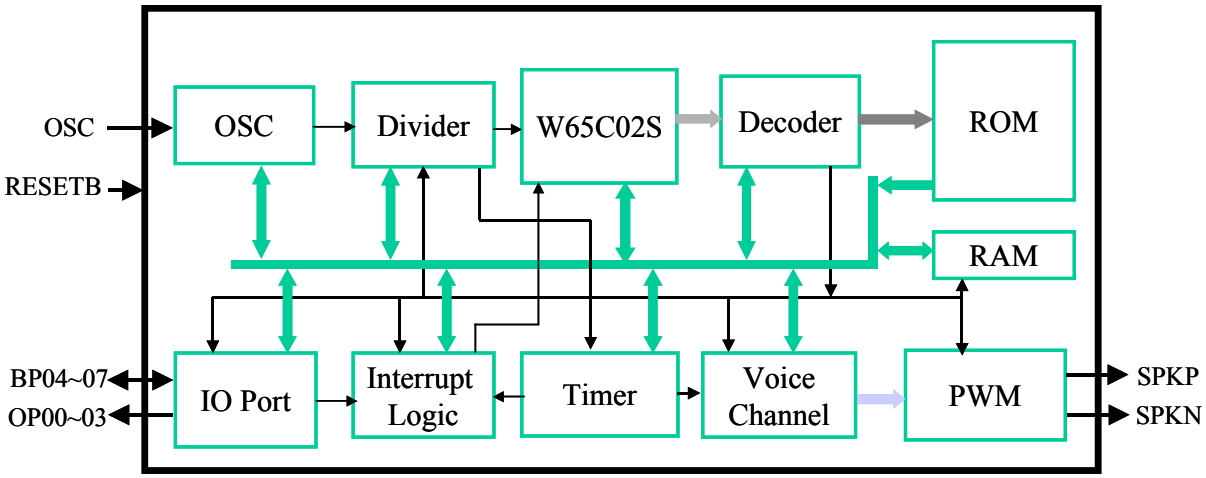
## 3. PIN DESCRIPTION

| NAME | I/O | DESCRIPTION |
|---|---|---|
| $V_{SS1}$ | - | Negative power supply for PWM |
| PWM+/DAC | O | PWM driver positive output / DAC output. |
| PWM- | O | PWM driver negative output |
| $V_{DD}1$ | - | Positive power supply for PWM |
| $V_{DD}$ | - | Positive power supply |
| /RESET | I | Active low reset pin, to reset whole device. |
| TEST | I | Test pin, internally pulled low. |
| *OP0[3:0] | O | Output port. The pins of OP0 are Inverter-type output. |
| BP0[7:4]<br>**BP0[0:3] | I/O | • I/O multiplexed port.<br>• As output port, the pins can be set as open–drain type or CMOS type.<br>• As input port, the pins can be set with pull-high resistor or not. Interrupt will be generated to release IC from STOP mode upon triggering.<br>• When BP0[7] is used as output pin, it can be the IR transmission carrier output for IR applications. |
| $V_{SS}$ | - | Negative power supply |
| OSC | I | Connect ROSC to Vss to generate the master clock |

*: Only for W588B003~B015

**: Only for W588B020~B120

## 4. BLOCK DIAGRAM




## 5. ELECTRICAL CHARACTERISTICS

### 5.1 Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITIONS | RATED VALUE | UNIT |
|---|---|---|---|---|
| Power Supply | $V_{DD} - V_{SS}$ | - | -0.3 to +7.0 | V |
| Input Voltage | $V_{IN}$ | All Inputs | $V_{SS}$ -0.3 to $V_{DD}$ +0.3 | V |
| Storage Temp. | $T_{STG}$ | - | -55 to +150 | °C |
| Operating Temp. | $T_{OPR}$ | - | 0 to +70 | °C |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

## 5.2 D.C. Characteristics

($V_{DD}$–$V_{SS}$ = 4.5 V, Ta = 25°C, No Load unless otherwise specified)

| PARAMETER | SYM. | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Operating Voltage | $V_{DD}$ | - | 2.4 | - | 5.5 | V |
| Operating Current | $I_{OP1}$ | No load, Fosc = 4 MHz | - | 3 | 5 | mA |
| Standby Current (STOP) | $I_{DD1}$ | No load | - | 1 | 2 | μA |
| Input Current (BP0) | $I_{IN}$ | VIN = 0V | -15 | - | -45 | μA |
| Output Current (BP0) | $I_{OL}$ | $V_{DD}$ = 3V, $V_{OUT}$ = 0.4V | 8 | - | - | mA |
| | $I_{OH}$ | $V_{DD}$ = 3V, $V_{OUT}$ = 2.6V | -4 | - | - | mA |
| Output Current (OP0) | $I_{OL}$ | $V_{DD}$ = 3V, $V_{OUT}$ = 0.4V | 4 | - | - | mA |
| | $I_{OH}$ | $V_{DD}$ = 3V, $V_{OUT}$ = 2.6V | -4 | - | - | mA |
| Output Current | $I_{OL1}$ | RL = 8 Ohm, | +200 | - | - | mA |
| SPK0+ / SPK0- | $I_{OH1}$ | Connection: [SPK+]----[RL]----[SPK-] | -200 | - | - | mA |
| DAC full scale current | $I_{DAC}$ | RL = 100Ω | -2.4<br>-4.0 | -3.0<br>-5.0 | -3.6<br>-6.0 | mA |
| Pull-low Resistor TEST | $R_{PL}$ | | 50 | - | 150 | KΩ |

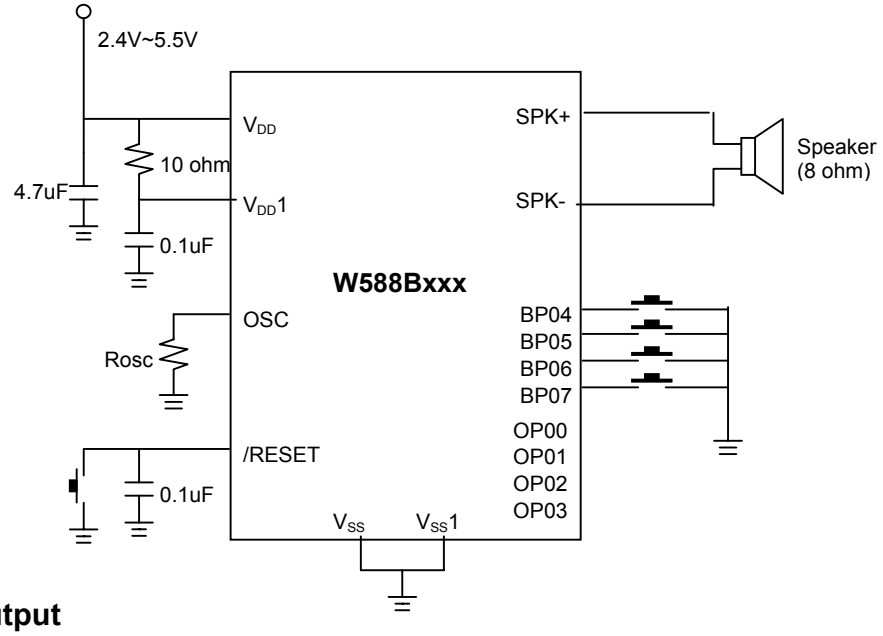
## 5.3 A.C. Characteristics

($V_{DD}$–$V_{SS}$ = 4.5 V, Ta= 25°C, No Load unless otherwise specified)

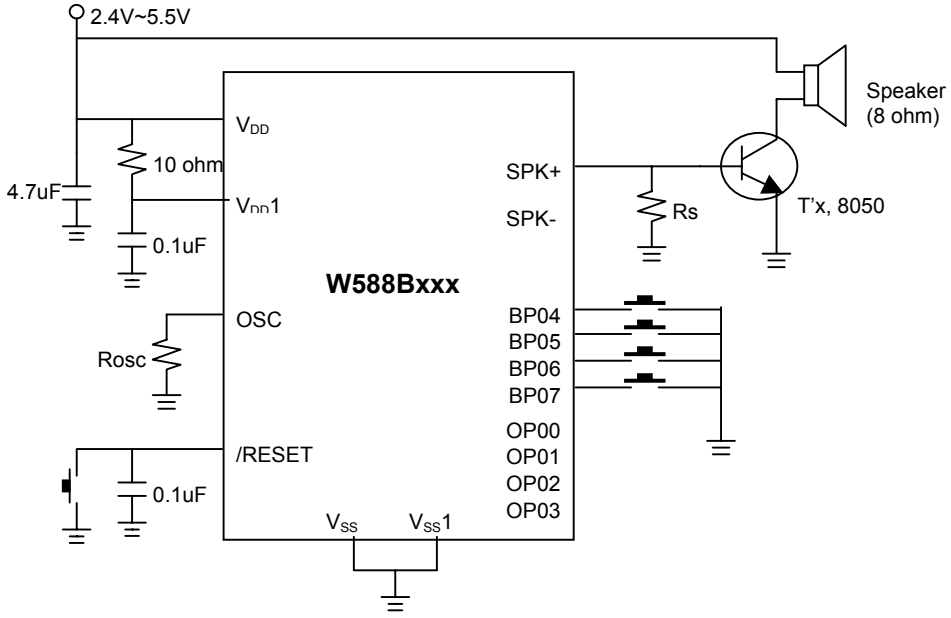
| PARAMETER | SYM. | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Main-clock Frequency | FM | ROSC = 300 Kohm<br>ROSC = 160 Kohm | 3.6<br>7.2 | 4<br>8 | 4.4<br>8.8 | MHz |
| Main-clock Wake-up Delay | WDm | Ring type, CPU clock = 4MHz | - | 3 | 5 | mS |
| Frequency Deviation by Voltage Drop<br>Main Oscillator, Ring | $\frac{\Delta F}{F}$ | CPU clock = 4 MHz, $\frac{F_{MAX} - F_{MIN}}{F_{MIN}}$ | - | 3 | 7.5 | % |
| Cycle Time | Tcyc | CPU clock = 4 MHz | 250 | - | DC | nS |
| Reset Signal Width | $T_{RST}$ | FM is enabled | 4 | - | - | Clocks of $F_M$ |

# 6. APPLICATION CIRCUIT

## 6.1 PWM Output




## 6.2 DAC Output




Notes:

1. The typical value of Rosc is 160 KΩ for 8MHz and 300 KΩ for 4MHz and should be connected to GND ($V_{SS}$).
2. In PCB layout, $V_{SS}1$ should be connected to $V_{SS}$; $V_{DD}1$ should be connected to $V_{DD}$.
3. The Rs value is suggested in 270Ω ~ 1KΩ to limit too large SPK+ output current flowing into transistor.
4. The capacitor, 0.1uF, shunted between $V_{DD}$/$V_{DD}1$ and GND ($V_{SS}$/$V_{SS}1$) is necessary.
5. The 10Ω and 4.7uF between $V_{DD}$, $V_{DD}1$ and GND are optional to reduce probability of latch-up occurring.
6. The I/O in W588B020~B120 is BP00~BP07.
7. The above application circuits are for reference only. No warranty for mass production.

## 7. REVISION HISTORY

| REVISION | DATE | MODIFICATIONS |
|---|---|---|
| A1 | Oct. 23, 2002 | Preliminary release. |
| A2 | Feb. 20, 2003 | W588B020~B030: 8I/O<br>Add PWM and DAC application circuit |
| A3 | May 15, 2003 | Add watch dog timer feature<br>Page2: OP0[3:0] only for W588B003~015 |
| A4 | June 5, 2003 | Add new part number: W588B040 ~ W588B120 |

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