Winbond Electronics Corp.

64K × 8 ELECTRICALLY ERASABLE EPROM

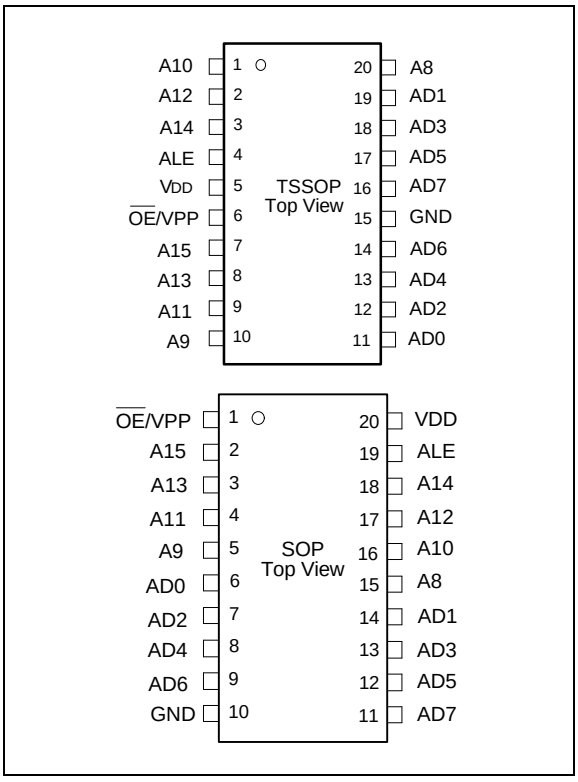
GENERAL DESCRIPTION

The W27LE520 is a high speed, low power Electrically Erasable and Programmable Read Only Memory organized as 65,536 × 8 bits. It includes latches for the lower 8 address lines to multiplex with the 8 data lines. To cooperate with the MCU, this device could save the external TTL component, also cost and space. It requires only one supply in the range of 3.0V to 3.6V or 4.5V to 5.5V in normal read mode. The W27LE520 provides an electrical chip erase function. It will be a great convenient when you need to change/update the contents in the device.

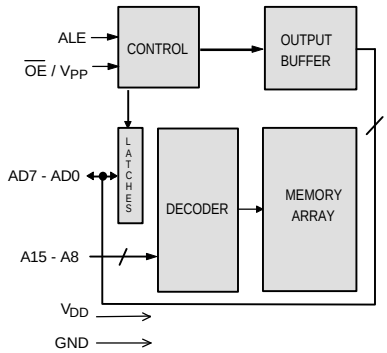
FEATURES

- High speed access time: 70/90 nS (max.)
- Read operating current: 8/20 mA (max.)
- Erase/Programming operating current 30 mA (max.)
- Standby current: 20/100 μA (max.)
- Unregulated battery power supply range, 3.0V to 3.6V and 4.5V to 5.5V
- +13V erase and programming voltage
- High Reliability CMOS Technology
  - 2K V ESD Protection
  - 200 mA Latchup Immunity
- Fully static operation
- All inputs and outputs directly LVTTL/CMOS compatible
- Three-state outputs
- Available packages: 20-pin TSSOP and 20-pin SOP

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
AD0–AD7	Address/Data Inputs/Outputs
A8–A15	Address Inputs
ALE	Address Latch Enable
$\overline{OE}$/VPP	Output Enable, Program/Erase Supply Voltage
VDD	Power Supply
GND	Ground

FUNCTIONAL DESCRIPTION

Read Mode

Unlike conventional UVEPROMs, which has $\overline{CE}$ and $\overline{OE}$ two control functions, the W27LE520 has one $\overline{OE}$/VPP and one ALE (address_latch_enable) control functions. The ALE makes lower address A[7:0] to be latched in the chip when it goes from high to low, so that the same bus can be used to output data during read mode. i.e. lower address A[7:0] and data bus DQ[7:0] are multiplexed. $\overline{OE}$/VPP controls the output buffer to gate data to the output pins. When addresses are stable, the address access time (TACC) is equal to the delay from ALE to output (TCE), and data are available at the outputs TOE after the falling edge of $\overline{OE}$/VPP, if TACC and TCE timings are met.

Erase Mode

The erase operation is the only way to change data from "0" to "1." Unlike conventional UVEPROMs, which use ultraviolet light to erase the contents of the entire chip (a procedure that requires up to half an hour), the W27LE520 uses electrical erasure. Generally, the chip can be erased within 100 mS by using an EPROM writer with a special erase algorithm.

There are two ways to enter Erase mode. One is to raise $\overline{OE}$/VPP to VPE (13V), VDD = VDE (6.5V), A9 = VHH (13V), A10 = high A8&A11 = low, and all other address pins include AD[7:0] keep at fixed low or high. Pulsing ALE high starts the erase operation. The other way is somewhat like flash, by programming two consecutive commands into the device and then enter Erase mode. The two commands are loading Data = AA(hex) to Addr. = 5555(hex) and Data = 10(hex) to Addr. = 2AAA(hex). Be careful to note that the ALE pulse widths of these two commands are different: One is 50 µS, while the other is 100 mS. Please refer to the Smart Erase Algorithm 1 & 2.

Erase Verify Mode

The device will enter the Erase Verify Mode automatically after Erase Mode. Only power down the device can force the device enter Normal Read Mode again.

Program Mode

Programming is the only way to change cell data from "1" to "0." The program mode is entered when $\overline{OE}$/VPP is raised to VPP (13V), VDD = VDP (6.5V), the address pins equal the desired addresses, and the input pins equal the desired inputs. Pulsing ALE high starts the programming operation.

Program Verify Mode

The device will enter the Program Verify Mode automatically after Program Mode. Only power down the device can force the device enter Normal Read Mode again.

Erase/Program Inhibit

Erase or program inhibit mode allows parallel erasing or programming of multiple chips with different data. When ALE low, erasing or programming of non-target chips is inhibited, so that except for the ALE and $\overline{OE}$/VPP pins, the W27LE520 may have common inputs.

Standby Mode

The standby mode significantly reduces VDD current. This mode is entered when ALE and $\overline{OE}$/VPP keep high. In standby mode, all outputs are in a high impedance state.

System Considerations

An EPROM's power switching characteristics require careful device decoupling. System designers are interested in three supply current issues: standby current levels (I_{SB}), active current levels (I_{DD}), and transient current peaks produced by the falling and rising edges of ALE Transient current magnitudes depend on the device output's capacitive and inductive loading. Proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a
0.1 µF ceramic capacitor connected between its V_{DD} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{DD} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

TABLE OF OPERATING MODES

(V_{PP} = 13V, V_{PE} = 13V, V_{HH} = 12V, V_{DP} = 6.5V, V_{DE} = 6.5V, V_{DD} = 3.3V or 5.0V, V_{DI} = 5.0V, X = V_{IH} or V_{IL})

MODE	PIN				
	ALE	**$\overline{OE}$/V_{PP}**	**OTHER ADDRESS**	**V_{DD}**	**AD[7:0]**
Address Latch Enable	V_{IH}	V_{IH}	A_{IN}	V_{DD}	A[7:0]
Read	V_{IL}	V_{IL}	A_{IN}	V_{DD}	D_{OUT}
Output Disable	V_{IL}/ V_{IH}	V_{IH}	X	V_{DD}	High Z
Standby	V_{IH}	V_{IH}	X	V_{DD}	A[7:0]
Program	V_{IH}	V_{PP}	A_{IN}	V_{DP}	D_{IN}
Erase 1	V_{IH}	V_{PE}	A8&A11 = V_{IL}, A9 = V_{PE}, A10 = V_{IH}, Others = X	V_{DE}	X
Erase 2	V_{IH}	V_{PE}	First command: Addr. = 5555 (hex)	V_{DE}	AA(hex)
			Second command: Addr. = 2AAA (hex)	V_{DE}	10(hex)
Product Identifier-manufacturer	V_{IL}	V_{IL}	A8 = V_{IL}, A9 = V_{HH}, Others = X	V_{DI}	DA(Hex)
Product Identifier-device	V_{IL}	V_{IL}	A8 = V_{IH}, A9 = V_{HH}, Others = X	V_{DI}	1F(Hex)

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Ambient Temperature with Power Applied	-55 to +125	°C
Storage Temperature	-65 to +150	°C
Voltage on all Pins with Respect to Ground Except $\overline{OE}$/V_{PP}, A9 and V_{DD} Pins	-2.0 to +7.0	V
Voltage on $\overline{OE}$/V_{PP} Pin with Respect to Ground	-2.0 to +7.0	V
Voltage on A9 Pin with Respect to Ground	-2.0 to +7.0	V
Voltage V_{DD} Pin with Respect to Ground	-2.0 to +14.0	V

Notes:
1. Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.
2. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 nS. Maximum output pin voltage is V_{DD} +0.75V DC which may overshoot to +7.0V for pulses of less than 20 nS.

DC Erase Characteristics

(T_A = 25° C ±5° C, V_{DD} = 6.5V ±0.25V)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I_{LI}	V_{IN} = V_{IL} or V_{IH}	-10	-	10	µA
V_{DD} Erase Current	I_{CP}	ALE = V_{IH}, $\overline{OE}$/V_{PP} = V_{PE} A8 & A11 = V_{IL}, A9 = V_{PE}, A10 = V_{IH}, Others = X	-	-	30	mA
V_{PP} Erase Current	I_{PP}	ALE = V_{IH}, $\overline{OE}$/V_{PP} = V_{PE} A8 & A11 = V_{IL}, A9 = V_{PE}, A10 = V_{IH}, Others = X	-	-	30	mA
Input Low Voltage	V_{IL}	-	-0.3	-	0.8	V
Input High Voltage	V_{IH}	-	2.4	-	V_{DD}+0.3	V
Output Low Voltage (Verify)	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage (Verify)	V_{OH}	I_{OH} = -0.4 mA	2.4	-	-	-
A9 SID Voltage	V_{HH}	V_{DD} = 5V ±10%	11.5	12	12.5	V
A9 Erase Voltage	V_{PE}	-	12.75	13	13.25	V
V_{PP} Erase Voltage	V_{PE}	-	12.75	13	13.25	V
V_{DD} Supply Voltage (Erase & Erase Verify)	V_{DE}	-	6.25	6.5	6.75	V

Note: V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

CAPACITANCE

(V_{DD} = 3.0V to 3.6V or 4.5V to 5.5V, T_A = 25° C, f = 1 MHz)

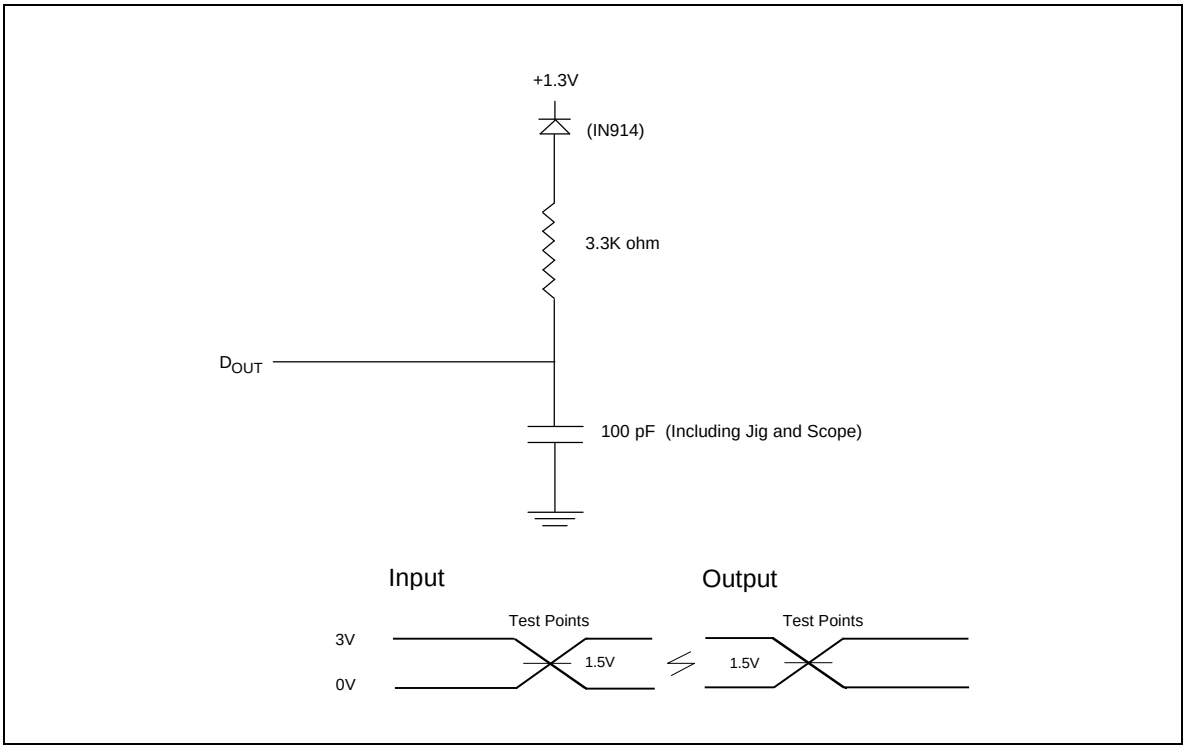
PARAMETER	SYMBOL		MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	12	pF

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V/3V
Input Rise and Fall Times	10 nS
Input and Output Timing Reference Level	1.5V/1.5V
Output Load	C_L = 100 pF, I_{OH}/I_{OL} = -0.4 mA/2.1 mA

AC Test Load and Waveforms



READ OPERATION DC CHARACTERISTICS

(V_{DD} = 3.0V to 3.6V or 4.5V to 5.5V, T_A = 0 to 70° C)

PARAMETER	SYM.	CONDITIONS		LIMITS			UNIT
				MIN.	TYP.	MAX.	
Input Load Current	I_{LI}	V_{IN} = 0V to V_{DD}		-5	-	5	µA
Output Leakage Current	I_{LO}	V_{OUT} = 0V to V_{DD}		-5	-	5	µA
Standby V_{DD} Current (CMOS input)	I_{SB}	V_{DD} = 3.0V to 3.6V	$\overline{ALE}$ = V_{DD} ±0.3V, $\overline{OE}$/VPP = V_{DD} ±0.3V All others inputs = GND/ V_{DD} ±0.3V	-	-	20	µA
		V_{DD} = 4.5V to 5.5V			-	100	
V_{DD} Operating Current	I_{DD}	V_{DD} = 3.0V to 3.6V	ALE = VIL, IOUT = 0 mA f = 5 MHz	-	-	8	mA
		V_{DD} = 4.5V to 5.5V		-	-	20	
Input Low Voltage	V_{IL}	-		-0.6	-	0.8	V
Input High Voltage	V_{IH}	-		2.0	-	V_{DD} +0.3	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -0.4 mA		2.4	-	-	V

READ OPERATION AC CHARACTERISTICS

(V_{DD} = 3.0V to 3.6V or 4.5V to 5.5V, T_A = 0 to 70° C)

PARAMETER	SYM.	W27LE520-70		W27LE520-90		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address Latch Enable Access Time	T_{CE}	-	70	-	90	nS
Address Latch Enable Width	T_{ALE}	45	-	45	-	nS
Address Access Time	T_{ACC}	-	70	-	90	nS
Address Setup Time	T_{AS}	15	-	15	-	nS
Address Hold Time	T_{AH}	15	-	15	-	nS
Output Enable Access Time	T_{OE}	-	35	-	35	nS
$\overline{OE}$ /VPP High to High-Z Output	T_{DF}	-	25	-	25	nS
Output Hold from Address Change	T_{OH}	0	-	0	-	nS

Note: V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

DC PROGRAMMING CHARACTERISTICS

(V_{DD} = 6.5V ±0.25V, T_A = 25° C ±5° C)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}	-10	-	10	µA
V_{DD} Program Current	I_{CP}	ALE = V_{IH}, $\overline{OE}/V_{PP} = V_{PP}$	-	-	30	mA
V_{PP} Program Current	I_{PP}	ALE = V_{IH}, $\overline{OE}/V_{PP} = V_{PP}$	-	-	30	mA
Input Low Voltage	V_{IL}	-	-0.3	-	0.8	V
Input High Voltage	V_{IH}	-	2.4	-	V_{DD} +0.5	V
Output Low Voltage (Verify)	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage (Verify)	V_{OH}	I_{OH} = -0.4 mA	2.4	-	-	V
A9 Silicon I.D. Voltage	V_{HH}	V_{DD} = 5V ±10%	11.5	12.0	12.5	V
V_{PP} Program Voltage	V_{PP}	-	12.75	13.0	13.25	V
V_{DD} Supply Voltage (Program)	V_{DP}	-	6.25	6.5	6.75	V

AC PROGRAMMING/ERASE CHARACTERISTICS

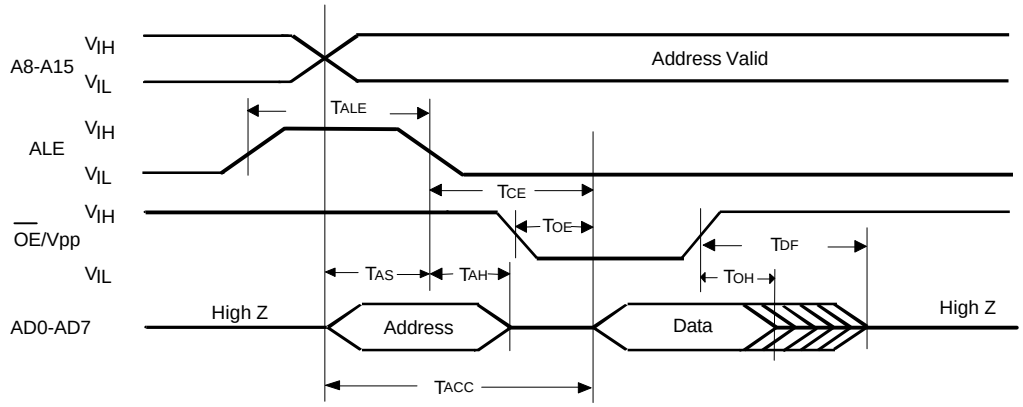
(V_{DD} = 6.5V ±0.25V, T_A = 25° C ±5° C)

PARAMETER	SYM.	LIMITS			UNIT
		MIN.	TYP.	MAX.	
$\overline{OE}/V_{PP}$ Pulse Rise Time	T_{PRT}	50	-	-	nS
Address Latch Enable Width	T_{ALE}	500	-	-	nS
ALE Program Pulse Width	T_{PPW}	47.5	50	52.5	µS
ALE Erase Pulse Width	T_{EPW}	95	100	105	mS
ALE Erase Pulse Width 1	T_{EPW1}	47.5	50	52.5	µS
ALE Erase Pulse Width 2	T_{EPW2}	95	100	105	mS
Latched Address Setup Time	T_{LAS}	100	-	-	nS
Latched Address Hold Time	T_{LAH}	100	-	-	nS
Address Setup Time	T_{AS}	2.0	-	-	µS
Address Hold Time	T_{AH}	0	-	-	µS
$\overline{OE}/V_{PP}$ Setup Time	T_{OES}	2.0	-	-	µS
$\overline{OE}/V_{PP}$ Hold Time	T_{OEH}	2.0	-	-	µS
Data Setup Time	T_{DS}	2.0	-	-	µS
Data Hold Time	T_{DH}	2.0	-	-	µS
Data Valid from $\overline{OE}/V_{PP}$ Low during Erase Verify	T_{EOE}	-	-	150	nS
Data Valid from $\overline{OE}/V_{PP}$ Low during Program Verify	T_{POE}	-	-	150	nS
$\overline{OE}/V_{PP}$ High to Output High Z	T_{DFP}	0	-	130	nS
$\overline{OE}/V_{PP}$ High Voltage Delay After ALE Low	T_{VS}	2.0	-	-	µS
$\overline{OE}/V_{PP}$ Recovery Time	T_{VR}	2.0	-	-	µS

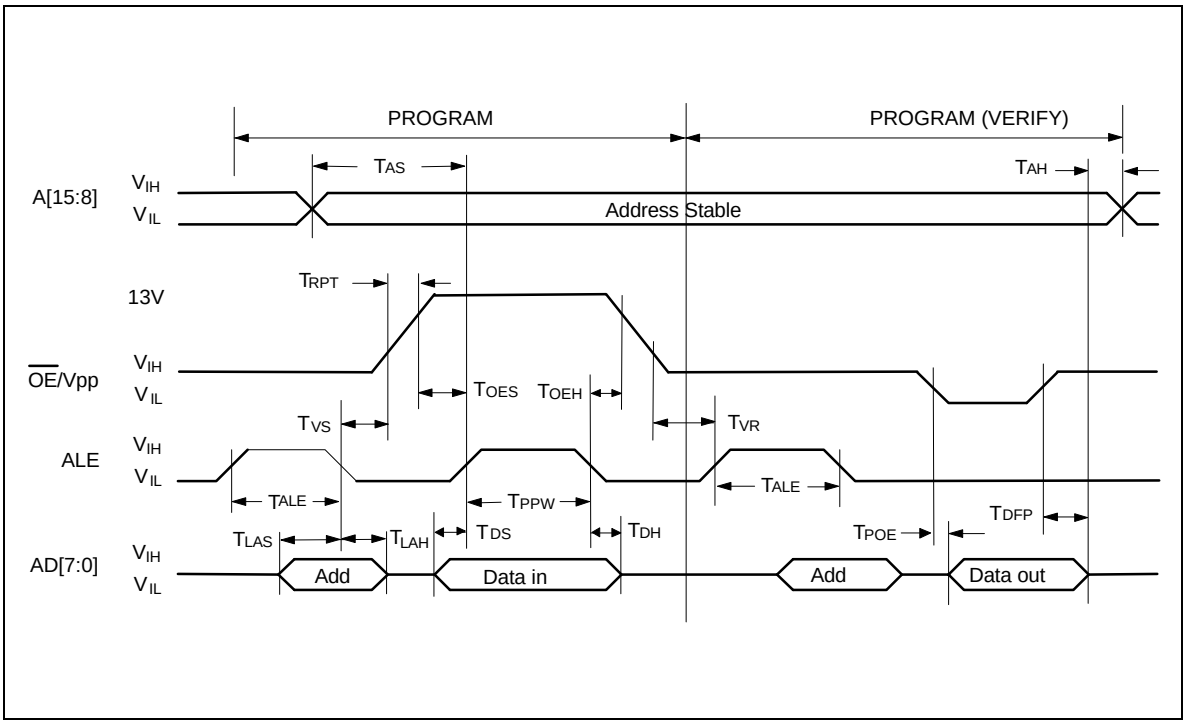
Note: V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

TIMING WAVEFORMS

AC Read Waveform

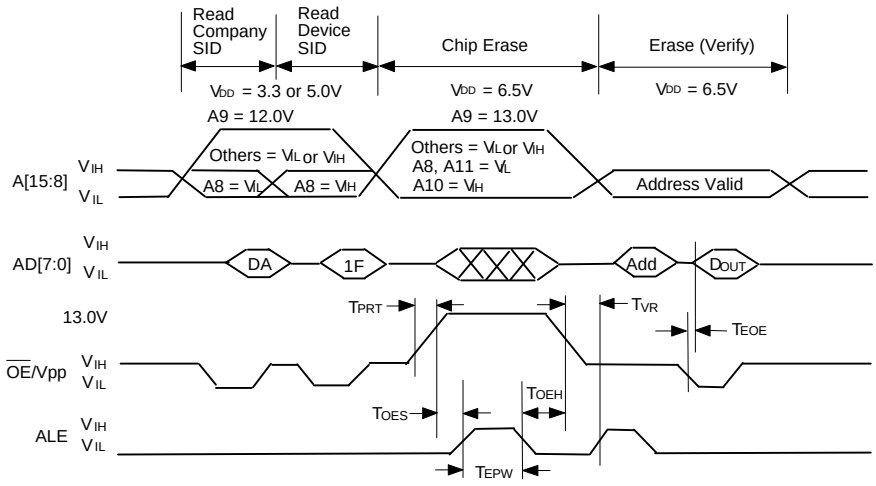


Programming Waveform

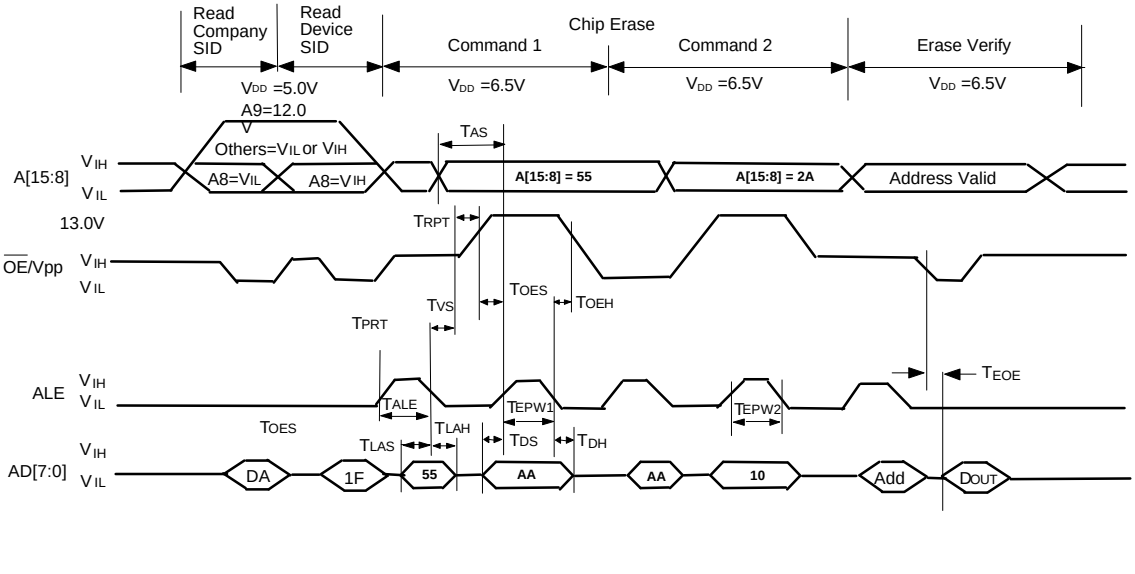


Timing Waveforms, continued

Erase Waveform 1

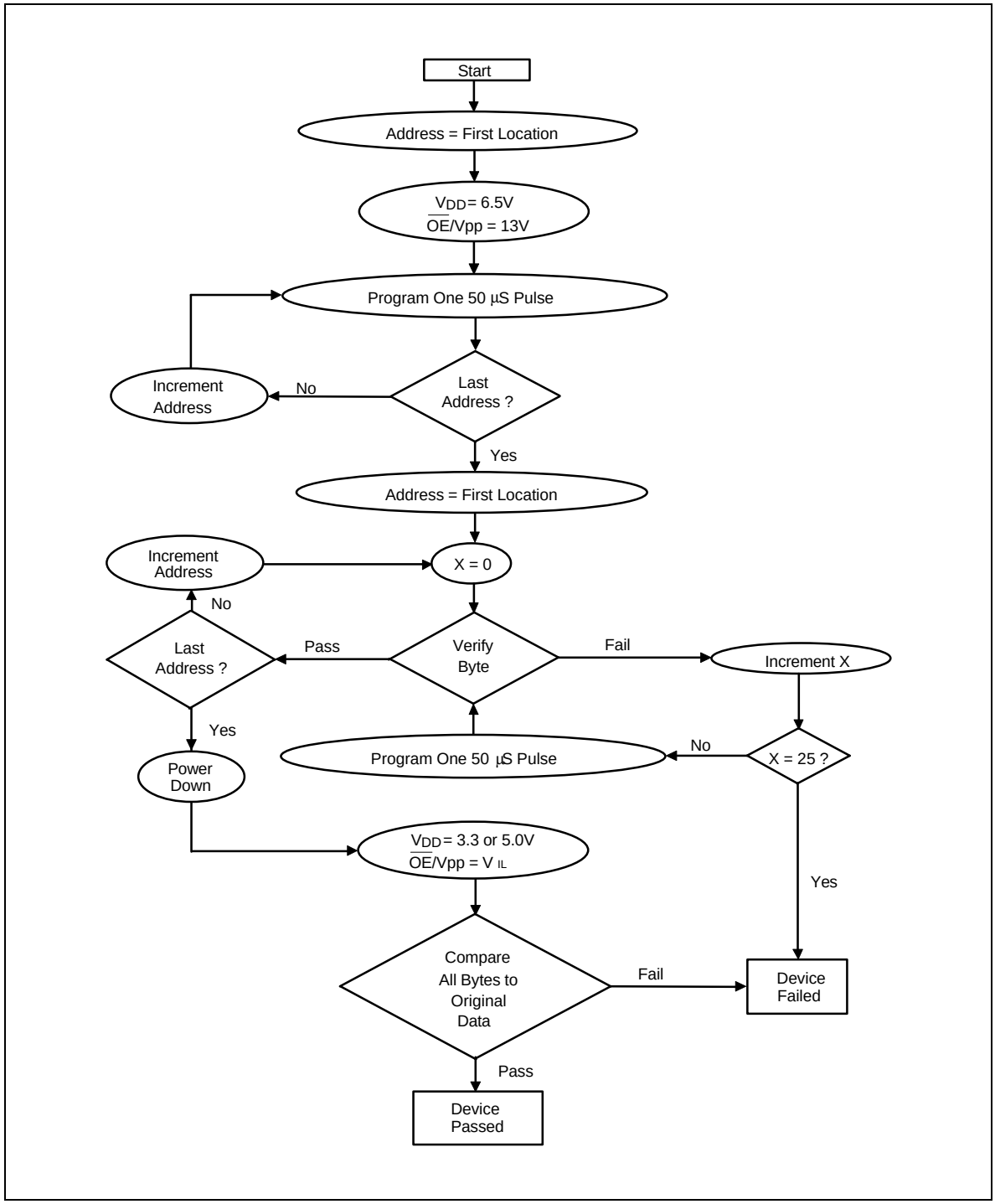


Erase Waveform 2

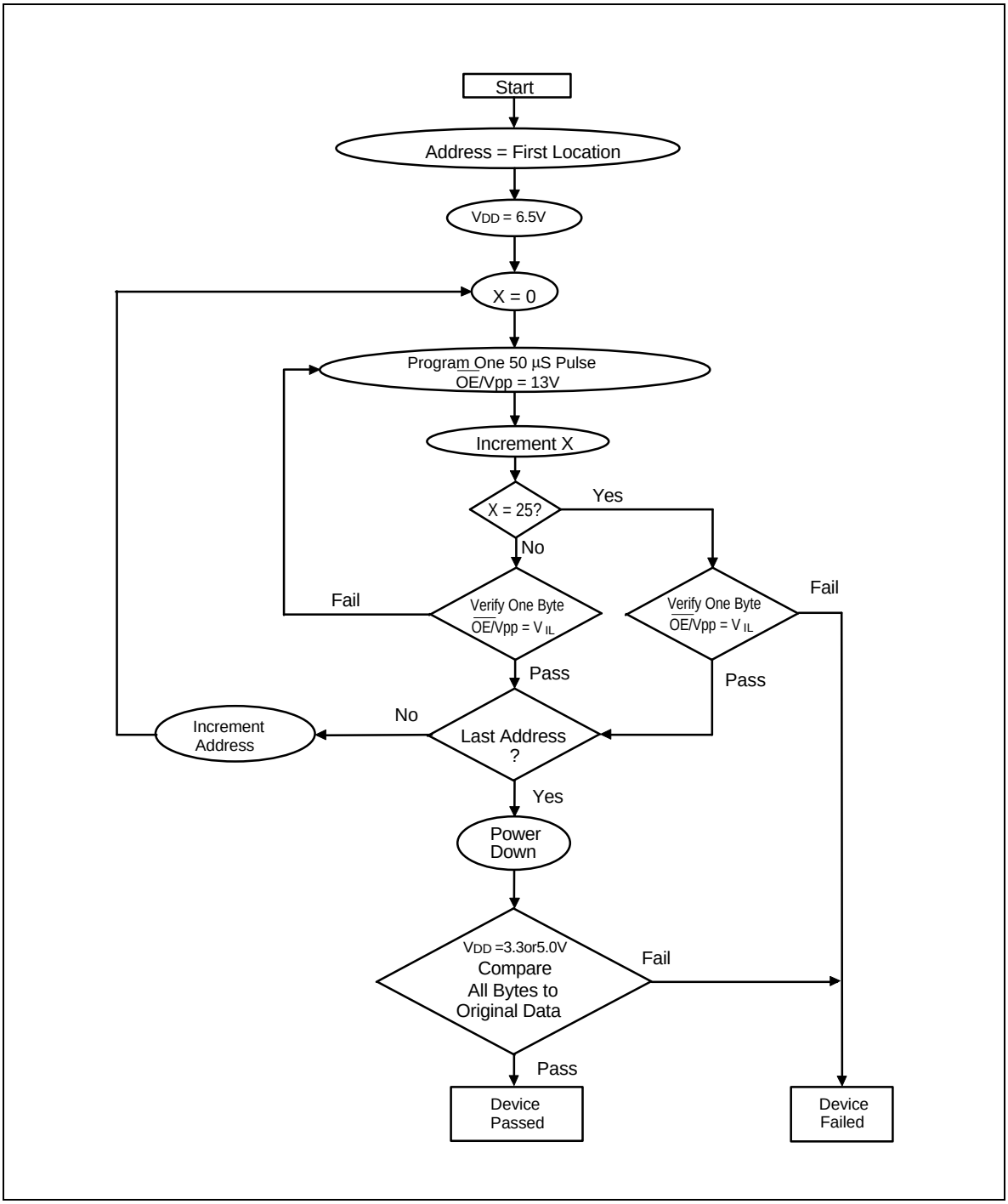


Note: First command Address = 5555(hex) with Data = AA(hex)
Second command Address = 2AAA(hex) with Data = 10(hex)

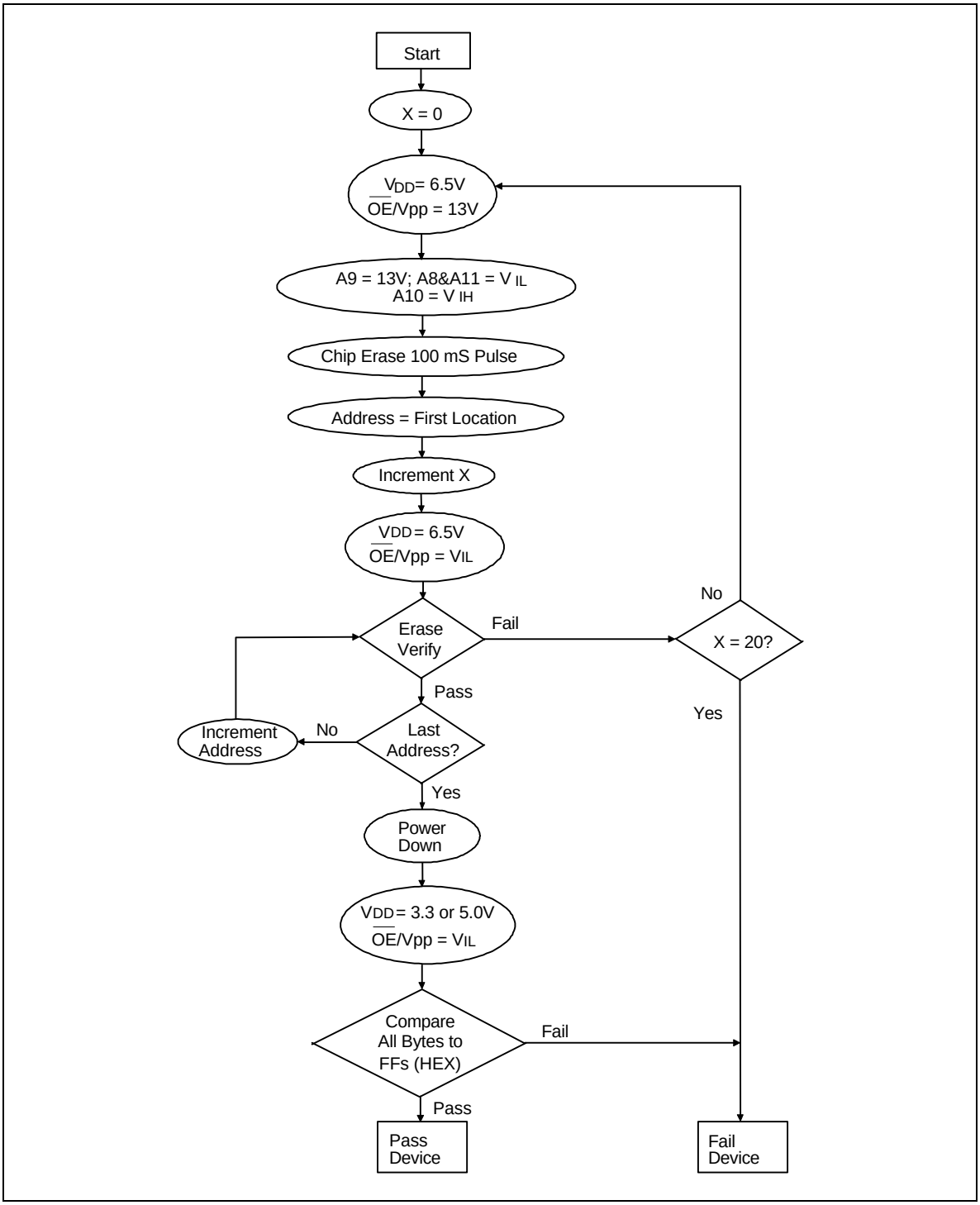
SMART PROGRAMMING ALGORITHM 1



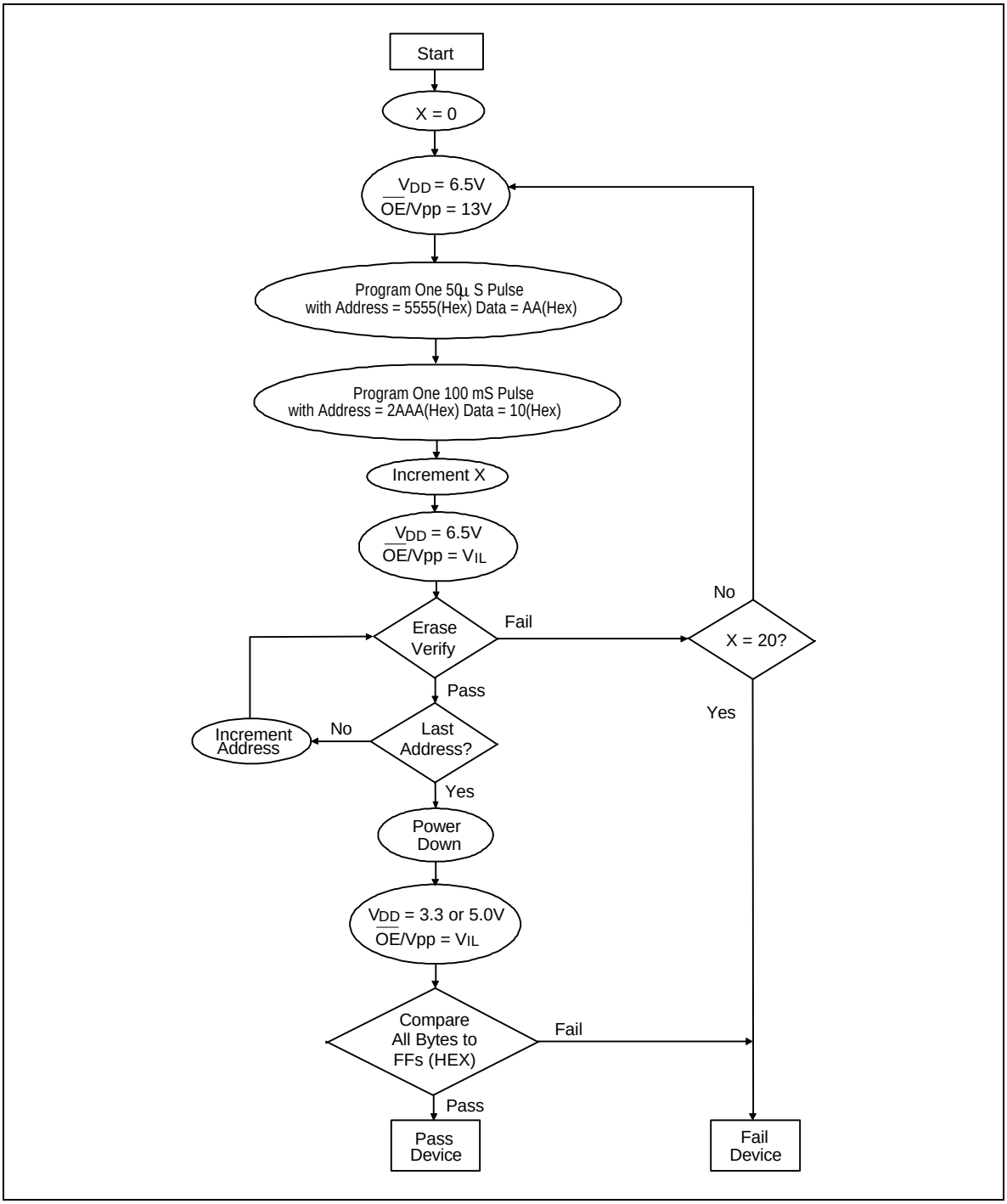
SMART PROGRAMMING ALGORITHM 2



SMART ERASE ALGORITHM 1



SMART ERASE ALGORITHM 2



ORDERING INFORMATION

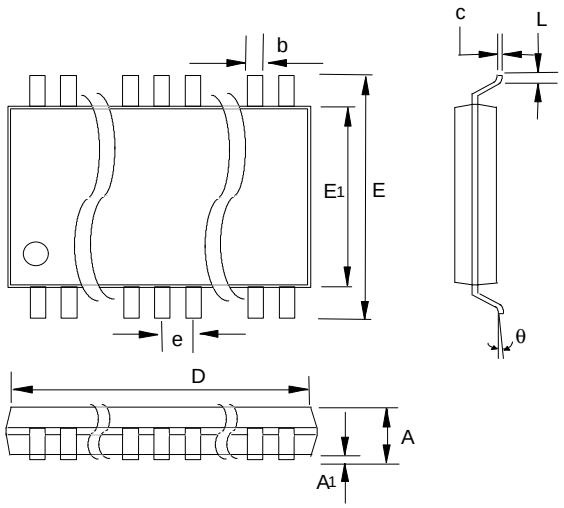
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (μA)	PACKAGE
W27LE520W-70*	70	8/20	20/100	173 mil TSSOP
W27LE520W-90*	90	8/20	20/100	173 mil TSSOP
W27LE520S-70*	70	8/20	20/100	300 mil SOP
W27LE520S-90*	90	8/20	20/100	300 mil SOP

Notes:

1. The Part No is preliminary and might be changed after project is consoled.
2. Winbond reserves the right to make changes to its products without prior notice.
3. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

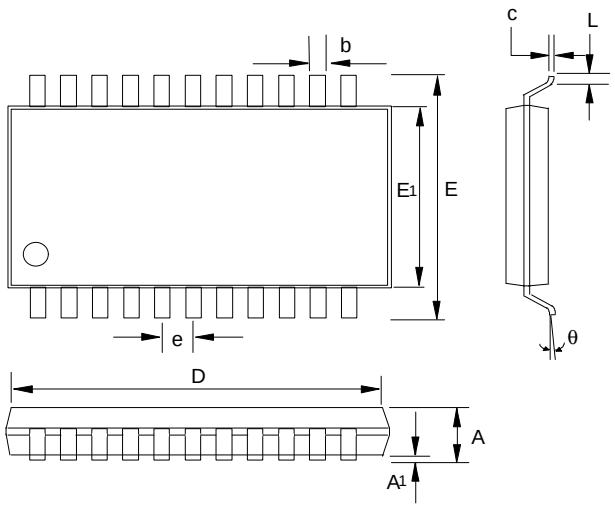
PACKAGE DIMENSIONS

20-pin TSSOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.043	—	—	1.10
A_1	0.002	—	0.006	0.05	—	0.15
L	0.020	—	0.028	0.50	—	0.70
D	0.252	—	0.260	6.40	—	6.60
E	0.246	—	0.256	6.25	—	6.50
E_1	0.169	—	0.176	4.30	—	4.48
b	0.007	—	0.012	0.18	—	0.30
c	0.003	—	0.007	0.09	—	0.18
e	0.65 BSC			0.256 BSC		
θ	0		8	0		8

20-pin SOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.092	—	0.105	2.34	—	2.67
A_1	0.003	—	0.012	0.076	—	0.305
L	0.015	—	0.035	0.381	—	0.889
D	0.497	—	0.513	12.6	—	13.0
E	0.393	—	0.420	9.98	—	10.7
E_1	0.291	—	0.299	7.39	—	7.60
b	0.013	—	0.020	0.330	—	0.508
c	0.009	—	0.013	0.229	—	0.330
e	0.50 BSC			1.27 BSC		
θ	0		8	0		8

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Jun. 2000	-	Initial Issued
A2	Sep. 2000	9	Correct Erase Waveform
		3	Modify Address Latch Enable Mode: X -> Ain; Modify Output Disable Mode: V_{IL} -> V_{IL}/V_{IH}; Modify Standby Mode: Ain -> X; Typo Correction

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