W232

Ten Output Zero Delay Buffer

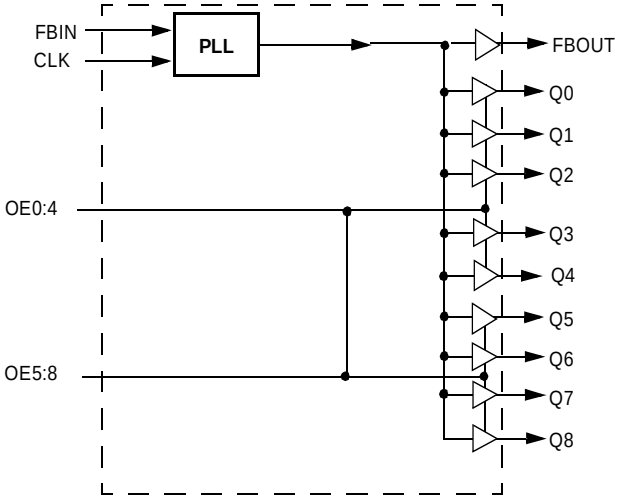
Features

- **Well suited to both 100- and 133-MHz designs**
- **Ten LVCMOS/LVTTL outputs**
- **3.3V power supply**
- **On-board 25Ω damping resistors**
- **Available in 24-pin TSSOP package**

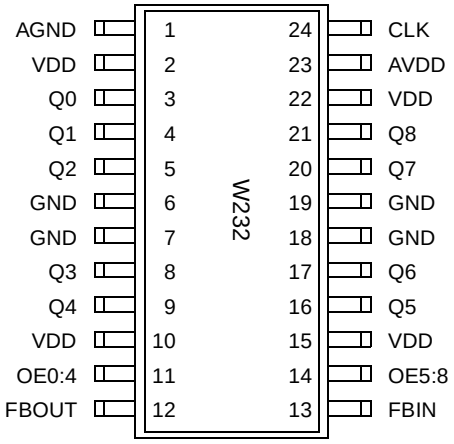
Key Specifications

Operating Voltage: .....3.3V±10%
Operating Range: .....25 MHz < f_{OUT} < 140 MHz
Cycle-to-Cycle Jitter: .....<150 ps
Output-to-Output Skew: .....<100 ps
Phase Error Jitter: .....<125 ps
Static Phase Error: .....<150 ps

Block Diagram



Pin Configurations



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Pin Definitions

Pin Name	Pin No. (-09B)	Pin Type	Pin Description
CLK	24	I	***Reference Input:*** Output signals Q0:9 will be synchronized to this signal.
FBIN	13	I	***Feedback Input:*** This input must be fed by one of the outputs (typically FBOUT) to ensure proper functionality. If the trace between FBIN and FBOUT is equal in length to the traces between the outputs and the signal destinations, then the signals received at the destinations will be synchronized to the CLK signal input.
Q0:8	3, 4, 5, 8, 9, 16, 17, 20, 21	O	***Integrated Series Resistor Outputs:*** The frequency and phase of the signals provided by these pins will be equal to the reference signal if properly laid out. Each output has a 25Ω series damping resistor integrated.
FBOUT	12	O	***Feedback Output:*** This output has a 25Ω series resistor integrated on chip. Typically it is connected directly to the FBIN input with a trace equal in length to the traces between outputs Q0:9 and the destination points of these output signals.
AVDD	23	P	***Analog Power Connection:*** Connect to 3.3V. Use ferrite beads to help reduce noise for optimal jitter performance.
AGND	1	G	***Analog Ground Connection:*** Connect to common system ground plane.
VDD	2, 10, 15, 22	P	***Power Connections:*** Connect to 3.3V. Use ferrite beads to help reduce noise for optimal jitter performance.
GND	6, 7, 18, 19	G	***Ground Connections:*** Connect to common system ground plane.
OE0:4	11	I	***Output Enable Input:*** Tie to V_{DD} (HIGH, 1) for normal operation. when brought to GND (LOW, 0) outputs Q0:4 are disabled to a LOW state.
OE5:8	14	I	***Output Enable Input:*** Tie to V_{DD} (HIGH, 1) for normal operation. when brought to GND (LOW, 0) outputs Q5:8 are disabled to a LOW state.

Overview

The W232 is a PLL-based clock driver designed for use in dual inline memory modules. The clock driver has output frequencies of up to 133 MHz and output-to-output skews of less than 100 ps. The W232 provides minimum cycle-to-cycle and long-term jitter, which is of significant importance to meet the tight input-to-input skew budget in DIMM applications.

The current generation of 256- and 512-megabyte memory modules needs to support 100-MHz clocking speeds. Especially for cards configured in 16x4 or 8x8 format, the clock signal provided from the motherboard is generally not strong enough to meet all the requirements of the memory and logic on the DIMM. The W232 takes in the signal from the motherboard and buffers out clock signals with enough drive to support all the DIMM board clocking needs. The W232 is also designed to meet the needs of new PC133 SDRAM designs, operating to 133 MHz.

The W232 was specifically designed to accept SSFTG signals currently being used in motherboard designs to reduce EMI. Zero delay buffers which are not designed to pass this feature through may cause skewing failures.

Output enable pins allow for shutdown of output when they are not being used. This reduces EMI and power consumption.

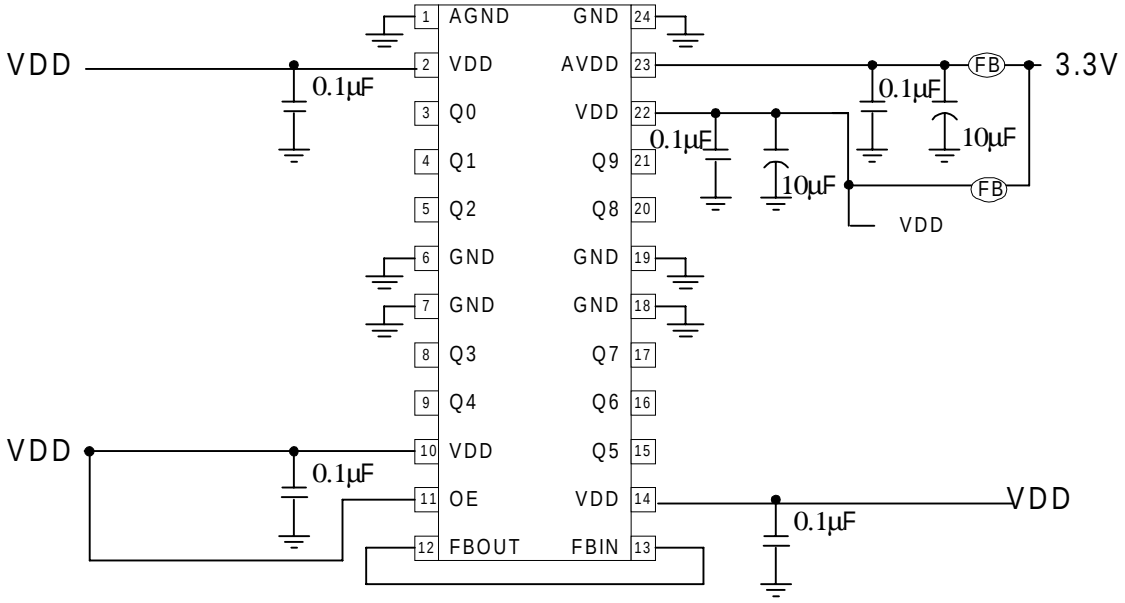


Figure 1. Schematic

Spread Aware™

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation. Cypress has been one of the pioneers of SSFTG development, and we designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the SS feature through, the result is a significant amount of tracking skew which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum timing technology, please see the Cypress application note titled, “EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator (SSFTG) ICs.”

How to Implement Zero Delay

Typically, zero delay buffers (ZDBs) are used because a designer wants to provide multiple copies of a clock signal in phase with each other. The whole concept behind ZDBs is that the signals at the destination chips are all going HIGH at the same time as the input to the ZDB. In order to achieve this, layout must compensate for trace length between the ZDB and the target devices. The method of compensation is described below.

External feedback is the trait that allows for this compensation. Since the PLL on the ZDB will cause the feedback signal to be in phase with the reference signal. When laying out the board, match the trace lengths between the output being used for feed back and the FBIN input to the PLL.

If it is desirable to either add a little delay, or slightly precede the input signal, this may also be affected by either making the trace to the FBIN pin a little shorter or a little longer than the traces to the devices being clocked.

Inserting Other Devices in Feedback Path

Another nice feature available due to the external feedback is the ability to synchronize signals up to the signal coming from some other device. This implementation can be applied to any device (ASIC, multiple output clock buffer/driver, etc.) which is put into the feedback path.

Referring to *Figure 2*, if the traces between the ASIC/buffer and the destination of the clock signal(s) (A) are equal in length to the trace between the buffer and the FBIN pin, the signals at the destination(s) device will be driven high at the same time the Reference clock provided to the ZDB goes high. Synchronizing the other outputs of the ZDB to the outputs form the ASIC/Buffer is more complex however, as any propagation delay in the ASIC/Buffer must be accounted for.

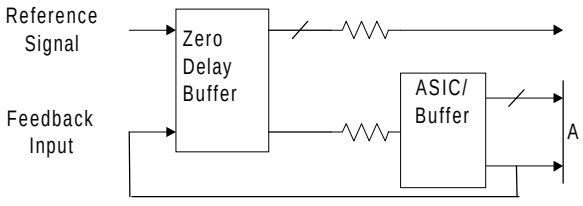


Figure 2. 6 Output Buffer in the Feedback Path

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
P_D	Power Dissipation	0.5	W

DC Electrical Characteristics: T_A =0°C to 70°C, V_{DD} = 3.3V ±10%

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{DD}	Supply Current	Unloaded, 100 MHz			200	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA			0.8	V
V_{OH}	Output High Voltage	I_{OH} = –12 mA	2.1			V
I_{IL}	Input Low Current	V_{IN} = 0V			50	µA
I_{IH}	Input High Current	V_{IN} = V_{DD}			50	µA

AC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V ±10%

Parameter	Description	Test Condition	Min	Typ	Max	Unit
fOUT	Output Frequency	30-pF load[1]	25		140	MHz
tR	Output Rise Time	0.8V to 2.0V, 30-pF load			2.1	ns
tF	Output Fall Time	2.0V to 0.8V, 30-pF load			2.5	ns
tICLKR	Input Clock Rise Time[2]				4.5	ns
tICLKF	Input Clock Fall Time[2]				4.5	ns
tPEJ	CLK to FBIN Skew Variation[3, 4]	Measured at VDD/2	–350	0	350	ps
tSK	Output to Output Skew	All outputs loaded equally	–100	0	100	ps
tD	Duty Cycle	30-pF load	43	50	58	%
tLOCK	PLL Lock Time	Power supply stable			1.0	ms
tJC	Jitter, Cycle-to-Cycle[5]				150	ps

Notes:

1. Production tests are run at 133 MHz.
2. Longer input rise and fall time will degrade skew and jitter performance.
3. Skew is measured at VDD/2 on rising edges.
4. Duty cycle is measured at VDD/2.
5. For frequencies below 40 MHz, Cycle to Cycle Jitter degrades to 175 ps.

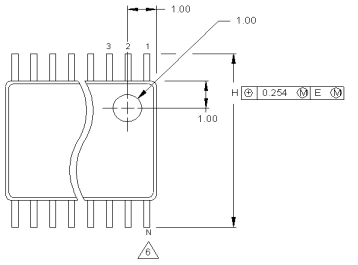
Ordering Information

Ordering Code	Package Type
W232	24-pin TSSOP

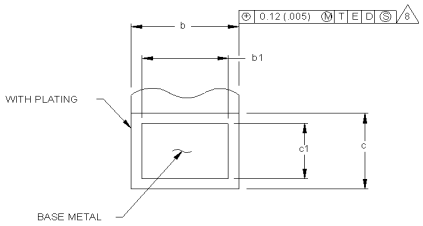
Document #: 38-00827

Package Diagram

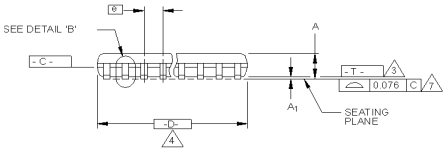
24-Pin Thin Shrink Small Outline Package (TSSOP)



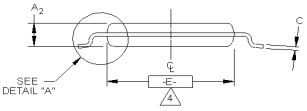
TOP VIEW



DETAIL "C"
SCALE: 120/1
(SEE NOTE 9)

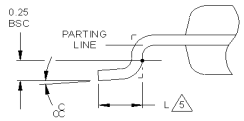


SIDE VIEW

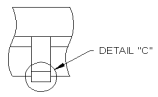


END VIEW

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.279±0.0127 (.0110±.0005 INCHES)
2. DIMENSIONING & TOLERANCES PER ANSI Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE.
8. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.14mm. SEE DETAILS 'B' AND 'C'.
9. DETAIL "C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
10. CONTROLLING DIMENSION: MILLIMETERS.
11. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153. VARIATIONS AA, AB, AC, AD AND AE.



DETAIL 'A'
(SCALE: 30/1)



DETAIL "B"
(SCALE: 30/1)
DAMBAR PROTRUSION

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A			1.10		AA	2.90	3.00	3.10	8
A_1	0.05	0.10	0.15		AB	4.90	5.00	5.10	14
A_2	0.85	0.90	0.95		AC	4.90	5.00	5.10	16
b	0.19	-	0.30	8	AD	6.40	6.50	6.60	20
b1	0.19	0.22	0.25		AE	7.70	7.80	7.90	24
c	0.090	-	0.20		AF	9.60	9.70	9.80	28
c1	0.090	0.127	0.135						
D	SEE VARIATIONS			4					
E	4.30	4.40	4.50	4					
e	0.65 BSC								
H	6.25	6.40	6.50						
L	0.50	0.60	0.70	5					
N	SEE VARIATIONS			6					
cc	0°	4°	8°						

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A			.0433		AA	.114	.118	.122	8
A_1	.002	.004	.006		AB	.193	.197	.201	14
A_2	.0335	.0354	.0374		AC	.193	.197	.201	16
b	.0075	-	.0118	8	AD	.252	.256	.260	20
b1	.0075	.0087	.0098		AE	.303	.307	.311	24
c	.0035	-	.0079		AF	.378	.382	.386	28
c1	.0035	.0050	.0053						
D	SEE VARIATIONS			4					
E	.169	.173	.177	4					
e	.0256 BSC								
H	.246	.252	.256						
L	.020	.024	.028	5					
N	SEE VARIATIONS			6					
cc	0°	4°	8°						

VARIATION AF IS DESIGNED BUT NOT TOOLED