Texas Instruments

TLC2543 Evaluation Module

User's Guide

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Mixed-Signal Products

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Preface

Read This First

About This Manual

This user's guide provides descriptive information about the hardware and software comprising the TLC2543 evaluation module (EVM). The evaluation module includes a TLC2543 12-bit analog-to-digital converter (ADC) and can be used to assist managers and hardware and software engineers in developing 12-bit ADC applications.

How to Use This Manual

This document contains the following chapters:

Chapter 1 **Overview**

Provides a general description of the TLC2543 EVM

Chapter 2 **Hardware Description and Operation**

Describes the features of the TLC2543 EVM hardware and provides operating specifications, schematic diagram, connections, layout, and parts

Chapter 3 **Board Layout**

Contains illustrations of the board layout and layers

Chapter 4 **Part Descriptions**

Lists and describes the TLC2543 EVM parts.

Chapter 5 **Software Program and Flow Charts**

Describes the TLC2543 EVM software program and program flowcharts

Notational Conventions

This document uses the following conventions.

- Program listings, program examples, and interactive displays are shown in a `special typeface` similar to a typewriter's. Examples use a **`bold version`** of the special typeface for emphasis; interactive displays use a **`bold version`** of the special typeface to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

  Here is a sample program listing:

  ```
  0011  0005  0001         .field    1, 2
  0012  0005  0003         .field    3, 4
  0013  0005  0006         .field    6, 3
  0014  0006               .even
  ```

  Here is an example of a system prompt and a command that you might enter:

  ```
  C:  csr –a /user/ti/simuboard/utilities
  ```

- In syntax descriptions, the instruction, command, or directive is in a **bold typeface** font and parameters are in an *italic typeface*. Portions of a syntax that are in **bold** should be entered as shown; portions of a syntax that are in *italics* describe the type of information that should be entered. Here is an example of a directive syntax:

  .asect **"***section name***",** *address*

  .asect is the directive. This directive has two parameters, indicated by *section name* and *address*. When you use .asect, the first parameter must be an actual section name, enclosed in double quotes; the second parameter must be an address.

- Square brackets (**[** and **]**) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets; you don't enter the brackets themselves. Here's an example of an instruction that has an optional parameter:

  LALK *16–bit constant [, shift]*

  The LALK instruction has two parameters. The first parameter, *16-bit constant*, is required. The second parameter, *shift*, is optional. As this syntax shows, if you use the optional second parameter, you must precede it with a comma.

  Square brackets are also used as part of the pathname specification for VMS pathnames; in this case, the brackets are actually part of the pathname (they are not optional).

- Braces ({ and }) indicate a list. The symbol **|** (read as *or*) separates items within the list. Here's an example of a list:

  `{ * | *+ | *– }`

  This provides three choices: `*`, `*+`, or `*–`.

Unless the list is enclosed in square brackets, you must choose one item from the list.

- Some directives can have a varying number of parameters. For example, the .byte directive can have up to 100 parameters. The syntax for this directive is:

  .byte *value*$_1$ *[, ... , value*$_n$*]*

  This syntax shows that .byte must have at least one value parameter, but you have the option of supplying additional value parameters, separated by commas.

Information About Cautions and Warnings

This book may contain cautions and warnings.

CAUTION

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

WARNING

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

TLC2543C, TLC2543I 12-Bit Analog-to-Digital Converters With Serial Control and 11 Analog Inputs data sheet (literature number SLAS079C) is included in Appendix A of this book. It contains electrical specifications, available temperature options, general overview of the device, and application information.

Microcontroller-Based Data Acquisition Using the TLC2543 12-Bit Serial-Out ADC Application Report (literature number SLAA012)

Data Acquisition Circuits Data Book (literature number SLAD001)

TSL250, TSL251, TSL252 Light-to-Voltage Optical Sensors data sheet (literature number SOES004C)

TLC226x, TLC226xA, TCL226xY Advanced LinCMOS Rail-to-Rail Operational Amplifiers data sheet (literature number SLOS177)

TL7726C, TL7726I, TL7726Q Hex Clamping Circuits data sheet (literature number SLAS078B)

TL7702B, TL7702Y, TL7705B, TL7705Y Supply Voltage Supervisors data sheet (literature number SLVS037E)

CDT Addendum to the TMS370 Family C Source Debugger User's Guide (literature number SPRU133)

TMS370 Family EPROM/EEPROM Programming Tool Getting Started Guide (literature number SPNU128)

CDT370 Addendum to the TMS370 Family C Source Debugger User's Guide (literature number DB197A)

TL1431C, TL1431Q, TL1431Y Precision Programmable References (literature number SLVS062B)

TIL311 Hexadecimal Display With Logic (literature number SODS001D)

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules. This device has been tested and found to comply with the limits for a CISPRII Group 1 and the following directives: EMC Directive 89/336/ECC amending directive 92/31/ECC and 93/68/ECC as per ENV50204: 1995, EN55011: 1995 Class A, EN61000-4-4: 1995, and EN61000-4-3:1994. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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Chapter 1

Overview

The TLC2543 evaluation module (EVM) provides a platform for evaluating the TLC2543 analog-to-digital converter (ADC). For ease of evaluation, the EVM provides for TLC2543 ADC evaluations using an optical sensor, temperature sensor, and variable voltage as inputs. Provisions are available for the user to configure the additional EVM inputs and the system configuration to accommodate other evaluations.

This section includes the following topics.

Topic **Page**

1.1 Introduction

The TLC2543 evaluation module (TLC2543EVM) consists of a TLC2543 12-bit ADC interface with a TSL250 optical sensor, a transistor-based temperature sensor, a TL1431 voltage reference, a TLC2264 quad op-amp to provide four analog signal buffers, a TL7726 hex clamping circuit for signal over-voltage protection, a TMS370C712 microcontroller, and three TIL311 hex display characters.

The microcontroller reads the user programmed dip switches and communicates with the TLC2543 to select the desired analog input, initiate the conversion process, and transfer the converted data back to the microcontroller. The microcontroller then transforms the data into hex form and transfers the result to the three TIL311 displays. A 74HC244 octal buffer is used as a buffer between the microcontroller and the displays.

A TL7705 power supply voltage monitor provides the reset for the processor at power-on or if the power supply voltage drops below the proper operating level.

Jumper provisions are made to connect the TLC2543 reference voltage to 5-V power for ratiometric measurements or to an absolute voltage provided by a TL1431 voltage reference device.

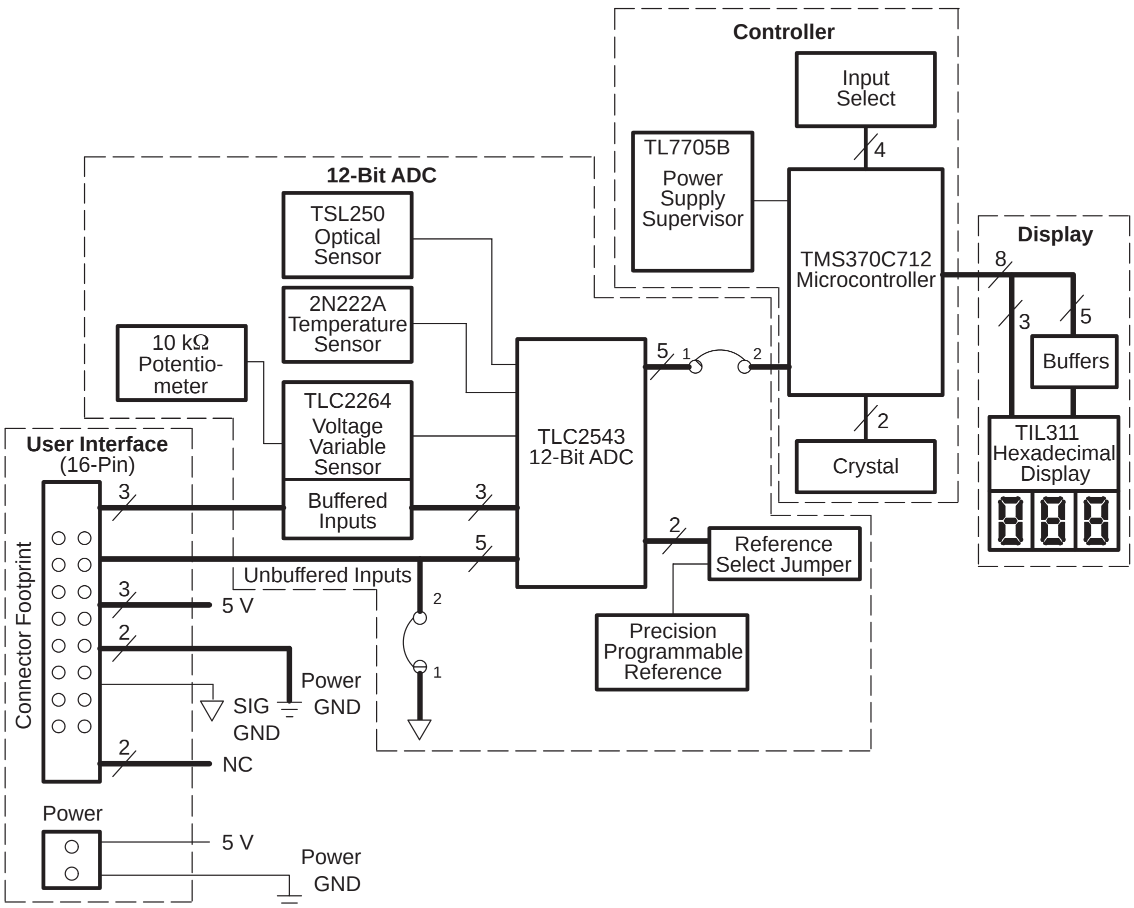
A connector pattern provides for a user installed interface connector and an uncommitted breadboard area. An external 5-V power supply (4.75 V to 5.25 V at 0.5 A) is required for operation.

The TL7726 hex clamping circuit (VZ1) is connected to inputs IN3 through IN8. The TL7726 clamps an input signal voltage in excess of the power supply voltage level to prevent damage to the semiconductor inputs. Signal voltages below 0 V (ground) are clamped to ground. Signal inputs between 5 V and ground are not affected. The TL7726 provides protection for inputs from incidental transients due to static discharge, excessive signals, etc. Transient current protection is limited to 25 mA.

1.2 Description

This section describes the EVM. A block diagram of the EVM is shown in Figure 1–1.

Figure 1–1. Evaluation Module Block Diagram



The EVM consists of the following:

- 12-bit analog-to-digital converter with:
  - Dedicated optical, temperature, and voltage variable inputs
  - Eight user-configurable inputs
  - User-selectable output for ratiometric or absolute voltage measurements
- Controller with input select and power supply supervisor
- Three-digit hexadecimal display
- User-configurable interface

The EVM functions are described in the following sections.

1.2.1 12-Bit Analog-to-Digital Converter

The TLC2543 is a 12-bit, switched-capacitor, successive-approximation ADC. The device has three control inputs, a chip select, an input-output clock, and a serial data in address input that are interconnected to the microcontroller.

The TLC2543 has an on-chip 14-channel multiplexer that can select any one of 11 inputs or any one of three internal self-test voltages. At the end of conversion, the end-of-conversion (EOC) output goes high indicating to the microcontroller that the conversion is complete.

The microcontroller supplies the serial data address to, and reads the serial digital data from, the TLC2543 ADC.

1.2.1.1 Outputs

At the ADC REF+ and REF– inputs, jumper provisions are made to connect the TLC2543 ADC reference voltage to the 5-V power source that produces ratiometric measurements, or measurements can be made with respect to an absolute voltage provided by a TL1431 voltage reference device.

1.2.1.2 Inputs

The 11 EVM inputs are configured to provide access to the ADC for the following types of conversions:

- Three dedicated inputs that include:
  - An optical sensor
  - A temperature sensor
  - A variable resistor
- Eight additional user-configurable analog inputs:
  - Three buffered inputs by using the TLC2264 operational amplifiers.
  - Five inputs are unbuffered and grounded.

Provisions are made for attaching the eight additional signal lines to the user-supplied interface connector.

1.2.2 Controller

The controller consists of the following:

- The TMS370C712 microcontroller and crystal
- The TL7705B power supply voltage monitor
- The input select switches

1.2.2.1 Microcontroller and Crystal

The microcontroller reads the user-programmed DIP switches and communicates with the TLC2543 to select the desired analog input, initiates the conversion process, and transfers the converted data back to the microcontroller. The microcontroller then transforms the data into hex form and transfers the result to the display.

The crystal generates the clock input for the microcontroller. The microcontroller supplies the TLC2543 ADC clock and the TIL311 display strobes.

1.2.2.2 Power Supply Voltage Monitor

The TL7705B power supply voltage monitor provides a reset for the processor at power-on or when the power supply voltage drops below the proper operating level.

1.2.3 User Interface

Provisions are available for the user to configure the additional EVM inputs and the system configuration to accommodate other evaluations. A connector pattern is provided for the user to install a 16-pin interface connector. A breadboard area is also available on the EVM. The following input and power/ground options are available at the connector interface:

- ❑ Three buffered ADC inputs
- ❑ Five unbuffered ADC inputs
- ❑ Three EVM 5-V power connections
- ❑ Two EVM power ground connections
- ❑ One EVM signal ground connection

Terminals for an external 5-V power supply are provided. An external 5-V power supply (4.75 V to 5.25 V at 0.5 A) is required for operation.

1.2.4 Display

The microcontroller decodes the 12-bit ADC data into hexadecimal three-digit values which activate the three hexadecimal displays.

Buffers are used between the microcontroller and the display data input ports and blanking inputs. The three display latch strobes are driven directly from the microcontroller I/O port.

Chapter 2

Hardware Description and Operation

This chapter contains descriptions of the hardware and operation of the TLC2543EVM. This chapter includes the following topics:

Topic **Page**

2.1 Setup and Operation

Figure 2–1, a schematic diagram of the EVM, identifies the EVM components and the setup and operating procedures.

Figure 2–1. EVM Board Schematic

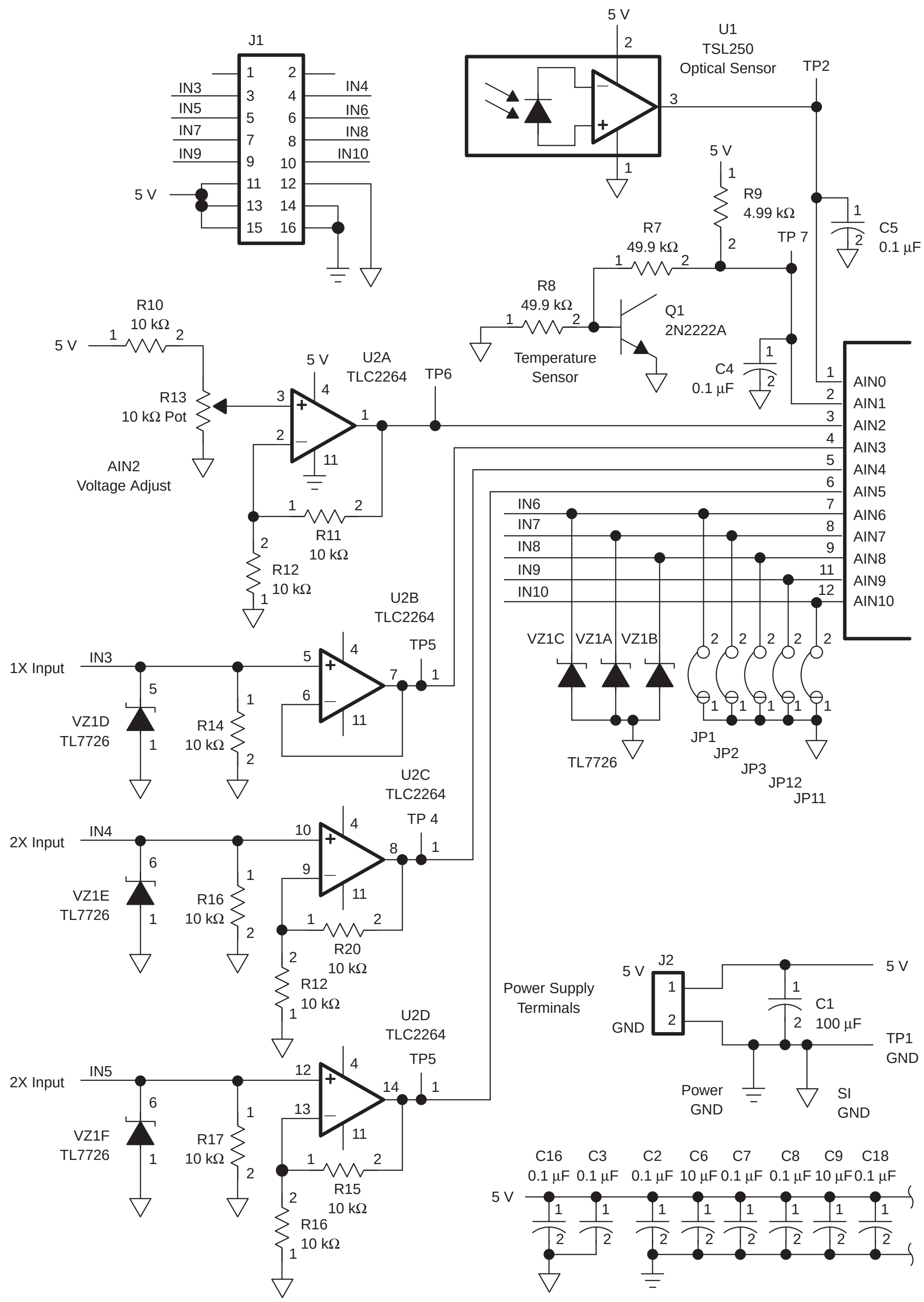
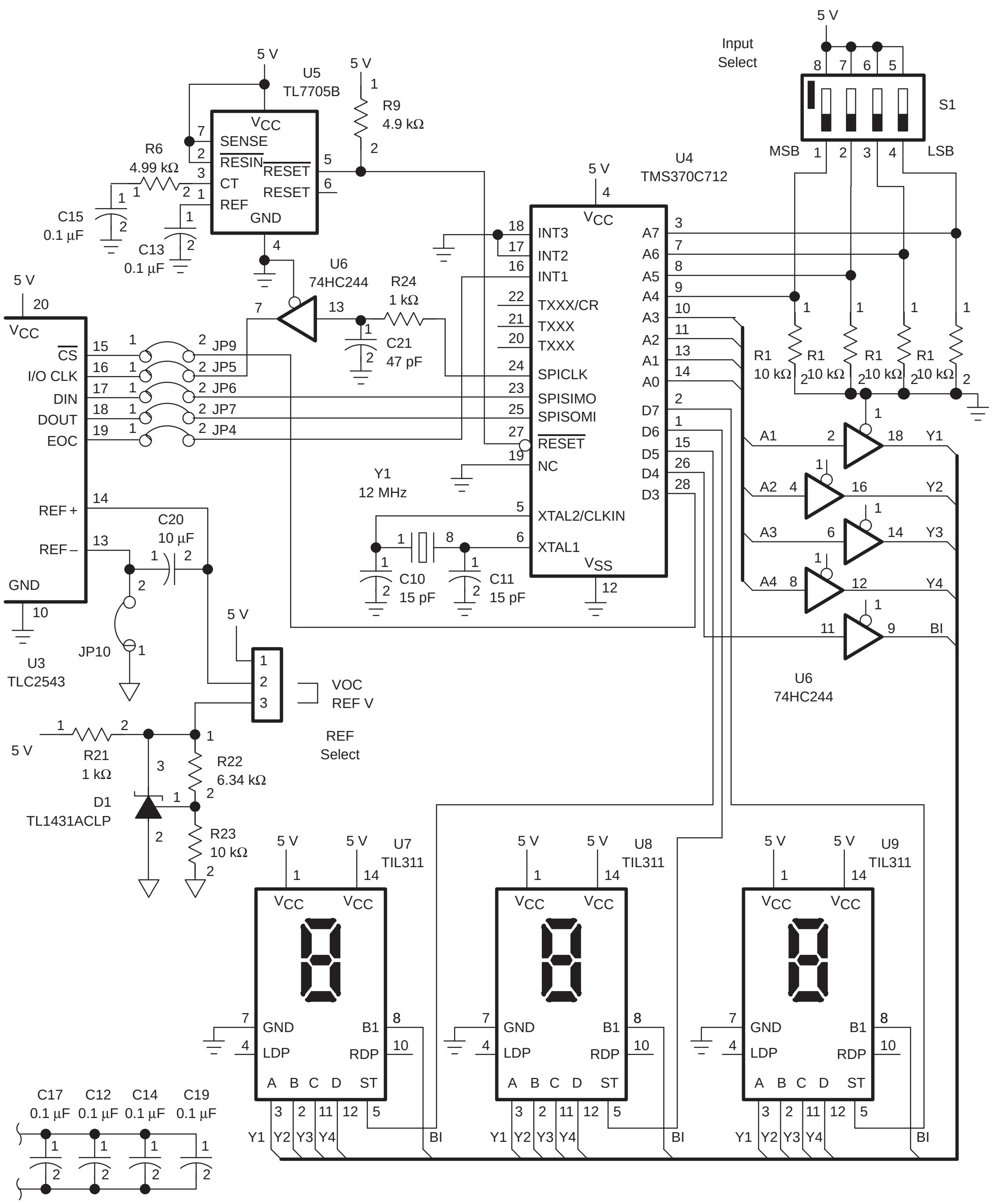


Figure 2–1. EVM Board Schematic (Continued)



2.1.1 Power Supply Terminals

The power supply terminals (J2) on the EVM, see Figure 2–1, should be connected to a regulated 4.75-V to 5.25-V power supply capable of providing at least 0.5 A.

CAUTION

This evaluation module is designed to have power supplied from an external regulated 5-V power supply. No form of power supply regulation is included on the EVM. Damage to the components can and probably will occur if the voltage exceeds the maximum specified level. Under voltage can cause improper operation.

When the power supply is switched on, the microcontroller is initialized and the displays flash to indicate proper operation. The displays then show the 2- or 3- digit hex value of the voltage generated by the TSL250 optical sensor. The value on the displays varies with the intensity of the light striking the TSL250 sensor (see section 2.3.1, *Optical Sensor*).

2.1.2 Input/Output Select Switches

The INPUT SELECT switch (S1) sets the binary address (LSB on the right) which selects the desired TLC2543 input (see subsection 2.1.3, *Input Select Switch*).

The EVM is shipped with the settings listed in Table 2–1:

Table 2–1. EVM Default Settings

Function	Setting
Input select switch (S1)	0000 hex (optical sensor selected)
Reference select jumper (JP9)	REF V
Input jumpers (JP1, JP2, JP3, JP11, JP12)	Ground
Output jumpers (JP4, JP5, JP6, JP7, JP8)	Shorted
REF– jumper (JP10)	Shorted

Note:

The input and output jumpers and the REF– jumper on the EVM are formed by a top-side copper trace on the PCB between two plated through-holes. If desired, the trace can be carefully cut to remove the jumper. The two-through-holes allow the user to restore the jumper with a wire or connector.

2.1.3 Input Select Switch

The four-position DIP switch (S1) labeled INPUT SELECT allows the user to select the desired analog input of the TLC2543 ADC. The software program then uses the onboard SPI interface to communicate with the TLC2543 and make the hexadecimal conversions.

2.1.3.1 Binary-to-Hexadecimal Conversion

The bits are read into the processor and output on the three LED displays approximately every 0.5 second. The switch is treated as a hex address command (MSB on left, LSB on right) as listed in Table 2–2:

Table 2–2. Input Select Switch Descriptions

Hex	Binary	Function Selected	Typical Response
0h	0000	Optical sensor input	User-controlled light intensity
1h	0001	Temperature sensor input	588h + temperature change
2h	0010	Potentiometer input	User adjusted
3h	0011	IN3 buffer input	000h or user input
4h	0100	IN4 buffer input	000h or user input
5h	0101	IN5 buffer input	000h or user input
6h–Ah	0110–1010	IN6 through IN10 inputs	000h or user input
Bh	1011	(V_{ref} input)/2 test	800h
Ch	1100	–V_{ref} input (ground) test	000h
Dh	1101	V_{ref} input test	FFFh
Eh	1110	Enter power-down mode	Display blank
Fh	1111	Fast conversion rate on IN4 input	User input

Note: Inputs IN3 through IN10 are made available to a user-supplied connector (see section 2.1.4, *Interface Connector Provisions*).

2.1.3.2 Fast Conversion Rate

When the INPUT SELECT switch is set to Fh, the EVM operates in a fast conversion rate mode. In this mode, the conversion rate is approximately 30k conversions per second from the IN4 input. The displays are updated once every 20 conversions.

2.1.4 Interface Connector Provisions

A PCB footprint is provided for a user-supplied connector to allow easy application of external analog signals. The hole pattern interface connector provided at J1, see Figure 2–2, accepts a standard 8-by-2 set of header posts (such as an AMP 87215–5 or MOLEX 10–89–1161) that can be soldered in place. This arrangement accommodates several different styles of connectors so the user can select the one that best satisfies the system requirements.

Figure 2–2. Interface Connector Hole Pattern

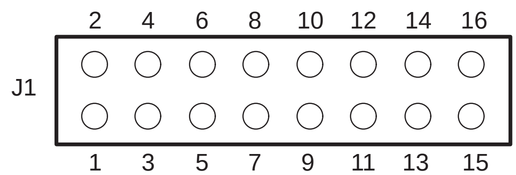


Table 2–3 describes the hole-pattern mapping to circuit functions.

Table 2–3. Interface Connector Hole Pattern Descriptions

Hole	Circuit Function
1	NC
2	NC
3	IN3 input (buffered with $1\times$ gain)
4	IN4 input (buffered with $2\times$ gain)
5	IN5 input (buffered with $2\times$ gain)
6	IN6 input
7	IN7 input
8	IN8 input
9	IN9 input
10	IN10 input
11	5 V
12	Signal ground (see Note)
13	5 V
14	Power ground
15	5 V
16	Power ground

Note: Hole 12 can be used as a signal ground return to avoid the higher current ground return paths that are associated with a power supply ground.

2.2 Microcontroller and Interface

This section provides an overview and describes the operation of the microcontroller and interface function.

2.2.1 Overview

The TLC2543EVM uses a TI TMS370C712 microcontroller to interface with the TLC2543 ADC. The program reads the four-position INPUT SELECT DIP switch to determine which input is selected to be digitized. The program then uses the serial peripheral interface (SPI) to communicate with the TLC2543. Sixteen bits of data (12 significant bits and 4 fill bits) are read into the processor and output on the three LED displays approximately every 0.5 second.

A fast mode can also be selected with the INPUT SELECT switch. In this mode, channel four is selected as input and 20 samples are taken at about a 30-kHz rate, data is converted and displayed, and the process is repeated until another input is selected with the switch. A power-down mode, which places the TLC2543 in a power-down mode and blanks the display, can also be selected.

2.2.2 Operation

The TMS370C712 microcontroller (U4) samples the status of the INPUT SELECT switch on ports A4–A7. This sample data, which is sent to the TLC2543 ADC through the SPI ports (SPICLK, SPISIM0, and SPISOMI) determines the specific multiplexer input that is converted. The microcontroller then reads back the converted 12 bits and decodes the data into hexadecimal three-digit values. The hexadecimal data is transferred to the three hexaecimal displays, U7, U8, and U9. Five sections of the 74HC244 octal buffer are used to drive the common-bused TTL inputs of the displays.

For all INPUT SELECT positions except Fh, the microcontroller instructs the TLC2543 ADC to perform the analog-to-digital conversions and display the results at a rate of approximately 2 conversions per second. When the INPUT SELECT position is Fh, the microcontroller selects input IN4 and the conversions from the ADC are at a rate of approximately 30-k conversions per second (see section 2.1.3.2, *Fast Conversion Rate*).

Notes:

The following information applies to the TMS370C712 SPI protocol to the TLC2543.

The TLC2543 strobes in the command data bits from the microcontroller on the DIN port at the rising edge of the clock pulse on the I/O CLK terminal. The TMS370C712 generates a clock rising edge on the SPICLK port, and at that time while conforming to the SPI interface requirements, the data output on the SPISIM0 port changes to reflect the next serial bit to be transferred.

Notes: Continued

Therefore, if the SPICLK output is connected directly to the TLC2543 ADC I/O CLK input, the required data setup time for the data to be present before a rising clock edge is applied cannot be less than 100 ns (see the TLC2543 data sheet). To solve this race condition, a resistor (R24) and capacitor (C21) are provided to delay the rising clock edge. One buffer section of the 74HC244 octal buffer (U6) is used to buffer the delayed clock signal. If only one TLC2543 ADC is being used (as with this EVM), the buffer is not usually required. However, if several TLC2543 devices are being driven in a bus configuration, this buffer is required to provide a proper clock signal into the additional capacitance.

2.2.3 Power Supply Supervisor

The TL7705 power supply supervisor, U5, (see Figure 2–1) monitors the power supply voltage. When power is first applied, a microprocessor reset is held until the power supply voltage exceeds 4.55 V (nominal). The reset is then released and the microprocessor begins operation.

If the power supply voltage falls below 4.55 V during normal operation, a reset is activated.

2.3 Sensor Inputs

The EVM inputs are configured to provide access to the ADC as outlined in Section 1.2.1.2. These inputs are discussed in more detail below.

2.3.1 Optical Sensor

The TSL250 (U1) optical sensor is connected to the AIN0 multiplexer analog input port of the TLC2543 ADC. This sensor converts light intensity to an output voltage ranging from less than 10 mV (dark) to about 3.5 V (at 2 mW/sq cm illumination intensity).

The output of the optical sensor can be varied by placing an object such as a dark-colored plastic marker pen cap over the sensor.

A practical application such as sorting can be demonstrated by holding similar objects of differing shades within the optical viewing range of the sensor (under a uniform intensity light) and noting the displayed values. A simple optical hood to mask ambient light (e.g., drill a hole in the side of the marker pen cap) provides more uniform results.

Note:

Office light generated by typical artificial lighting contains high ac line frequency intensity variations not usually perceived by the human eye. These variations are detected by the optical sensor. Since the ADC is commanded to make measurements at random times with respect to the ac line frequency, the converted values appear to be unstable in the lower order bits, even though each individual measurement is accurate. This line frequency light intensity variation can be minimized by using dc power to drive the dominate light source (light-emitting diodes work well) in addition to shielding the sensor from the ac-driven room lighting.

An extension of the sorting concept yields a simple color-sorting sensor system. This system requires three optical sensors, each masked by a red, blue, or green optical filter. The individual readings from the three sensors can then be calibrated to the specific color of the object to be identified. For repeatable results, the intensity and color content of the illuminating light source must be uniform.

2.3.2 Temperature Sensor

When a single transistor and the 12-bit A/D conversion range of the TLC2543 ADC are used, the following occurs:

- A simple temperature sensor is generated
- The textbook temperature variation of a transistor base-emitter junction
- The dc temperature instability of a simple 1-transistor amplifier

The 2N2222A transistor (Q1) is connected in a classic feedback amplifier configuration that forces the collector voltage to a base-emitter junction voltage of 2 V_{be}. The base-emitter junction (essentially a forward-biased diode) voltage is about 0.7 V at room temperature (25 °C) and has a temperature variation of about –2.2 mV/°C. Therefore, at room temperature the collector voltage is approximately 1.4 V with a decrease of approximately 4.4 mV for each degree of temperature increase.

If the REF SELECT jumper is set to the onboard reference (REF V) position, the conversion reference is set to approximately 4096 mV or 4.1 V. This setting allows the display to decrement approximately 1 count for each mV or about 4 counts per °C of temperature increase.

If the ambient room temperature is approximately 25°C and human body temperature is approximately 38°C, the display should reduce about 52 counts when the transistor is held firmly between two fingers. (For an exact analysis, exact transistor characteristics, absolute reference voltage levels, and exact room and finger temperatures would have to be taken into account.)

2.3.3 Voltage Variable Input (Potentiometer)

The IN2 input is controlled by a potentiometer (R13). One section of the TLC2264 (U2) serves as a buffer/amplifier for the AIN2 TLC2543 input port. When the potentiometer is adjusted over its range, the input voltage changes from 0 V to V_{CC}/2. Since the buffer/amplifier has a gain of 2, the input to the TLC2543 ADC port varies from 0 V to V_{CC}.

For ratiometric measurements, the REF SELECT jumper should be set to the V_{CC} position. Then the TLC2543 ADC reference becomes V_{CC} and all A/D conversions are made relative to the value of V_{CC}. The potentiometer output voltage, due to its connection, is also relative to V_{CC}. An A/D conversion of that voltage yields a value proportional to the setting of the potentiometer and independent of the power supply voltage.

2.3.4 Buffered User Inputs

The IN3 input is connected to the TLC2543 input port through unity gain configured buffer/amplifier (one section of the TLC2264, U2). Although providing unity gain (gain = 1), the input signal can only be within approximately 1.5 V (see the common-mode input-voltage range specifications of the TLC2264 ADC) of the power supply voltage to maintain predictable operation. As long as the power supply voltage to the TLC2264 remains at 5 V, this restricts the usable signal input voltage range from 0 V to 3.5 V; however, this range can be acceptable for some input level requirements.

The input impedance is dictated by the 10-kΩ value of resistor R14 and can be changed to almost any suitable value due to the extremely high input impedance of the TLC2264.

Inputs IN4 and IN5 are connected to the TLC2543 ADC input ports, each through a buffer stage of the TLC2264, and each with a gain of 2. The full output voltage swing of 0 V to 5 V to the ADC inputs is achieved with signal inputs of 0 V to 2.5 V as listed in 2–4.

Table 2–4. Buffered User Input Descriptions

Input	Gain	Unbuffered	Input Range
IN3	×1	N	0 V – 3.5 V (input to ADC is 3.5/5 of full scale)
IN4	×2	N	0 V – 2.5 V
IN5	×2	N	0 V – 2.5 V
IN6		Y	0 V – 5 V
IN7		Y	0 V – 5 V
IN8		Y	0 V – 5 V
IN9		Y	0 V – 5 V
IN10		Y	0 V – 5 V

2.3.5 Unbuffered Inputs

The IN6–IN10 inputs are connected to ground by the top-side circuit board etch jumpers, JP1, JP2, JP3, JP12, and JP11, respectively. Any etch jumper can be removed by carefully cutting the copper trace between the feed-through holes at the JP marking, allowing that input to be connected to an external signal.

When these unbuffered inputs are used, the TLC2543 ADC requires a low source impedance (see Section 2.7, *Driving the Input of a Switched-Capacitor ADC*) and input voltage range of 0 V to 5 V to produce a zero-to-full-scale digital output. Ensure that the signal grounds are not improperly connected to the high-current power supply grounds (see Section 2.5, *Grounding Considerations*).

2.3.6 Input Voltage Clamp

The TL7726 hex clamping circuit (VZ1) is connected to inputs IN3 through IN8. The TL7726 clamps an input signal voltage in excess of the power supply voltage level to prevent damage to the semiconductor inputs. Signal voltages below 0 V (ground) are clamped to ground. Signal inputs between 5 V and ground are not affected. The TL7726 provides protection for inputs from incidental transients due to static discharge, excessive signals, etc. Transient current protection is limited to 25 mA.

2.4 Input Reference Voltage Select

The REF SELECT jumper allows ratiometric measurements (jumper set to V_{CC}) or allows absolute measurements (jumper set to REF V) relative to a voltage reference established by the TL1431 (D1). This voltage reference is programmed by resistors R22 and R23 to a voltage level of approximately 4.1 V.

2.4.1 Ratiometric Measurements

Ratiometric measurements are measurements made relative to the 5-V power supply voltage. If a sensor or input signal voltage is used that varies proportionally to the 5-V power supply voltage (such as the potentiometer R13), then the signal becomes a ratio of the absolute value of the power supply voltage. Therefore, when the reference voltage is connected to 5 V (REF SELECT jumper position at V_{CC}), the TLC2543 tracks the power supply voltage and provides a converted result independent of the power supply voltage variations.

2.4.2 Absolute Measurements

Absolute measurements are required when the input analog signal does not change with the power supply voltage. The optical and temperature sensors are in this category. For these sensors, the REF SELECT jumper is set to the REF V position.

2.5 Grounding Considerations

This section explains the grounding techniques that should be considered when designing or configuring systems using analog devices such as the ADC.

2.5.1 Grounding Problems

When designing analog circuits that share a ground with digital and high current power supplies, the voltage drop along the high current paths must be taken into account. This voltage drop is a result of the current flowing through the greater-than-zero resistance of the current path, and/or high frequency current transients flowing through the greater-than-zero inductance of a current path.

If the signal ground is connected to the power supply ground at a location where excessive power currents may flow through the analog ground, the voltage drop is injected into the signal ground and appears as part of the signal, thus causing an error.

2.5.2 Using a Single Ground Point

For low frequency circuits, usually below 100 kHz, the solution is to establish a single ground point on the PC board and connect all grounds individually to that point (the EVM single ground point is at the GND terminal of the power supply connector). By using this method, currents flowing along any one path to ground do not inject error voltages in any other ground path.

2.5.3 A Practical Approach

As a practical implementation, however, it may not be reasonable to run a separate ground trace for each component that connects to ground. Therefore, the next best approach is to group the higher current grounds (such as the power supply and digital grounds) together and run them to the central PC board ground point, while still maintaining separate ground paths for the analog grounds.

An analysis of current flow paths within the analog section gives an indication of which grounded components could be grouped together into a common ground path and which should be kept separate. For instance, on the EVM, it would be reasonable to use a common path for the TLC2543 REF– terminal, the TL1431 anode, and the grounded side of R23. This is because the only significant current flow is through the TL1431 (approximately 1 mA) and is not enough to cause a significant error. (A 1/2 LSB error at a reference voltage of 4.1 V would be approximately 0.5 mV, so the ground trace would have to be in excess of 0.5 Ω to cause such an error.)

If all of the input signals are low current, such as the optical sensor (approximately 2 mA), the temperature sensor (approximately 1 mA), and the potentiometer (approximately 0.25 mA), it may be reasonable to use a common ground trace. (As always, wider trace widths are desirable to keep the resistance low.) Whenever high currents are associated with any input signal, always use a separate PC board trace directly to the central ground point location.

Even though the operating current of the TLC2543 is low (2.5 mA maximum), some high speed current transients due to the internal digital switching are present and a separate ground trace is reasonable.

Note:

Keep the power supply decoupling capacitor as close as possible to the supply pins using a separate ground trace for the decoupling capacitor and the TLC2543 ground pin.

If free area is available, or if the PC board is multilayer, a large ground plane may be acceptable to connect all of the analog side ground connections, providing that any one signal ground connection is not carrying a large current. That ground plane should be connected directly to the central ground point without touching any of the digital or power supply ground locations along its path.

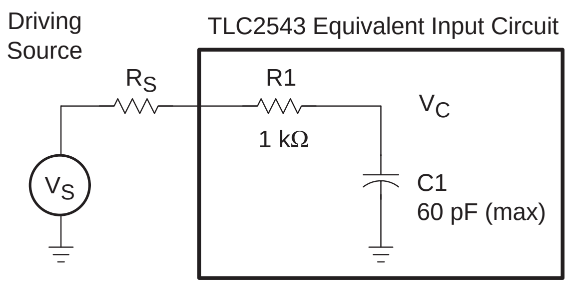
2.6 Power Considerations

Analyzing the distribution of the digital and analog 5-V current paths on the PCB in a similar manner to the grounds is also a good practice. The designated central power point location is the 5-V terminal of the power supply connector (J2) on the EVM board.

2.7 Driving the Input of a Switched-Capacitor ADC

When applying an analog signal to the input of a switched-capacitor ADC such as the TLC2543, care must be taken to provide a low enough impedance to the input terminal to charge the internal capacitor (see Figure 2–3) enough for an accurate conversion during the sampling phase of the converter. The sampling time depends on the period of the I/O clock rate being used to drive the converter and the number of transfer bits commanded. With the maximum I/O clock frequency of 4.1 MHz and a 12-bit transfer mode, the TLC2543 uses eight clock cycles (or approximately 2 µs) for the sampling time.

Figure 2–3. Equivalent Input Circuit



The input equivalent circuit of the TLC2543 looks like a series resistance and a capacitor to ground during sampling and an open circuit during conversion.

For accurate operation the input capacitor must be charged to the required accuracy of 1/2 LSB (or more, depending on the required system error budget) during the sampling phase of the ADC cycle.

The voltage on capacitor C1 is given by:

$$V_C = V_S\left(1 - e^{-t/TC}\right) \qquad (1)$$

Where:

TC = the time constant $C1(R_S + R1)$

The final voltage value of V_C within 1/2 LSB of V_S is given by:

$$V_C\,(1/2\ \text{LSB}) = V_S - V_S/2^{n+1} \qquad (2)$$

Where:

n = the resolution of the converter.

Equating equation 1 to equation 2, then:

$$V_S - V_S/2^{n+1} = V_S\left(1 - e^{-t/TC}\right) \qquad (3)$$

Therefore, the charging time in terms of the circuit time constants is:

$$t\,(1/2\ \text{LSB}) = TC\ \ln\left(2^{n+1}\right) \qquad (4)$$

For a 12-bit converter, this would be:

$$t_S = TC \times \ln(8192) = 9TC \qquad (5)$$

The internal capacitance for the TLC2543 is 60 pF maximum and the internal series resistance is 1 kΩ. Therefore, with an I/O clock at 4.1 MHz and a 12-bit transfer mode (sample period = 2 μs), the time constant should be no more than:

$$1/9 \text{ x } 2 \ \mu s = 0.22 \ \mu s \tag{6}$$

Therefore,

$$C1(R_S + R1) = 0.22 \ \mu s \tag{7}$$

So,

$$(R_S + R1) = 3.67 \ K\Omega \tag{8}$$

Since R_S = 1 kΩ, the source impedance should be less than 2.67 kΩ to stay within 1/2 LSB error. Good design practice dictates that the source impedance be as low as possible, such as the output of an op-amp. However, in an application where fast conversion time is not critical, slow I/O clock rates can allow the driving source impedance to be relatively large.

Chapter 3

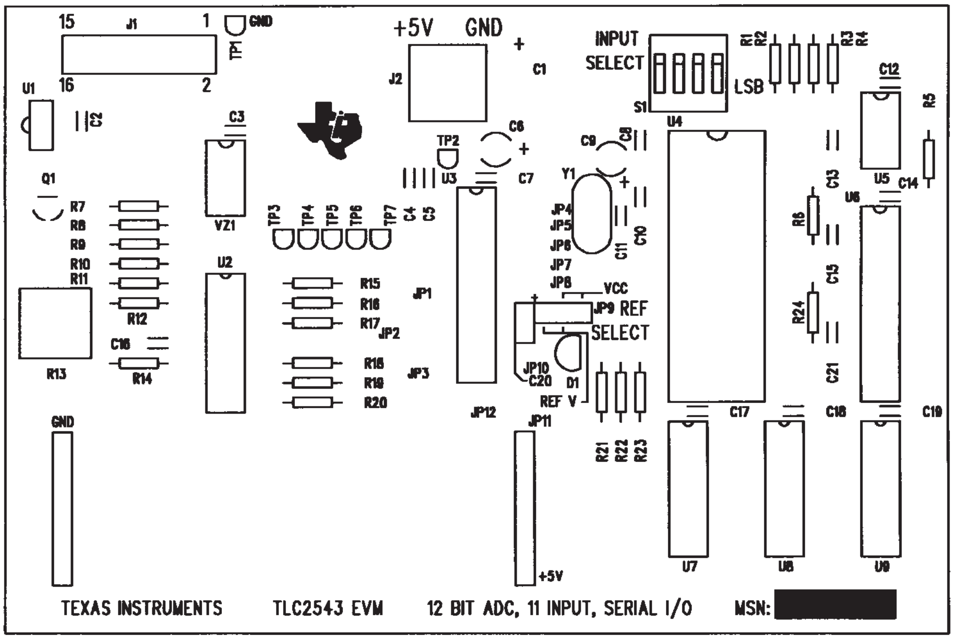
Board Layout

This chapter contains illustrations of the board layout and layers.

Topic **Page**

3.1 Board Layout

Figure 3–1. TLC2543EVM Board Layout



3.2 Board Layers

Figure 3–2. Solder Mask

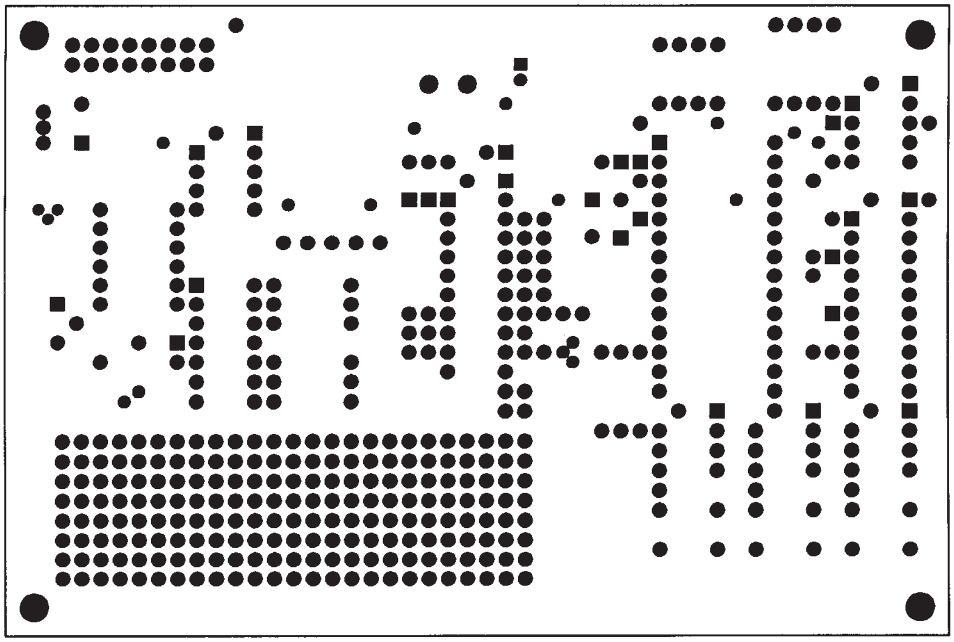


Figure 3–3. Layer 1

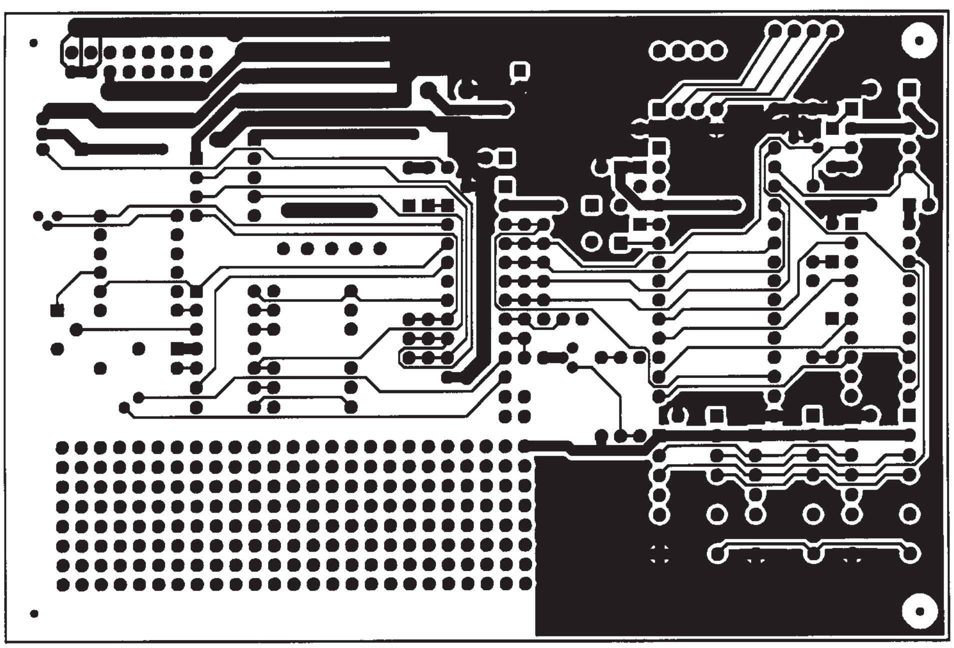


Figure 3–4. Layer 2 (Bottom Side)

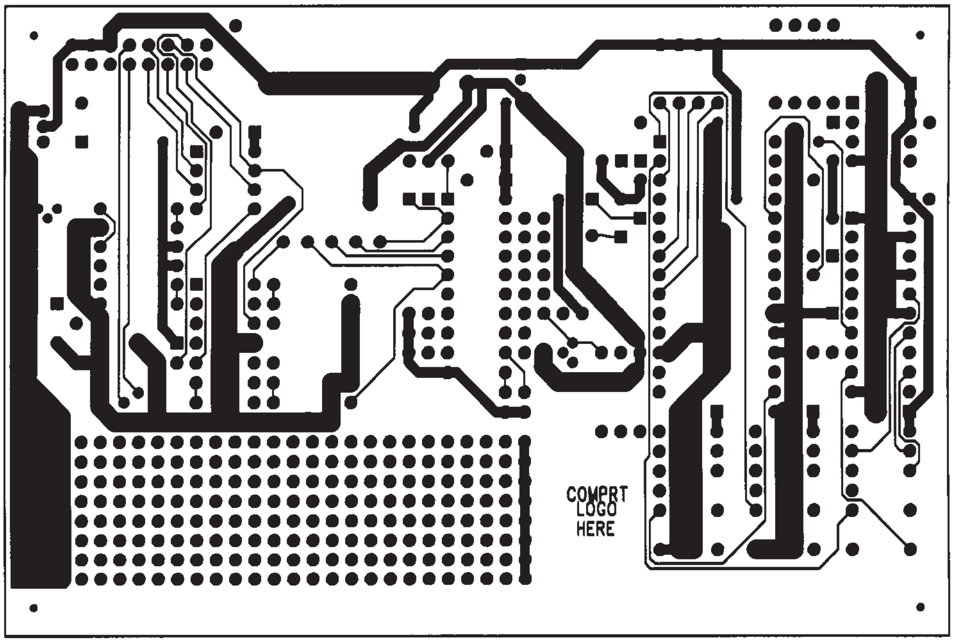
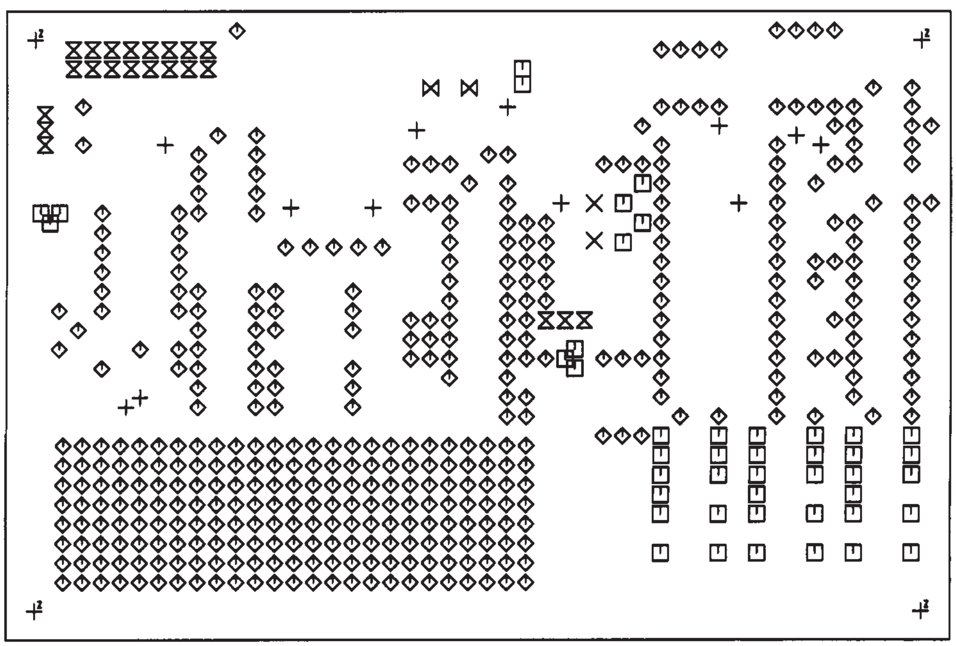


Figure 3–5. Drill Template



Chapter 4

Part Descriptions

Table 4–1 lists and describes the TLC2543 EVM parts.

Table 4–1. Part Descriptions

Description	Reference	Quantity	Value/Type Number
Capacitors	C1	1	100 µF, 16 V aluminum
	C2, C3, C4, C5, C7, C8, C12, C13, C14, C15, C16, C17, C18, C19	14	0.1 µF ceramic, Z5U, 0.2-inch
	C6, C9,	2	10 µF, 10 V tantalum, 0.2-inch
	C10, C11	2	15 pF ceramic, NPO, 0.2-inch
Precision programmable reference	D1	1	TL1431CLP
Power supply terminals	J2	1	Terminal block, 2-pos, 5-mm, side entry (OST ED1601)
Header and shorting jumper	JP9	1	3-pin header
		1	2-pin jumper
Temperature sensor	Q1	1	2N2222A (T0–18 metal can)
Resistors	R1, R2, R3, R4, R5, R10, R11, R12, R14, R15, R16, R17, R18, R19, R20, R23	16	10 kΩ, 1%, 0.25-W
	R6	1	499 Ω
	R7, R8	2	49.9 kΩ
	R9	1	4.99 kΩ
	R21	1	1 kΩ
	R22	1	6.34 kΩ
	R13	1	10 kΩ potentiometer, single turn, top adj, 3/8-inch sq (Bourns 3386 P)
Input select switch	S1	1	DIP, 4-pos, gold
Optical sensor	U1	1	TSL251
Rail-to-rail operational amplifiers	U2	1	TLC2264
12-bit analog-to-digital converter	U3	1	TLC2543
Microcontroller	U4	1	TMS370C712
Supply voltage supervisor	U5	1	TL7705B
Octal buffer	U6	1	74HC244
Hexadecimal display with logic	U7, U8, U9	3	TIL311
Hex clamping circuits	VZ1	1	TL7726
Crystal	Y1	1	12 MHz, HC–49/µs
PCB		1	TLC2543 EVM

Chapter 5

Software Program and Flow Charts

This chapter lists the software program and provides flow charts for the program and each of the programs subroutines.

The following topics are covered:

Topic **Page**

5.1 Software Program

```
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adc_evm.asm                                                      PAGE    1

                ;;;;;;;;;;;;;;;;;;;;;;;;
                ;
                ; TLC2543 EVALUATION MODULE PROGRAM
                ;
                ;       VERSION 1.2   8/17/95
                ;
                ;       THIS PROGRAM READS A FOUR–POSITION DIP
                ;       SWITCH WHICH IS USED TO SELECT THE INPUT
                ;       SIGNAL CHANNEL TO THE ADC.  THE PROGRAM
                ;       THEN SELECTS THIS CHANNEL ON THE ADC AND
                ;       CONVERTS THE ANALOG INPUT TO A 12–BIT
                ;       HEX NUMBER AND OUTPUTS THE RESULTS ON
                ;       3 7–SEGMENT DISPLAYS. POSITIONS ARE ALSO
                ;       PROVIDED TO PUT THE ADC IN A POWER–DOWN
                ;       MODE AND A FAST MODE (APPROX 26 kHz RATE).
                ;
                ;;;;;;;;;;;;;;;;;;;;;;;;
                ;;;;;;;;;;;;;;;;;;;;;;;;
                ;
                ; SYSTEM EQUATES
                ;
                ;;;;;;;;;;;;;;;;;;;;;;;;
                ;
                ; SERIAL PERIPHERAL INTERFACE (SPI) REGISTERS
                ;
        0030    SPICCR  .EQU    P030    ;SPI CONFIG REG
        0031    SPICTL  .EQU    P031    ;SPI OPERATION CONTROL REG
        0037    SPIBUF  .EQU    P037    ;SPI INPUT BUFFER
        0039    SPIDAT  .EQU    P039    ;SPI SERIAL DATA REG
        003d    SPIPC1  .EQU    P03D    ;SPI PORT CONTROL REG1
        003e    SPIPC2  .EQU    P03E    ;SPI PORT CONTROL REG2
        003f    SPIPRI  .EQU    P03F    ;SPI INTERRUPT CONTROL REG
                ;
                ; PORT A AND D REGISTERS
                ;
        0021    APORT2  .EQU    P021    ;PORT A CONTROL REG
        0022    ADATA   .EQU    P022    ;PORT A DATA
        0023    ADIR    .EQU    P023    ;PORT A DIRECTION
        002c    DPORT1  .EQU    P02C    ;PORT D CONTROL REG1
        002d    DPORT2  .EQU    P02D    ;PORT D CONTROL REG 2
        002e    DDATA   .EQU    P02E    ;PORT D DATA
        002f    DDIR    .EQU    P02F    ;PORT D DIRECTION
                ;
                ; TIMER 1 DEFINITIONS
                ;
        0040    T1CNTR1 .EQU    P040    ;MSB OF COUNTER
        0041    T1CNTR2 .EQU    P041    ;LSB OF COUNTER
        0042    TC11    .EQU    P042    ;MSB OF COMPARE REGISTER
        0043    TC12    .EQU    P043    ;LSB OF COMPARE REGISTER
        0049    T1CTL1  .EQU    P049    ;TIMER 1 CONTROL REG 1
        004a    T1CTL2  .EQU    P04A    ;TIMER 1 CONTROL REG 2
        004b    T1CTL3  .EQU    P04B    ;TIMER 1 CONTROL REG 3
                ;
                ; BIT DEFINITIONS
                ;
```

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            2e        CSBIT   .DBIT   3,DDATA   ;ADC CHIP SELECT BIT
            31        SPIF    .DBIT   6,SPICTL  ;SPI INTR FLAF
            2e        DOUT1   .DBIT   5,DDATA   ;STROBE FOR DISPLAY 1
            2e        DOUT2   .DBIT   6,DDATA   ;STROBE FOR DISPLAY 2
            2e        DOUT3   .DBIT   7,DDATA   ;STROBE FOR DISPLAY 3
            2e        DBLANK  .DBIT   4,DDATA   ;BLANK STROBE
            4a        RST     .DBIT   0,T1CTL2  ;SW TIMER RESET
            4b        TOUT    .DBIT   5,T1CTL3  ;TIMER 1 TIME OUT
                      ;
                      ;;;;;;;;;;;;;;;;;;;;;;;;
                      ;
     6000                     .TEXT   6000H   ;START OF PROGRAM
                      ;
                      ;;;;;;;;;;;;;;;;;;;;;;;;
                      ;
                      ; MAIN PROGRAM
                      ;
     6000   5260      START   MOV     #60H,B
     6002   fd                LDSP            ;SET STACK POINTER TO 60H
     6003  ’8e6014            CALL    INIT    ;INITIALIZE SYSTEM
                      ;
     6006  ’8e6056    LOOP    CALL    READSW  ;READ INPUT DIP SWITCH
     6009  ’8e60ed            CALL    ADC     ;DIGITIZE INPUT
     600c  ’8e614d            CALL    DISPLAY ;DISPLAY VALUE
     600f  ’8e6126            CALL    DELAY   ;DELAY .5 SEC
     6012  ’00f2              JMP     LOOP
                      ;
                      ;;;;;;;;;;;;;;;;;;;;;;;;
                      ;;;;;;;;;;;;;;;;;;;;;;;;
                      ;
                      ; INIT
                      ;
                      ;       THIS ROUTINE INITIALIZES PORTS A AND
                      ;       D, SETS UP THE SPI, AND INITIALIZES
                      ;       THE DISPLAYS BY FLASHING 8 AND 0 THREE
                      ;       TIMES.
                      ;
     6014   f70021    INIT    MOV     #0,APORT2  ;SET PORT A TO I/O
     6017   f70f23            MOV     #0FH,ADIR  ;SET A4–A7=INPUT, A0–A3 = OUTPUT
     601a   f7002c            MOV     #0,DPORT1  ;SET PORT D TO I/O
     601d   f7002d            MOV     #0,DPORT2
     6020   f7f82f            MOV     #0F8H,DDIR ;SET D3–D7 OUTPUTS
                      ;
     6023   f78030            MOV  #80H,SPICCR ;INIT SPI
     6026   f70730            MOV  #07H,SPICCR ;SET CLOCK, 8BIT CHAR LEN
     6029   f7033d            MOV  #03H,SPIPC1 ;SET SPI CLK TO OUTPUT
     602c   f7223e            MOV  #22H,SPIPC2 ;SET SPISOMI AND SPISIMO TO SPI DATA
                      ;
     602f   720019            MOV  #0,R25      ;CLR CHANNEL REGS
     6032   72001d            MOV  #0,R29
                      ;
                      ;       FLASH DISPLAY
                      ;
     6035   720314            MOV  #03,R20 ;SET LOOP CTR TO 3 CYCLES
     6038   2208              MOV  #08H,A  ;SET DISPLAY REGS TO 8
```

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adc_evm.asm                                                     PAGE    3

603a   d01a                 MOV     A,R26
603c   d01b                 MOV     A,R27
603e   d01c                 MOV     A,R28
6040  ’8e614d    LOOP1      CALL    DISPLAY
6043   720218               MOV     #02H,R24   ;SET DELAY TO .5 SEC
6046  ’8e6126               CALL    DELAY
6049   a4102e               SBIT1   DBLANK     ;BLANK DISPLAY
604c  ’8e6126               CALL    DELAY
604f   a3ef2e               SBIT0   DBLANK     ;TURN OFF BLANK
6052  ’da14eb               DJNZ    R20,LOOP1  ;JMP BACK IF NOT DONE
6055   f9        RTS
                 ;
                 ;;;;;;;;;;;;;;;;;;;;;;;;
                 ;;;;;;;;;;;;;;;;;;;;;;;;
                 ;
                 ;READSW
                 ;
                 ;       THIS ROUTINE READS THE 4 POSITION DIP
                 ;       SWITCH FOR THE CHANNEL NUMBER AND SAVES
                 ;       IT IN R29.  IF 0EH IS SELECTED THE ADC
                 ;       IS PLACED IN A POWER DOWN MODE. IF 0FH
                 ;       IS SELECTED THE INPUT ON CHANNEL 4 IS
                 ;       CONVERTED IN FAST MODE. ADC CHANNEL NUMBER
                 ;       IS STORED IN R25.
                 ;
                 ;
6056   8022      READSW     MOV     ADATA,A ;READ SWITCHES
6058   b7                   SWAP    A       ;SWAP NIBBLES
6059   230f                 AND     #0FH,A
605b   1d1d                 CMP     R29,A
605d  ’0601                 JNE     READ1   ;JMP IF ADC INPUT CHANGED
605f   f9                   RTS
                 ;
                 ; ADC INPUT CHANGED – WAIT FOR COMPLETE
                 ;
6060   d01d      READ1      MOV     A,R29   ;SAVE IT
6062   720318               MOV     #03,R24 ;SET DELAY FLAG TO 2 SEC
6065  ’8e6126               CALL    DELAY
6068   8022                 MOV     ADATA,A ;CHECK AGAIN
606a   b7                   SWAP    A
606b   230f                 AND     #0FH,A
606d   1d1d                 CMP     R29,A
606f  ’06ef                 JNE     READ1
                 ;
                 ;SEE IF POWER DOWM MODE
                 ;
6071   7d0e1d               CMP     #0EH,R29
6074  ’061b                 JNE     READ2   ;JMP IF NOT POWER DOWN
6076   a4102e               SBIT1   DBLANK  ;BLANK DISPLAY
6079   a3f72e               SBIT0   CSBIT   ;ENABLE ADC
607c   f70631               MOV     #06H,SPICTL
607f   f7ec39               MOV     #0ECH,SPIDAT
6082   8022      READ3      MOV     ADATA,A ;WAIT FOR CHANGE
6084   b7                   SWAP    A
6085   230f                 AND     #0FH,A
```

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6087 * 4d001d             CMP     A,R29
608a  '02f6               JEQ     READ3
608c   a3ef2e             SBIT0   DBLANK       ;CLEAR BLANK
608f  '00cf               JMP     READ1
                  ;
                  ; SEE IF FAST MODE
                  ;
6091   7d0f1d    READ2    CMP     #0FH,R29      ;IS IT FAST MODE
6094  '0650               JNE     READ4
6096   a3f72e    RLOOP1   SBIT0   CSBIT         ;ENABLE ADC
6099   720419             MOV     #04H,R25      ;CHANNEL 4 – FAST MODE
609c   224c               MOV     #4CH,A        ;CHANNEL 4,16BITS,MSB 1ST
609e   721414             MOV     #20,R20       ;DO 20 FAST THEN UPDATE
60a1   f70631             MOV     #06H,SPICTL
60a4   2139      RLOOP2   MOV     A,SPIDAT
60a6  'a74031fc  RFLG1    JBIT0   SPIF,RFLG1    ;WAIT FOR DATA
60aa   a21537             MOV     SPIBUF,R21
60ad   2139               MOV     A,SPIDAT
60af  'a74031fc  RFLG2    JBIT0   SPIF,RFLG2    ;WAIT FOR DATA
60b3   a21637             MOV     SPIBUF,R22
60b6   ff                 NOP                   ;GIVE TIME FOR
60b7   ff                 NOP                   ; CONVERSION TO
60b8   ff                 NOP                   ;  COMPLETE
60b9  'da14e8             DJNZ    R20,RLOOP2
                 ;DISPLAY VALUE
60bc   42151a             MOV     R21,R26
60bf   d71a               SWAP    R26
60c1   730f1a             AND     #0FH,R26      ;SAVE MSDIGIT IN R26
60c4   42151b             MOV     R21,R27
60c7   730f1b             AND     #0FH,R27      ;SAVE MIDDLE DIGIT IN R27
60ca   42161c             MOV     R22,R28
60cd   d71c               SWAP    R28
60cf   730f1c             AND     #0FH,R28      ;SAVE LSDIGIT IN R28
60d2  '8e614d             CALL    DISPLAY
60d5   a4082e             SBIT1   CSBIT         ;DISABLE ADC
                 ;SEE IF FAST MODE STILL SELECTED
60d8   8022               MOV     ADATA,A       ;WAIT FOR CHANGE
60da   b7                 SWAP    A
60db   230f               AND     #0FH,A
60dd * 4d001d             CMP     A,R29
60e0  '02b4               JEQ     RLOOP1
60e2 *'89ff7b             JMP     READ1
60e5   f9                 RTS
                 ;
                 ; SETUP CHANNEL # IN R25
                 ;
60e6   421d19    READ4    MOV     R29,R25
60e9   720218             MOV     #02,R24       ;SET DELAY TO .5SEC
60ec   f9                 RTS
                 ;
                 ;;;;;;;;;;;;;;;;;;;;;;;;
                 ;;;;;;;;;;;;;;;;;;;;;;;;
                 ;
                 ; ADC
                 ;
```

```
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                       ;       THIS ROUTINE DIGITIZES THE INPUT ON
                       ;       THE CHANNEL SPECIFIED IN R25.  THE RESULTS
                       ;       ARE PLACED IN REGISTERS R26, R27, AND R28.
                       ;
    60ed   1219        ADC     MOV     R25,A
    60ef   b7                  SWAP    A
    60f0   23f0                AND     #0F0H,A       ;CHANNEL # IN MS NIBBLE
    60f2   240c                OR      #0CH,A        ;16 BITS, MSB 1ST, BINARY
    60f4   a3f72e              SBIT0   CSBIT         ;ENABLE ADC
    60f7   f70631              MOV     #06H,SPICTL
    60fa   2139                MOV     A,SPIDAT
    60fc  ’a74031fc    ADCFLG1 JBIT0   SPIF,ADCFLG1  ;WAIT FOR DATA
    6100   a21537              MOV     SPIBUF,R21    ;SAVE MSBYTE
    6103   2139                MOV     A,SPIDAT
    6105  ’a74031fc    ADCFLG2 JBIT0   SPIF,ADCFLG2  ;WAIT FOR DATA
    6109   a21637              MOV     SPIBUF,R22    ;SAVE LSBYTE
                       ;
                       ; SAVE DATA
                       ;
    610c   42151a              MOV     R21,R26
    610f   d71a                SWAP    R26
    6111   730f1a              AND     #0FH,R26      ;SAVE MSDIGIT IN R26
    6114   42151b              MOV     R21,R27
    6117   730f1b              AND     #0FH,R27      ;SAVE MIDDLE DIGIT IN R27
    611a   42161c              MOV     R22,R28
    611d   d71c                SWAP    R28
    611f   730f1c              AND     #0FH,R28      ;SAVE LSDIGIT IN R28
    6122   a4082e              SBIT1   CSBIT         ;DISABLE ADC
    6125   f9                  RTS
                       ;
                       ;;;;;;;;;;;;;;;;;;;;;;;;;
                       ;;;;;;;;;;;;;;;;;;;;;;;;;
                       ;
                       ; DELAY
                       ;       THIS ROUTINE USES TIMER 1 AS
                       ;       A GENERAL PURPOSE TIMER TO
                       ;       DELAY 0, .5, OR 2 SECONDS.
                       ;       R24 IS SET AS FOLLOWS:
                       ;               1 = 0 SEC.
                       ;               2 = 0.5 SEC.
                       ;               3 = 2 SEC.
                       ;
    6126   7d0118      DELAY   CMP     #1,R24        ;SEE IF NO DELAY
    6129  ’0601                JNE     DELAY1
    612b   f9                  RTS
    612c   7d0218      DELAY1  CMP     #2,R24        ;SEE IF 0.5 SEC DELAY
    612f  ’0614                JNE     DELAY2
    6131   f71642              MOV     #16H,TC11     ;0.5 SEC COMPARE VALUE
    6134   f7e343              MOV     #0E3H,TC12
    6137   a40749      DLOOP   OR      #07H,T1CTL1   ;SET PRESCALER TO 256
    613a   a4014a              OR      #1,T1CTL2     ;START COUNTER AT ZERO
    613d   a3df4b              SBIT0   TOUT          ;CLR CMP FLAG
    6140  ’a7204bfc    DFLAG1  JBIT0   TOUT,DFLAG1   ;WAIT FOR TIMEOUT
    6144   f9                  RTS
    6145   f75b42      DELAY2  MOV     #5BH,TC11     ;2–SEC COMPARE VALUE
```

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6148   f78d43             MOV     #8DH,TC12
614b  '00ea               JMP     DLOOP
                  ;
                  ;;;;;;;;;;;;;;;;;;;;;;;;
                  ;;;;;;;;;;;;;;;;;;;;;;;;
                  ;
                  ; DISPLAY
                  ;
                  ;       THIS ROUTINE DISPLAYS THE HEX
                  ;       DIGITS STORED IN REGS R26, R27,
                  ;       AND R28.
                  ;
614d   321a       DISPLAY MOV     R26,B           ;OUTPUT LSD
614f  'aa6175             MOV     *DTBL[B],A
6152   2122               MOV     A,ADATA
6154   a3df2e             SBIT0   DOUT1           ;STROBE IT
6157   a4202e             SBIT1   DOUT1
615a   321b               MOV     R27,B           ;OUTPUT MIDDLE DIGIT
615c  'aa6175             MOV     *DTBL[B],A
615f   2122               MOV     A,ADATA
6161   a3bf2e             SBIT0   DOUT2
6164   a4402e             SBIT1   DOUT2
6167   321c               MOV     R28,B           ;OUTPUT MSD
6169  'aa6175             MOV     *DTBL[B],A
616c   2122               MOV     A,ADATA
616e   a37f2e             SBIT0   DOUT3
6171   a4802e             SBIT1   DOUT3
6174   f9                 RTS
6175   00         DTBL    .BYTE   00H             ;0
6176   08                 .BYTE   08H             ;1
6177   04                 .BYTE   04H             ;2
6178   0c                 .BYTE   0CH             ;3
6179   02                 .BYTE   02H             ;4
617a   0a                 .BYTE   0AH             ;5
617b   06                 .BYTE   06H             ;6
617c   0e                 .BYTE   0EH             ;7
617d   01                 .BYTE   01H             ;8
617e   09                 .BYTE   09H             ;9
617f   05                 .BYTE   05H             ;A
6180   0d                 .BYTE   0DH             ;B
6181   03                 .BYTE   03H             ;C
6182   0b                 .BYTE   0BH             ;D
6183   07                 .BYTE   07H             ;E
6184   0f                 .BYTE   0FH             ;F
                  ;;;;;;;;;;;;;;;;;;;;;;;;
                  ;;;;;;;;;;;;;;;;;;;;;;;;
7ffe                      .SECT   "RESET",7FFEH  ;RESET VECTOR ADDR
7ffe   6000               .WORD   6000H           ;PROGRAM START
                  ;
                          .END

 No Errors,  No Warnings
```

5.2 Flow Charts

The flow charts for the TLC2543 EVM are shown in Figure 5–1 through Figure 5–6.

Figure 5–1. Main Program Flow Chart

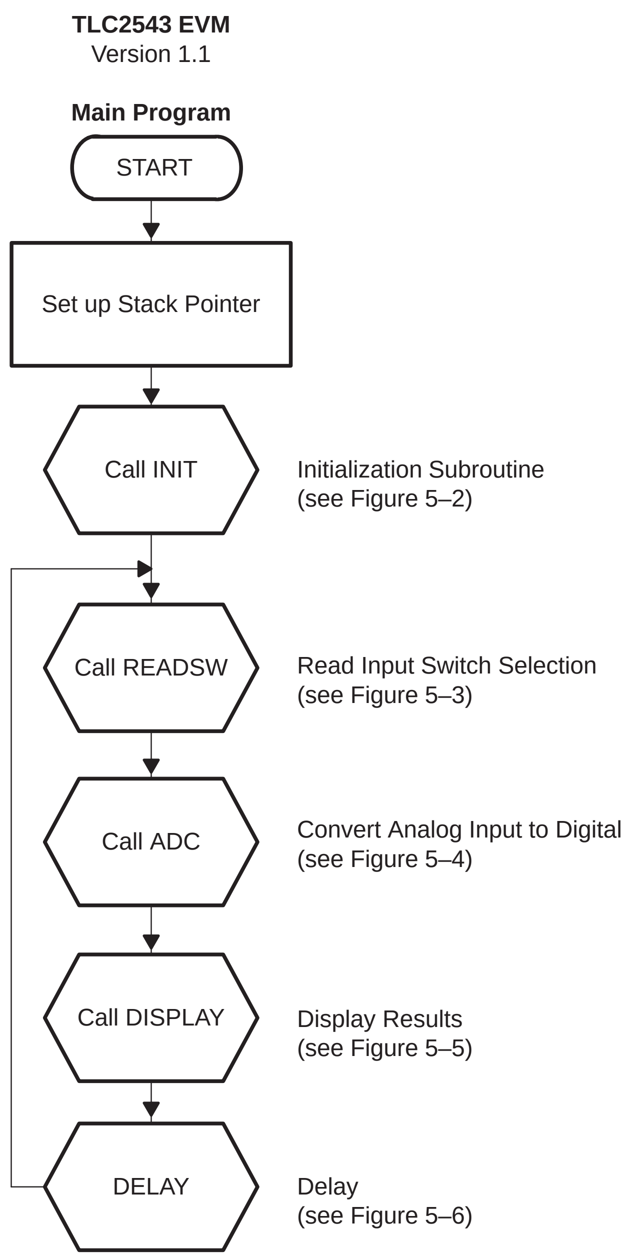

Figure 5–2. Initialization Subroutine Flow Chart

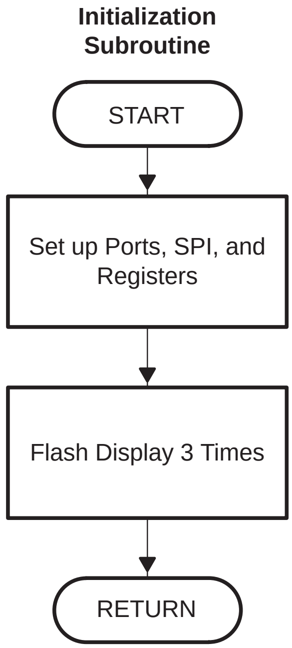

Figure 5–3. Read Input Switch Subroutine Flow Chart

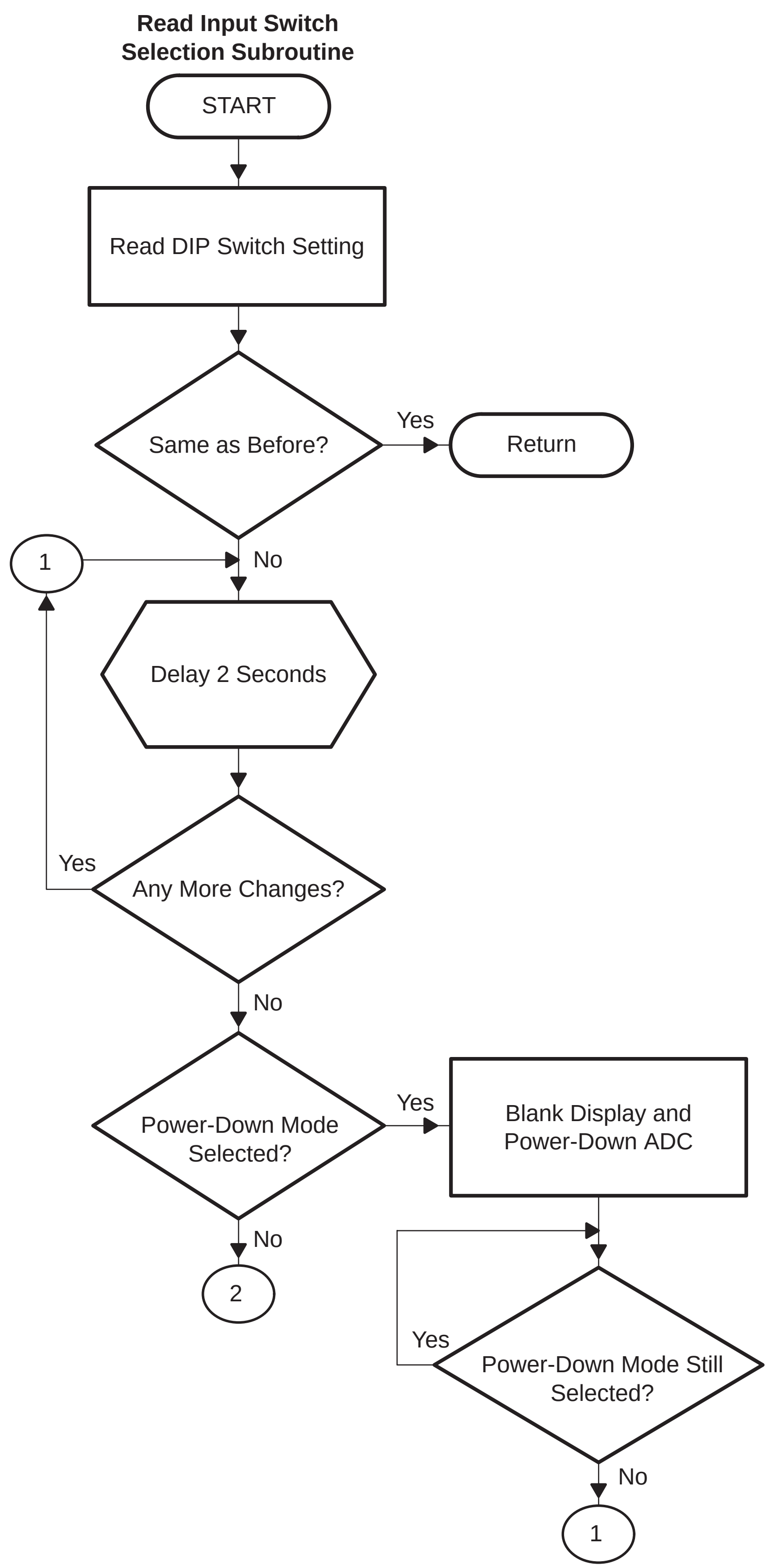

Figure 3–3. Read Input Switch Subroutine Flow Chart (Continued)

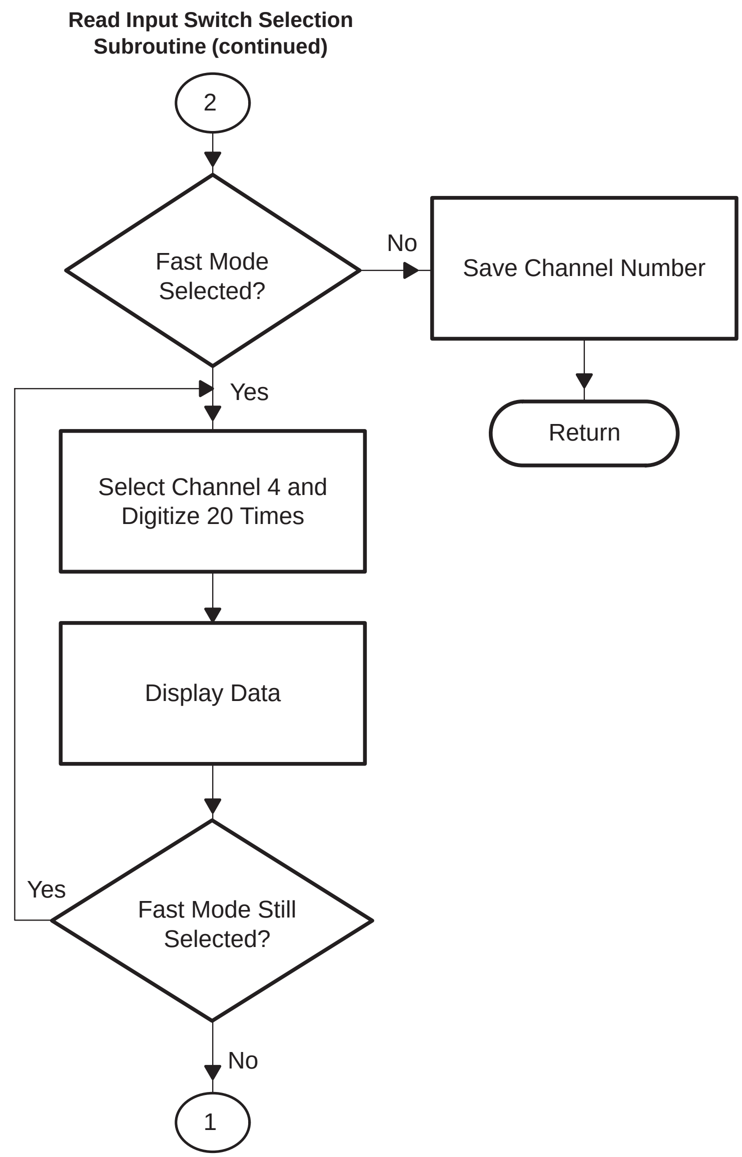

Figure 5–4. Analog-to-Digital Convert Subroutine Flow Chart

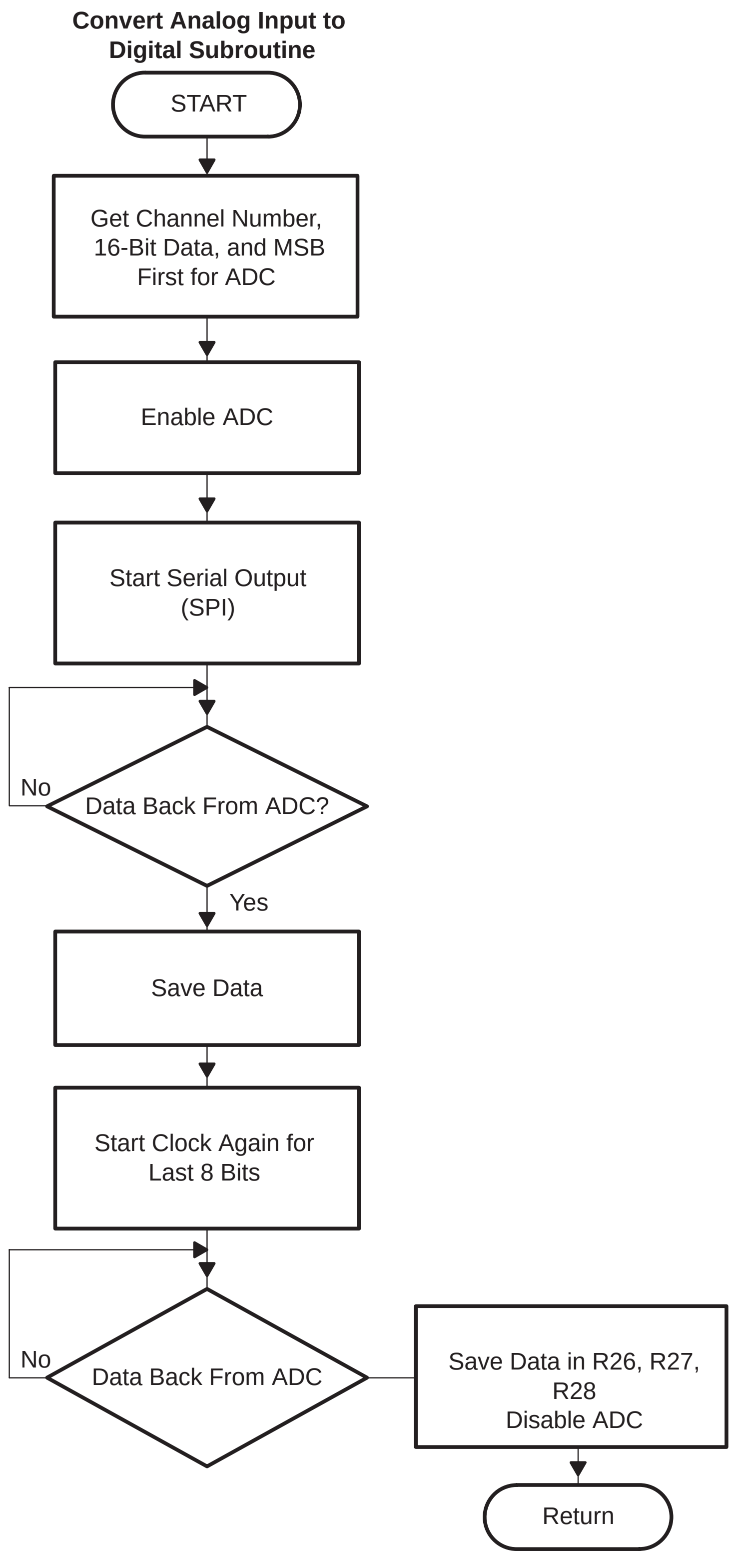

Figure 5–5. Display Subroutine Flow Chart

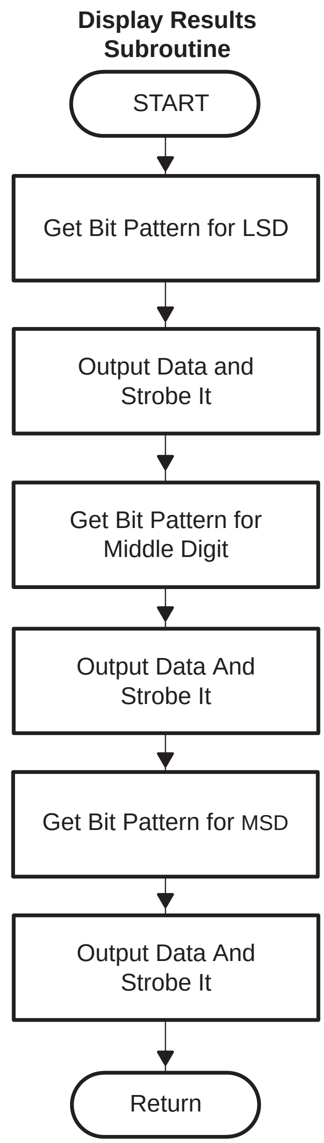

Figure 5–6. Delay Subroutine Flow Chart