

SN74F657

OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS

SDFS027A – D3217, JANUARY 1989 – REVISED OCTOBER 1993

- Combines 'F245 and 'F280B Functions in One Package
- High-Impedance N-P-N Inputs for Reduced Loading (70 μ A in Low and High States)
- High Output Drive and Light Bus Loading
- 3-State B Outputs Sink 64 mA and Source 15 mA
- Input Diodes for Termination Effects
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

description

The SN74F657 contains eight noninverting buffers with 3-state outputs and an 8-bit parity generator/checker. It is intended for bus-oriented applications. The buffers have a specified current sinking capability of 24 mA at the A port and 64 mA at the B port.

The transmit/receive ($\overline{T/R}$) input determines the direction of the data flow through the bidirectional transceivers. When $\overline{T/R}$ is high, data is transmitted from the A port to the B port. When $\overline{T/R}$ is low, data is received at the A port from the B port.

When the output enable (\overline{OE}) input is high, both the A and B ports are placed in a high-impedance state (disabled). The $\text{ODD}/\overline{\text{EVEN}}$ input allows the user to select between odd or even parity systems. When transmitting from A port to B port ($\overline{T/R}$ high), PARITY is an output from the generator/checker. When receiving from B port to A port ($\overline{T/R}$ low), PARITY is an input.

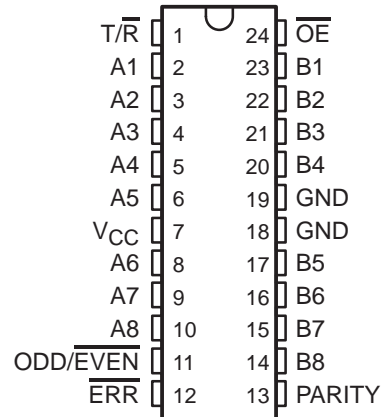
When transmitting ($\overline{T/R}$ high), the parity select ($\text{ODD}/\overline{\text{EVEN}}$) input is made high or low as appropriate. The A port is then polled to determine the number of high bits. The PARITY output goes to the logic state determined by $\text{ODD}/\overline{\text{EVEN}}$ and the number of high bits on A port. When $\text{ODD}/\overline{\text{EVEN}}$ is low (for even parity) and the number of high bits on A port is odd, the PARITY will be high, transmitting even parity. If the number of high bits on A port is even, the PARITY will be low, keeping even parity.

When in the receive mode ($\overline{T/R}$ low), the B port is polled to determine the number of high bits. If $\text{ODD}/\overline{\text{EVEN}}$ is low (for even parity) and the number of highs on B port is:

1. Odd and the PARITY input is high, then $\overline{\text{ERR}}$ will be high signifying no error.
2. Even and the PARITY input is high, then $\overline{\text{ERR}}$ will be low indicating an error.

The SN74F657 is characterized for operation from 0°C to 70°C.

DW OR NT PACKAGE
(TOP VIEW)



SN74F657

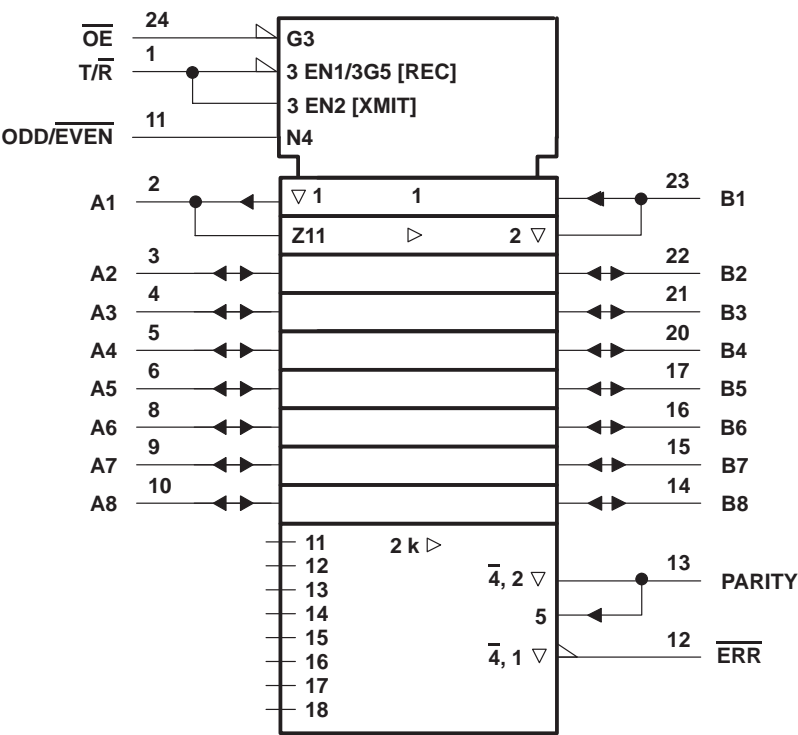
OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER

AND 3-STATE OUTPUTS

SDFS027A – D3217, JANUARY 1989 – REVISED OCTOBER 1993

FUNCTION TABLE						
NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	\overline{OE}	T/\overline{R}	ODD/ \overline{EVEN}		\overline{ERR}	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

logic symbol†

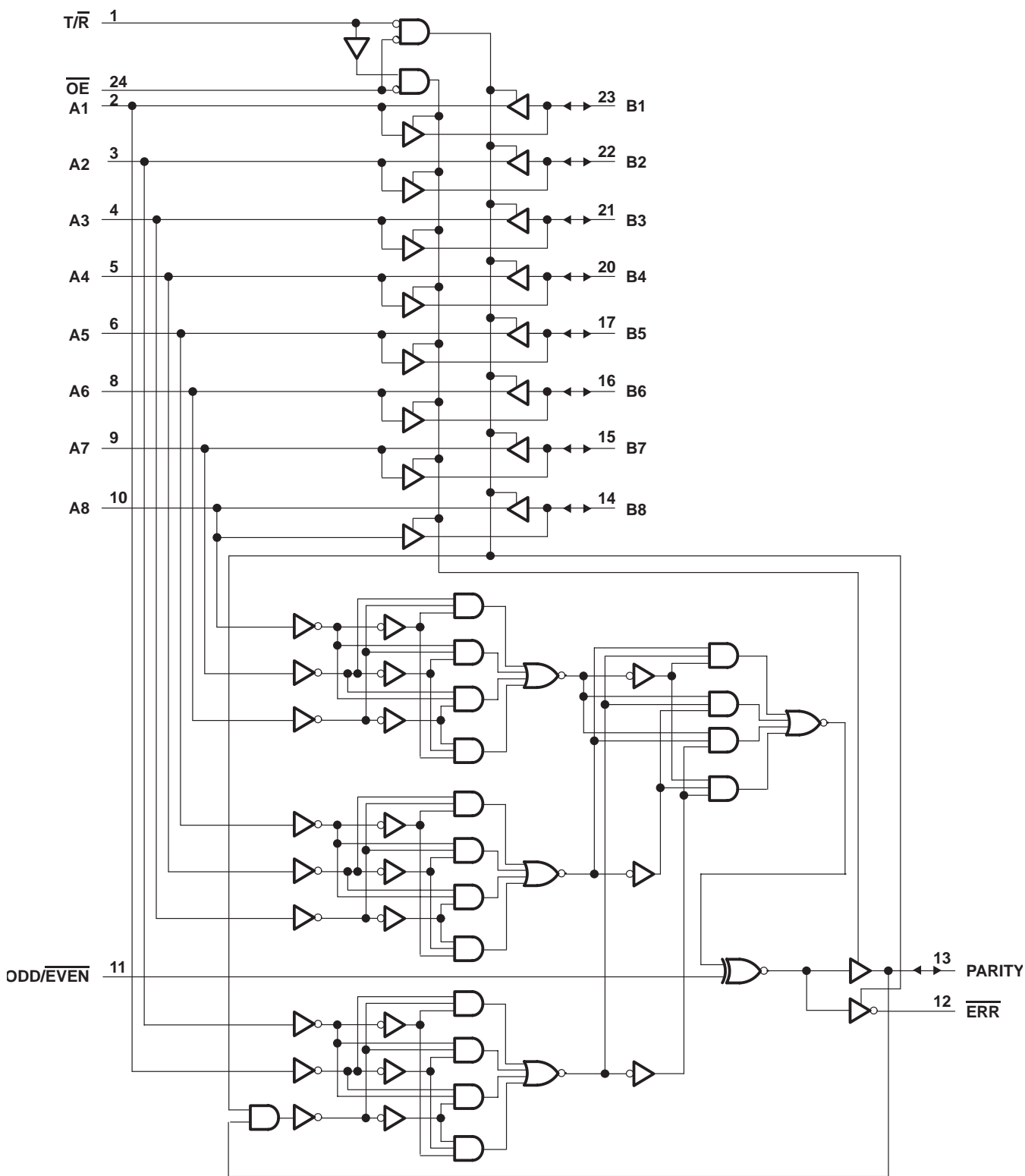


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74F657 OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS

SDFS027A – D3217, JANUARY 1989 – REVISED OCTOBER 1993

logic diagram (positive logic)



SN74F657

OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS

SDFS027A – D3217, JANUARY 1989 – REVISED OCTOBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (excluding I/O ports) (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state	–0.5 V to 5.5 V
Voltage range applied to any output in the high state	–0.5 V to V_{CC}
Current into any output in the low state: A1–A8	48 mA
B1–B8	128 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	A1–A8		–3	mA
		B1–B8, PARITY, \overline{ERR}		–12	
I_{OL}	Low-level output current	A1–A8		24	mA
		B1–B8, PARITY, \overline{ERR}		64	
T_A	Operating free-air temperature	0		70	°C



SN74F657

OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS

SDFS027A – D3217, JANUARY 1989 – REVISED OCTOBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}	Any output	$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -3\text{ mA}$	2.4	3.3		V
	B1–B8, PARITY, \overline{ERR}	$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -15\text{ mA}$	2	3.1		
	Any output	$V_{CC} = 4.75\text{ V}$,	$I_{OH} = -1\text{ mA to } -3\text{ mA}$	2.7			
V_{OL}	A1–A8	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 24\text{ mA}$		0.35	0.5	V
	B1–B8, PARITY, \overline{ERR}		$I_{OL} = 64\text{ mA}$		0.42	0.55	
I_I	$\overline{T/R}$	$V_{CC} = 0$,	$V_I = 7\text{ V}$,			0.1	mA
	\overline{OE}	$V_{CC} = 0$,	$V_I = 7\text{ V}$,			0.1	
	ODD/EVEN	$V_{CC} = 0$,	$V_I = 7\text{ V}$			0.1	
	A1–A8	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$			2	
	B1–B8					1	
I_{IH}^\ddagger	A, B, PARITY	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			70	μA
	$\overline{T/R}$, \overline{OE}					40	
	ODD/EVEN					20	
I_{IL}^\ddagger	A, B, PARITY	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.5\text{ V}$			-70	μA
	$\overline{T/R}$, \overline{OE}					-40	
	ODD/EVEN					-20	
I_{OS}^\S	A1–A8	$V_{CC} = 5.5\text{ V}$,	$V_O = 0$	-60		-150	mA
	B1–B8			-100		-225	
I_{OZH}	\overline{ERR}	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			50	μA
I_{OZL}	\overline{ERR}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.5\text{ V}$			-50	μA
I_{CCH}		$V_{CC} = 5.5\text{ V}$			90	125	mA
I_{CCL}		$V_{CC} = 5.5\text{ V}$			106	150	mA
I_{CCZ}		$V_{CC} = 5.5\text{ V}$			98	145	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN74F657

OCTAL TRANSCEIVER WITH PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS

SDFS027A – D3217, JANUARY 1989 – REVISED OCTOBER 1993

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	2.5	4.2	7.5	2.5	8	ns
t _{PHL}			3	4	7.5	3	8	
t _{PLH}	A	PARITY	6	8.4	14	6	16	ns
t _{PHL}			6.8	8.5	15	6.8	16	
t _{PLH}	ODD/ $\overline{\text{EVEN}}$	PARITY, $\overline{\text{ERR}}$	4	6.4	11	4	12	ns
t _{PHL}			4.5	6.9	11.5	4.5	12.5	
t _{PLH}	B	$\overline{\text{ERR}}$	8	12.7	20.5	7.5	22.5	ns
t _{PHL}			8	13.4	20.5	7.5	22.5	
t _{PLH}	PARITY	$\overline{\text{ERR}}$	6	8.1	15.5	6	16.5	ns
t _{PHL}			7.5	8.8	15.5	7.5	17	
t _{PZH}	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}^\ddagger$	3	5.3	8	3	9	ns
t _{PZL}			4	5.4	9.5	4	11	
t _{PHZ}	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}^\ddagger$	2	4.2	7.5	2	8	ns
t _{PLZ}			2	3.7	6	2	6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These delay times reflect the 3-state recovery time only and not the signal through the buffers or parity check circuitry. To assure valid information at the $\overline{\text{ERR}}$ output pin, time must be allowed for the signal to propagate through the drivers (B to A), and to the $\overline{\text{ERR}}$ output. Valid data at the $\overline{\text{ERR}}$ output is greater than or equal to (B to A) + (A to PARITY).

NOTE 2: Load circuits and waveforms are shown in Section 1.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.