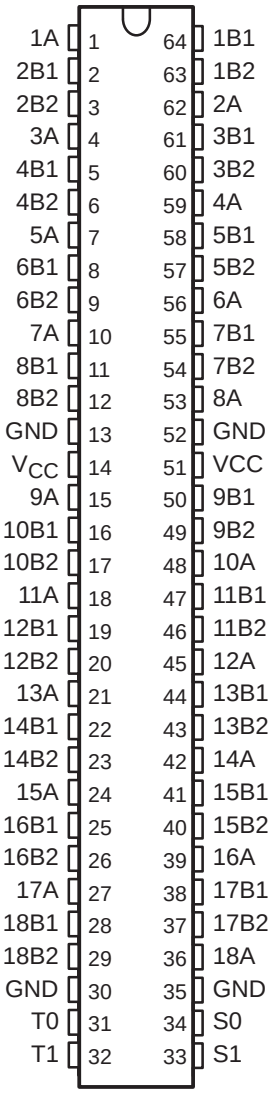
- **4-Ω Switch Connection Between Two Ports**
- **Isolation Under Power-Off Conditions**
- **Break-Before-Make Feature**
- **Packaged in Plastic Thin Shrink Small-Outline Package**

NOTE: For tape and reel order entry:
The DGGR package is abbreviated to GR.

DGG PACKAGE
(TOP VIEW)



description

The SN74CBTLV16235 is an 18-bit 1-of-2 FET multiplexer/demultiplexer used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, where two different banks of memory need to be addressed simultaneously.

The device is organized as a dual 9-bit 1-of-2 multiplexer/demultiplexer with separate control inputs. It can be used as two 9-bit multiplexers/demultiplexers or as one 18-bit multiplexer/demultiplexer. Two select (S0 and S1) inputs control the data flow. When the test (T0 and T1) inputs are asserted, port A is connected to both ports B1 and B2. The control inputs can be driven with a low-voltage TTL or an SSTL_3 driver.

The SN74CBTLV16235 is specified by the break-before-make design to have no through current when switching directions.

The SN74CBTLV16235 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 9-bit multiplexer/demultiplexer)

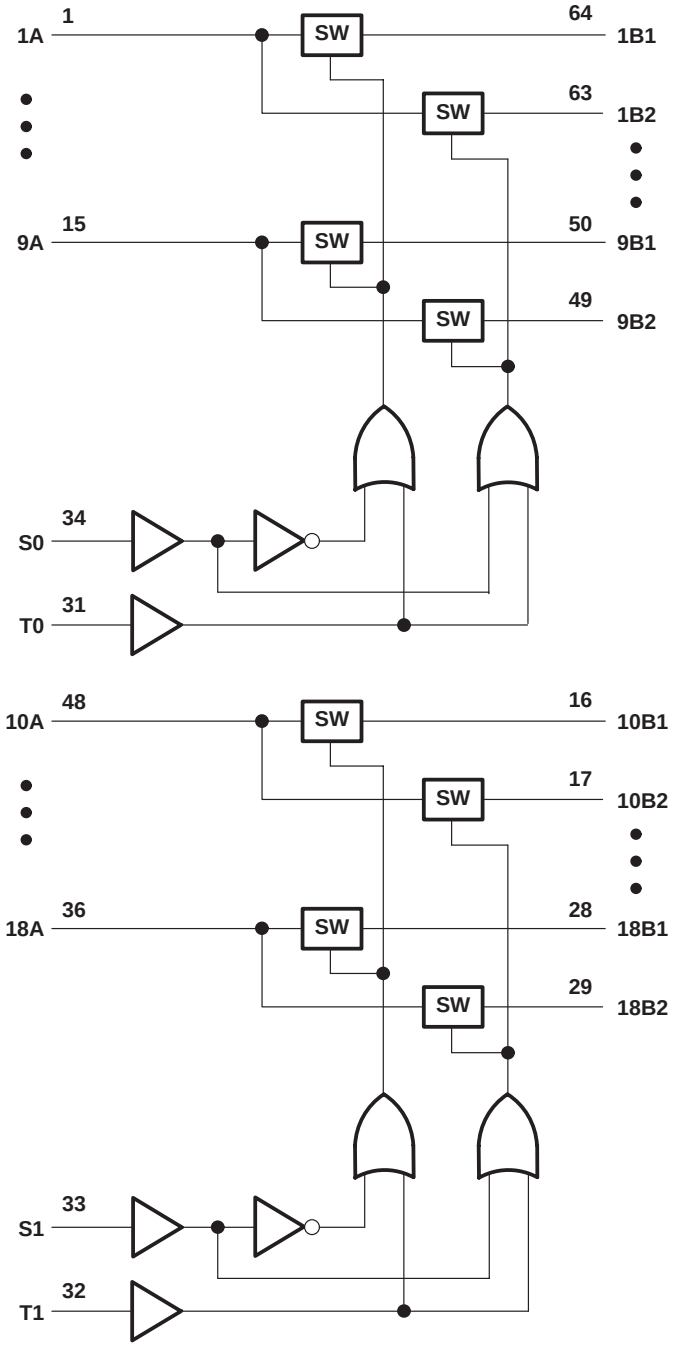
INPUTS		FUNCTION
T	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	A port = B1 port = B2 port

PRODUCT PREVIEW

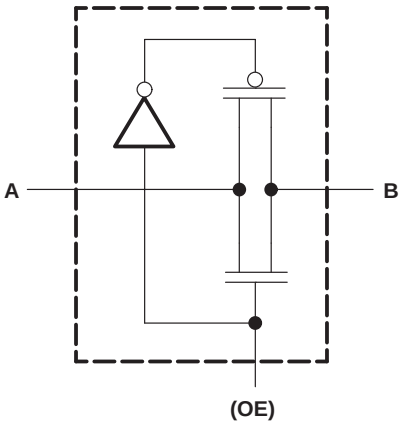
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCT PREVIEW

logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 4.6 V
Continuous channel current . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 55°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±5	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	µA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			10	µA
ΔI_{CC}‡	Control input	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	µA
C_i	Control input	V_I = 3 V or 0						pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0						pF
	B port							
r_{on}§		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA				Ω
				I_I = 24 mA				
			V_I = 1.7 V,	I_I = 15 mA				
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA				
				I_I = 24 mA				
			V_I = 2.4 V,	I_I = 15 mA				

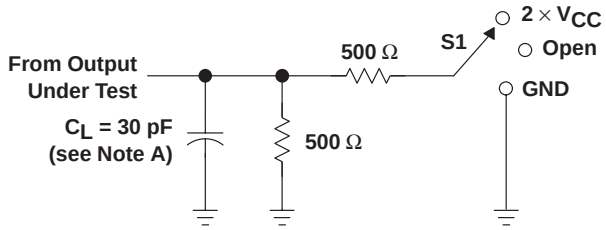
† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A					ns
t_{en}	S	A or B					ns
t_{dis}	S	A or B					ns
t_{en}	T	A or B					ns
t_{dis}	T	A or B					ns

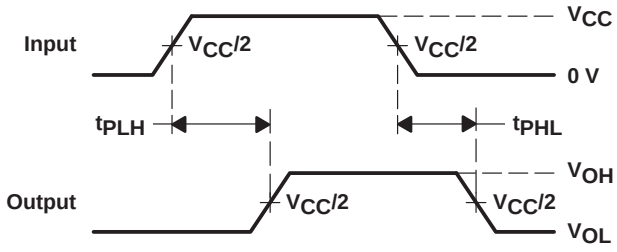
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

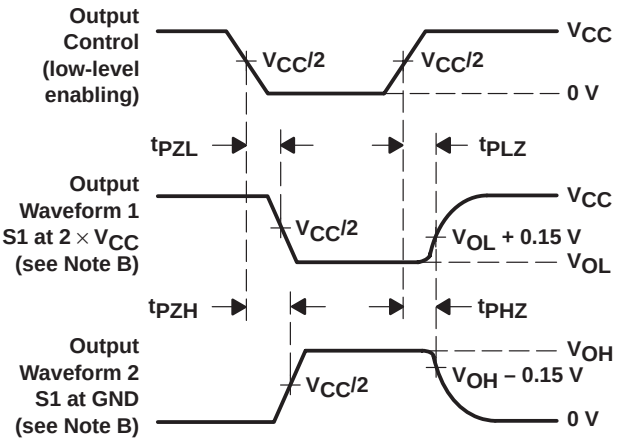


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



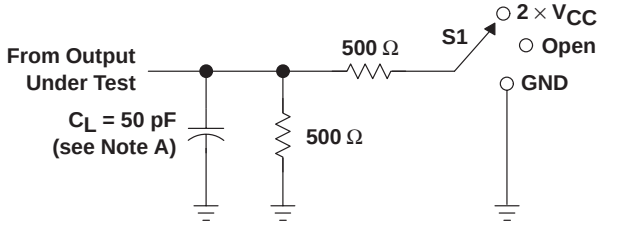
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

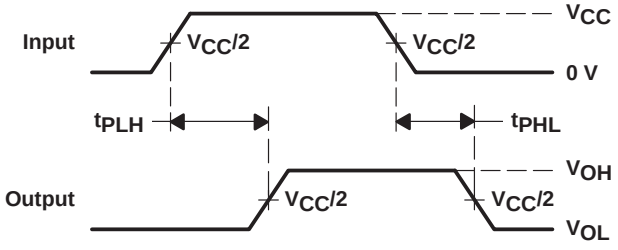
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3 V ± 0.3 V

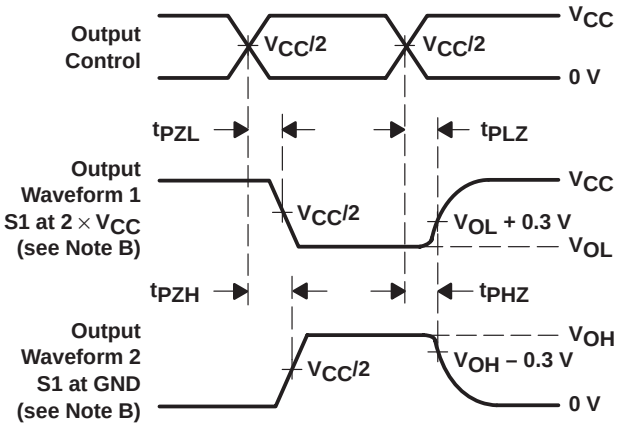


LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



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F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

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