SN74CBT16233
16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and Shrink Small-Outline (DL) Packages**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)

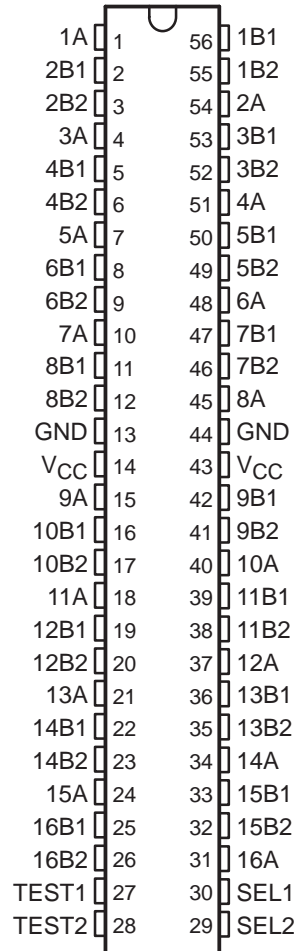|			
1A	1	56	1B1
2B1	2	55	1B2
2B2	3	54	2A
3A	4	53	3B1
4B1	5	52	3B2
4B2	6	51	4A
5A	7	50	5B1
6B1	8	49	5B2
6B2	9	48	6A
7A	10	47	7B1
8B1	11	46	7B2
8B2	12	45	8A
GND	13	44	GND
V_{CC}	14	43	V_{CC}
9A	15	42	9B1
10B1	16	41	9B2
10B2	17	40	10A
11A	18	39	11B1
12B1	19	38	11B2
12B2	20	37	12A
13A	21	36	13B1
14B1	22	35	13B2
14B2	23	34	14A
15A	24	33	15B1
16B1	25	32	15B2
16B2	26	31	16A
TEST1	27	30	SEL1
TEST2	28	29	SEL2

description

The SN74CBT16233 is a 16-bit 1-of-2 FET multiplexer/demultiplexer used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, where two different banks of memory need to be addressed simultaneously. The device can be used as two 8-bit to 16-bit multiplexers or as one 16-bit to 32-bit multiplexer.

Two select (SEL1 and SEL2) inputs control the data flow. When the TEST inputs are asserted, the A port is connected to both the B1 and the B2 ports. SEL1, SEL2, and the TEST inputs can be driven with a 5-V CMOS, a 5-V TTL, or a low-voltage TTL driver.

This device is designed so it does not have through current when switching directions.

The SN74CBT16233 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each multiplexer/demultiplexer)

INPUTS		FUNCTION
SEL	TEST	
L	L	A = B1
H	L	A = B2
X	H	A = B1 and A = B2

TEXAS INSTRUMENTS

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logic diagram (positive logic)
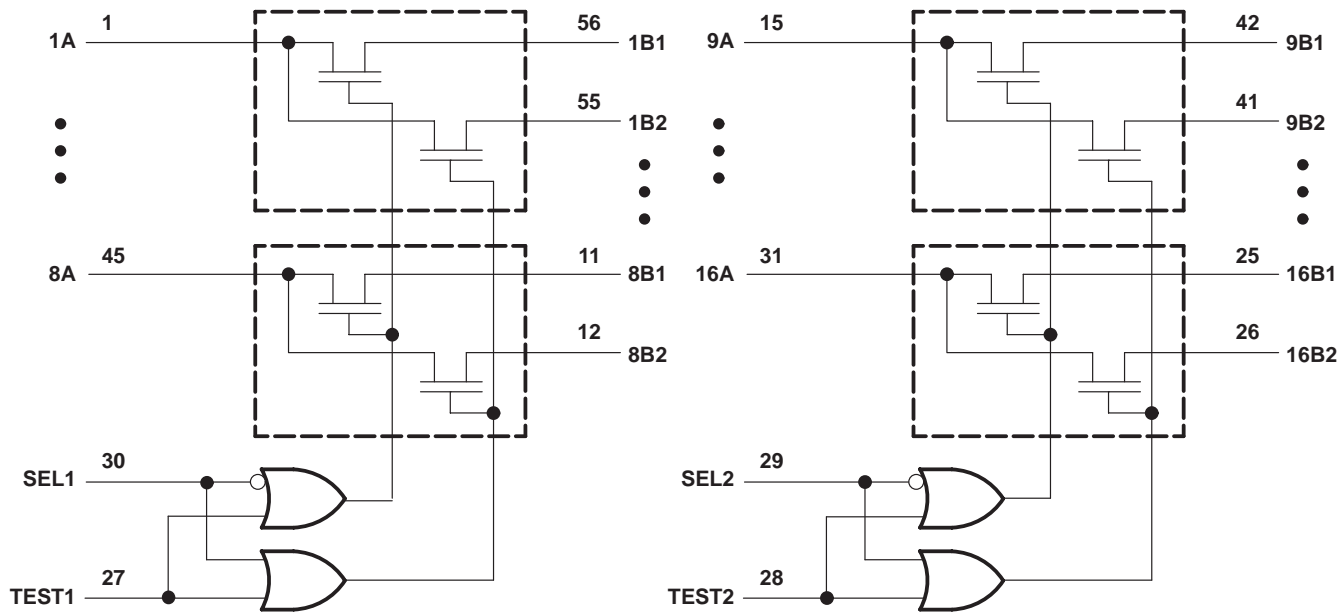
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Continuous channel current .... 128 mA
Input clamp current, I_{IK} (V_I < 0) .... –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package .... 64°C/W
DGV package .... 48°C/W
DL package .... 56°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	0	70	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		$V_{CC} = 4.75$ V,	$I_I = -18$ mA				−1.2	V
I_I		$V_{CC} = 0$,	$V_I = 5.25$ V				10	µA
		$V_{CC} = 5.25$ V,	$V_I = 5.25$ V or GND				±1	µA
I_{CC}		$V_{CC} = 5.25$ V,	$I_O = 0$,	$V_I = V_{CC}$ or GND			3	µA
ΔI_{CC}[‡]	Control inputs	$V_{CC} = 5.5$ V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	$V_I = 3$ V or 0				4.5		pF
$C_{io(OFF)}$		$V_O = 3$ V or 0				4		pF
r_{on}[§]		$V_{CC} = 4.75$ V	$V_I = 0$	$I_I = 64$ mA		5	7	Ω
				$I_I = 30$ mA		5	7	
			$V_I = 2.4$ V,	$I_I = 15$ mA		7	12	

[†] All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
[§] Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}[¶]	A or B	B or A		0.25	ns
t_{pd}	SEL	A	1.6	5.3	ns
t_{en}	TEST or SEL	B	1.3	5.2	ns
t_{dis}	TEST or SEL	B	1	5.3	ns

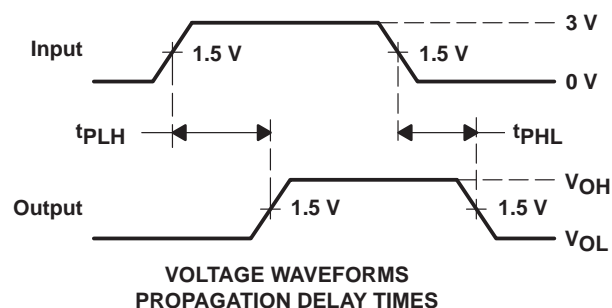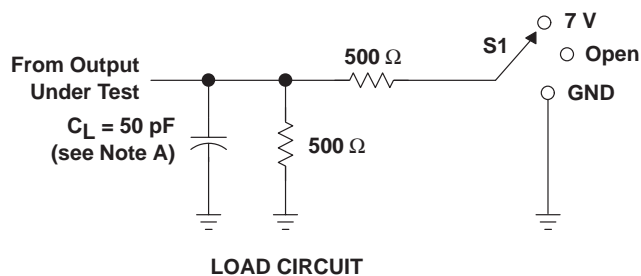[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
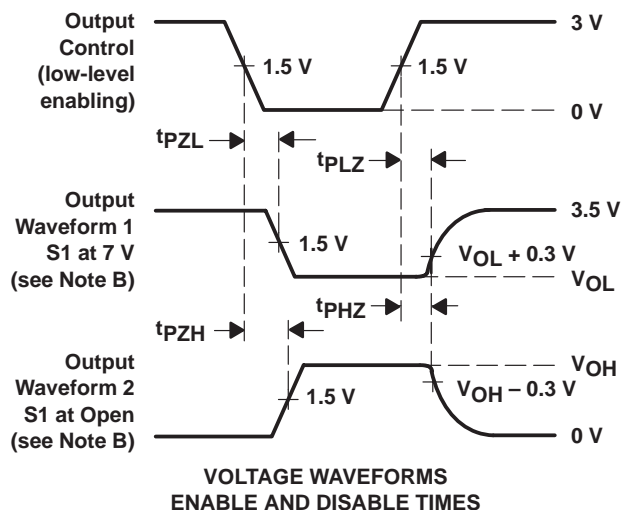
PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT

From Output Under Test
500 Ω
S1
7 V
Open
GND
C_L = 50 pF (see Note A)
500 Ω

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

Input — 1.5 V — 1.5 V — 3 V / 0 V
t_{PLH} — t_{PHL}
Output — 1.5 V — 1.5 V — V_{OH} / V_{OL}

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

Output Control (low-level enabling) — 1.5 V — 1.5 V — 3 V / 0 V
t_{PZL} — t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B) — 1.5 V — V_{OL} + 0.3 V — 3.5 V / V_{OL}
t_{PZH} — t_{PHZ}
Output Waveform 2 S1 at Open (see Note B) — 1.5 V — V_{OH} – 0.3 V — V_{OH} / 0 V

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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