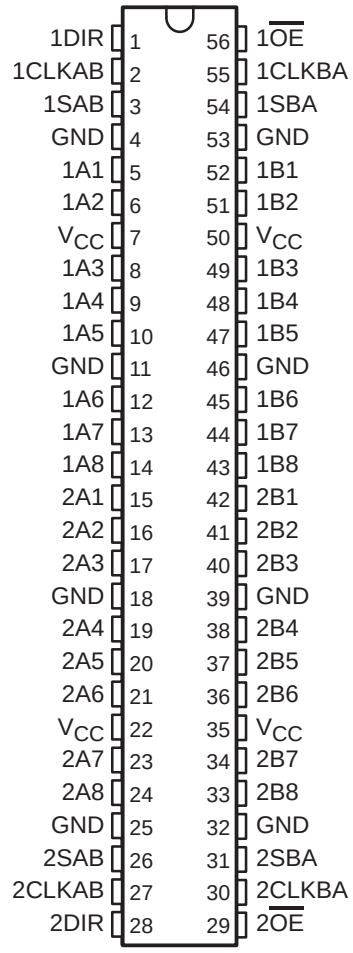
- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **Independent Registers for A and B Buses**
- **Inverting Data Path**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

54ACT16648 . . . WD PACKAGE
74ACT16648 . . . DL PACKAGE
(TOP VIEW)



description

The ’ACT16648 are 16-bit bus transceivers that consist of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 74ACT16648.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data can be stored in one register and/or B data can be stored in the other register.

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

The 74ACT16648 is packaged in TI’s shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

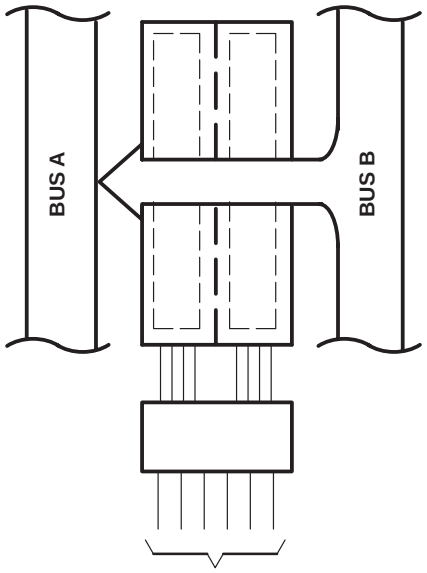
description (continued)

The 54ACT16648 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16648 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

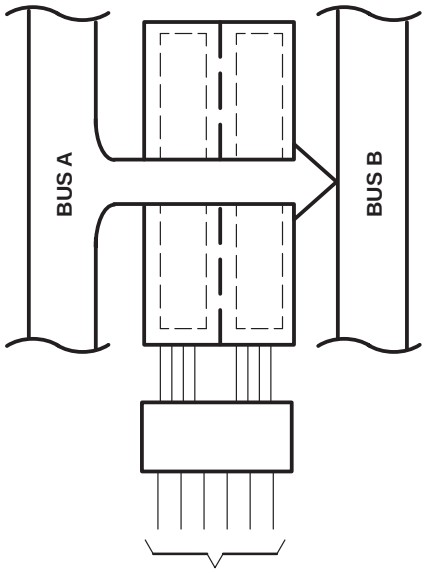
INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	L	X	H	Output	Input	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
L	H	L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus

† The data-output functions may be enabled or disabled by a variety of level combinations at $\overline{OE}$ and DIR. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.



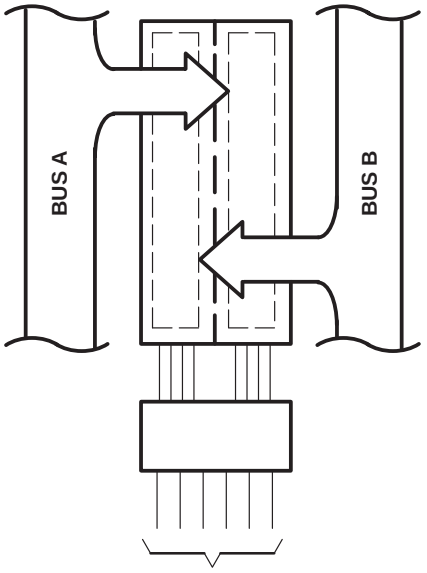
56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



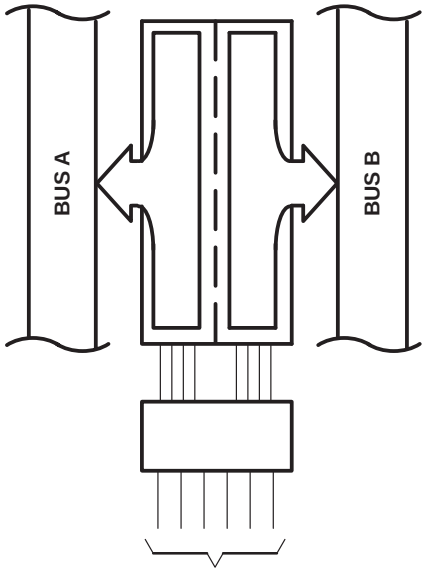
56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

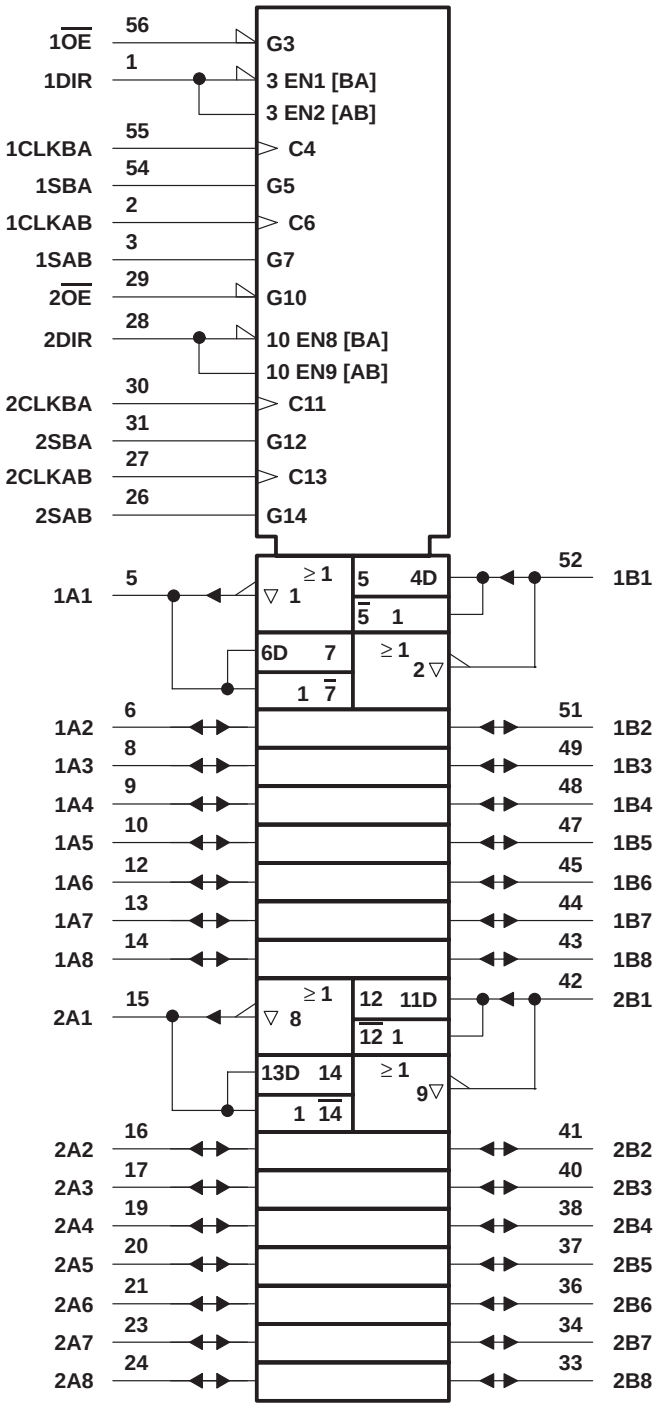


56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

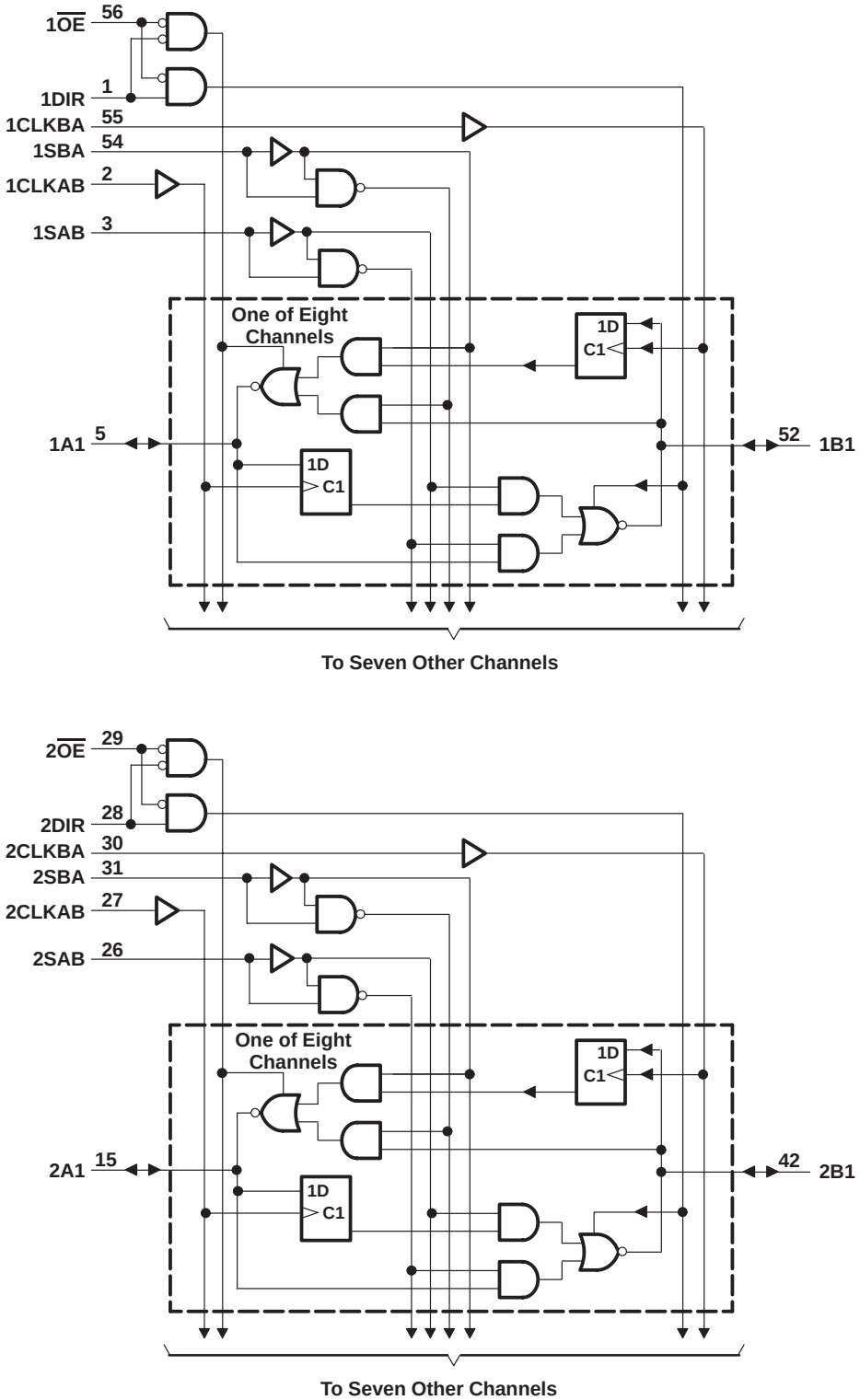
Figure 1. Bus-Management Functions

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±400 mA
Maximum package power dissipation at T_A = 55°C (in still air) (see Note 2): DL package . . . . . 1.4 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		54ACT16684			74ACT16684			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			–24			–24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16648		74ACT16648		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 µA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = –24 mA	4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
		I_{OH} = –75 mA†	5.5 V				3.85		3.85		
V_{OL}		I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65		1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80		80	µA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		54ACT16648		74ACT16648		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	75	0	75	0	75	MHz
t_w	Pulse duration, CLKAB or CLKBA high or low	6.5		6.5		6.5		ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	4.5		4.5		4.5		ns
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

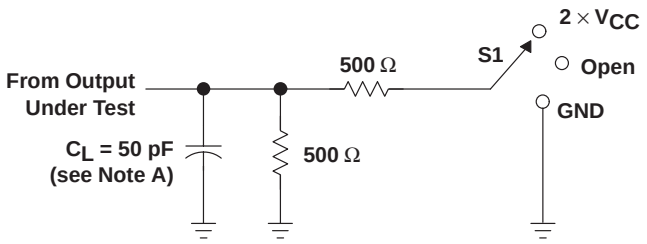
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16648		74ACT16648		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			75			75		75		MHz
t_{PLH}	A or B	B or A	2.4	7.2	9.8	2.4	11	2.4	11	ns
t_{PHL}			3.8	7.7	10.1	3.8	11.2	3.8	11.2	
t_{PZH}	$\overline{OE}$	A or B	2.9	7.9	10.7	2.9	12	2.9	12	ns
t_{PZL}			3.6	9.1	12.1	3.6	13.7	3.6	13.7	
t_{PHZ}	$\overline{OE}$	A or B	5.2	8.1	9.7	5.2	10.4	5.2	10.4	ns
t_{PLZ}			4.7	7.3	9.1	4.7	9.9	4.7	9.9	
t_{PLH}	CLKBA or CLKAB	A or B	4.4	8.5	11.3	4.4	12.7	4.4	12.7	ns
t_{PHL}			4.6	8.8	11.4	4.6	12.7	4.6	12.7	
t_{PLH}	SBA or SAB† (with A or B high)	A or B	3.8	7.5	10	3.8	11.3	3.8	11.3	ns
t_{PHL}			5.1	11.4	12.7	5.1	16.6	5.1	16.6	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	4.5	10.6	13.9	4.5	15.8	4.5	15.8	ns
t_{PHL}			4.3	8.3	10.8	4.3	11.9	4.3	11.9	
t_{PZH}	DIR	A or B	2.8	7.8	10.7	2.8	11.9	2.8	11.9	ns
t_{PZL}			3.7	9.3	12.2	3.7	13.7	3.7	13.7	
t_{PHZ}	DIR	A or B	4.6	8.6	10.9	4.6	11.5	4.6	11.5	ns
t_{PLZ}			4	7.4	9.7	4	10.4	4	10.4	

† These parameters are measured with the internal output state of the storage registers opposite that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

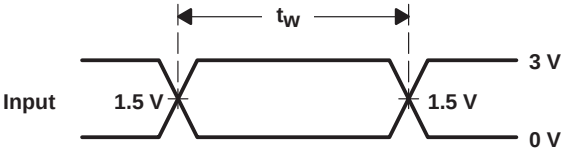
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	63	pF
		Outputs disabled		14	

PARAMETER MEASUREMENT INFORMATION

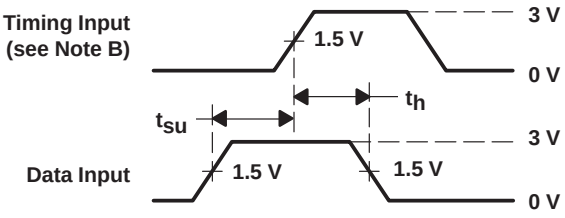


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

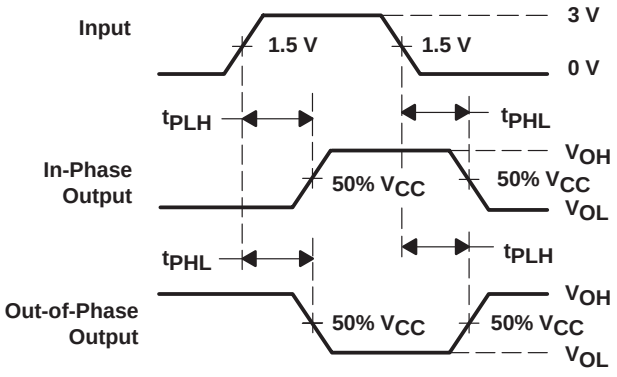
LOAD CIRCUIT



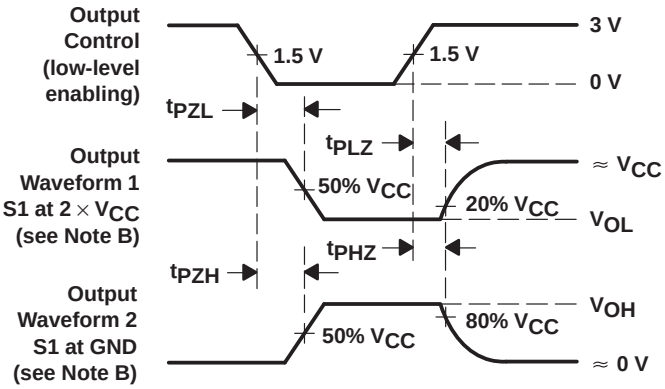
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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