256-word×4-bit parallel NON-VOLATILE RAM

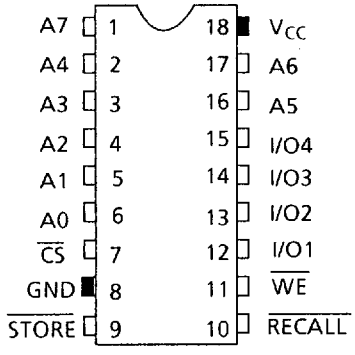
The S-22S12R/I is a non-volatile CMOS RAM, composed of a CMOS static RAM and a non-volatile electrically erasable programmable memory (E²PROM) to backup the SRAM. The organization is 256-word × 4-bit (total 1024 bits) and the RAM is asynchronously CMOS static. The pin layout is compatible with X2212 of Xicor Ltd.
When a store signal is input to the SRAM, all the data is copied into the E²PROM. When a recall signal is input, the E²PROM data is recopied into the SRAM.

■ Features

- Low current consumption
  Operating : 10 mA typ.
  Standby : 1 μA max.
- All inputs and outputs except $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ are compatible with TTL
- +5-V single power supply (+5 V ± 10%)
- Completely static operation
- Access time: 200 ns max.
- CMOS floating gate process
- Tri-state output
- $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ are controlled by a short pulse width: 200 ns min.
- E²PROM store cycles: $10^4/10^5$ times
- E²PROM memory retention: 10 years
- Erroneous store protection: ≃ 3.5 V
- 18-pin DIP/SOP

■ Pin Arrangement

18-pin DIP/SOP
Top view



A0 to A7	Address input
I/O1 to I/O4	Data input/output
$\overline{\text{WE}}$	Write enable
$\overline{\text{CS}}$	Chip select
$\overline{\text{RECALL}}$	Recall
$\overline{\text{STORE}}$	Store
V_{CC}	Power supply voltage (+5 V)
GND	Ground (0 V)

Figure 1

■ Block Diagram

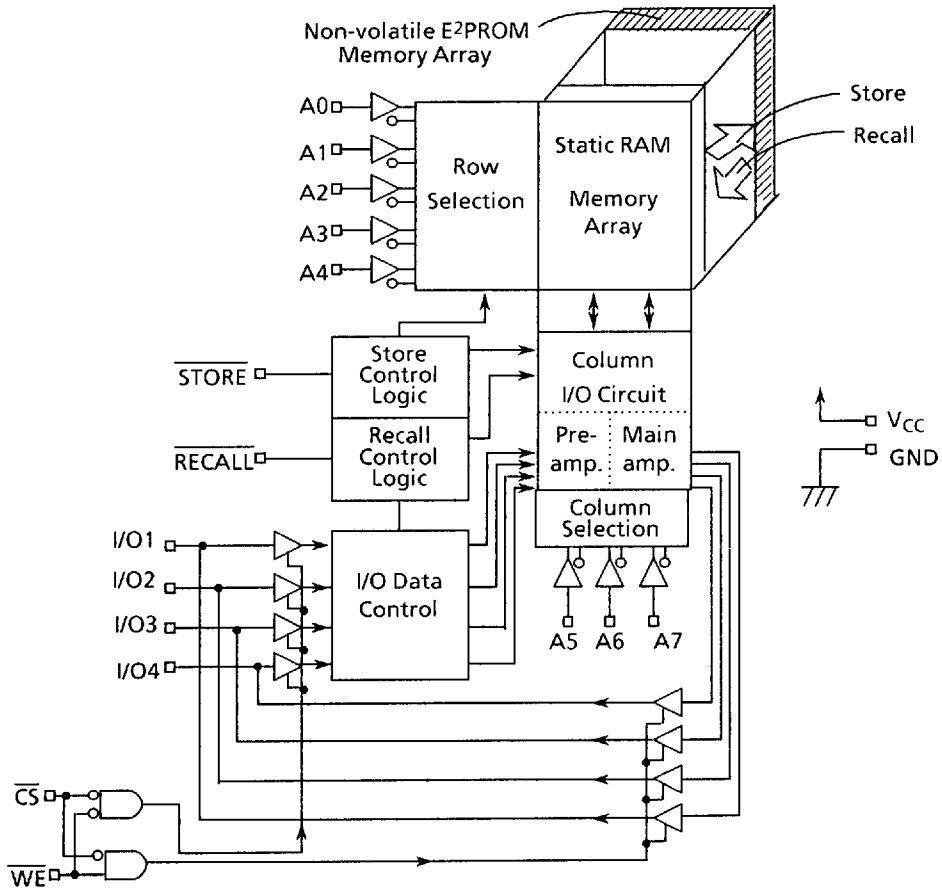


Figure 2

■ Absolute Maximum Ratings

Table 1

Item	Symbol	Condition	Ratings	Unit
Storage temperature	T_{stg}	S-22S12R	-65 to + 125	°C
		S-22S12I	-65 to + 150	°C
Storage temperature under bias	T_{bias}	S-22S12R	-10 to + 85	°C
		S-22S12I	-50 to + 95	°C
Power supply voltage	V_{CC}		-0.3 to + 6.0	V
Input voltage	V_{IN}		-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}		0.0 to V_{CC}	V

■ Recommended Operating Conditions

Table 2

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage 1	V_{IH1}	$\overline{CS}$, $\overline{WE}$, I/O, A0 to A7	2.0	—	V_{CC}	V
High level input voltage 2	V_{IH2}	$\overline{STORE}$, $\overline{RECALL}$	3.4	—	V_{CC}	V
Low level input voltage 1	V_{IL1}	$\overline{CS}$, $\overline{WE}$, I/O, A0 to A7	0.0	—	0.8	V
Low level input voltage 2	V_{IL2}	$\overline{STORE}$, $\overline{RECALL}$	0.0	—	0.8	V
Operating temperature	T_{opr}	S-22S12R	0	—	+70	°C
		S-22S12I	−40	—	+85	°C

■ DC Electrical Characteristics

Table 3

(S-22S12R : Ta = 0°C to +70°C, V_{CC} = +5V ± 10%
S-22S12I : Ta = -40°C to +85°C, V_{CC} = +5V ± 10%)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating current consumption	I_{CC}	S-22S12R	—	10	20	mA
		S-22S12I	—	10	30	mA
Standby current consumption	I_{SB}	$\overline{CS}$ = V_{CC} Other inputs are V_{CC} or GND	—	—	1	μA
Inputs leakage current	I_{LI}	V_{IN} = GND to V_{CC}	—	0.1	1	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	—	0.1	1	μA
High level output voltage	V_{OH}	TTL I_{OH} = -2 mA	2.4	—	—	V
		CMOS I_{OH} = -100 μA	V_{CC}-0.1	—	—	V
Low level output voltage	V_{OL}	TTL I_{OL} = 4.2 mA	—	—	0.4	V
		CMOS I_{OL} = 100 μA	—	—	0.1	V
Store inhibition voltage	V_{WI}	S-22S12R	—	3.5	4.0	V
		S-22S12I	—	3.5	4.1	V
Schmitt width	V_{WD}	$\overline{RECALL}$, $\overline{STORE}$	0.4	—	—	V

■ Data Hold Characteristics

Table 4

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data hold voltage	V_{DH}	$\overline{CS} \geqq V_{CC} - 0.2V$, $\overline{RECALL} \geqq V_{CC}-0.2V$	1.5	—	5.5	V
Data hold setup time	t_{CDH}		50	—	—	ns
Recovery time	t_R		300	—	—	ns

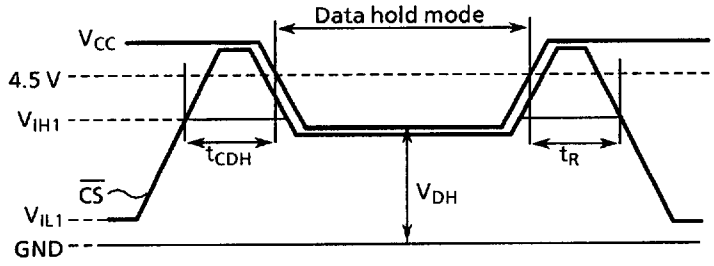


Figure 3

■ Capacitance

Table 5

($Ta = 25°C$, $f = 1.0$ MHz, $V_{CC} = 5$ V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0$ V	—	—	6	pF
Output capacitance (I/O pin)	$C_{I/O}$	$V_{I/O} = 0$ V	—	—	10	pF

■ AC Electrical Characteristics

Table 6 Measurement conditions

Item	Conditions	S-22S12R	S-22S12I	Unit
Input pulse voltage	$\overline{CS}$, $\overline{WE}$, I/O, A0 to A7	0.65 to 2.2	0.0 to 3.0	V
	$\overline{STORE}$, $\overline{RECALL}$	0.0 to 4.0	0.0 to 4.0	V
Input pulse rise/fall time		10	10	ns
I/O reference voltage		1.5	1.5	V
Output load		1TTL + 100pF	1TTL + 100pF	

1. Read cycle

Table 7

Item	Symbol	Min.	Typ.	Max.	Unit
Read cycle time	t_{RC}	200	—	—	ns
Address access time	t_{AA}	—	—	200	ns
$\overline{CS}$ access time	t_{CS}	—	—	200	ns
Output data hold time	t_{OH}	20	—	—	ns
Output enable time ($\overline{CS}$)	t_{CLZ}	10	—	—	ns
Output disable time ($\overline{CS}$)	t_{CHZ}	10	—	70	ns

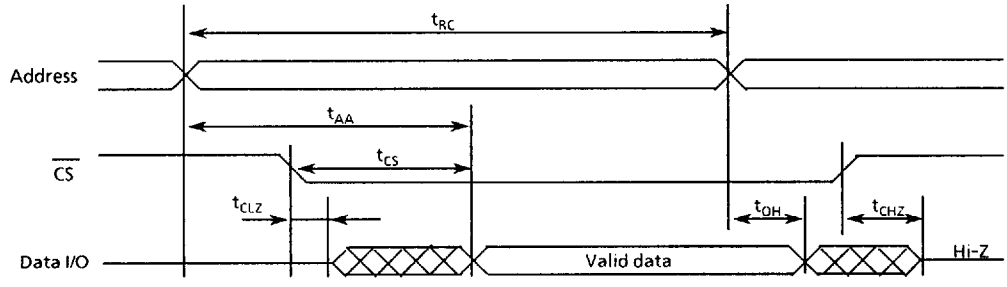


Figure 4

2. Write cycle

Table 8

Item	Symbol	Min.	Typ.	Max.	Unit
Write cycle time	t_{WC}	200	—	—	ns
$\overline{CS}$ pulse width	t_{CW}	120	—	—	ns
Address setup time	t_{AS}	20	—	—	ns
$\overline{WE}$ pulse width	t_{WP}	120	—	—	ns
Write reset time	t_{WR}	25	—	—	ns
Input data setup time	t_{DW}	50	—	—	ns
Input data hold time	t_{DH}	20	—	—	ns
Output disable time ($\overline{WE}$)	t_{WHZ}	10	—	70	ns
Output enable time ($\overline{WE}$)	t_{WLZ}	10	—	—	ns

· Write cycle 1 : $\overline{WE}$ control

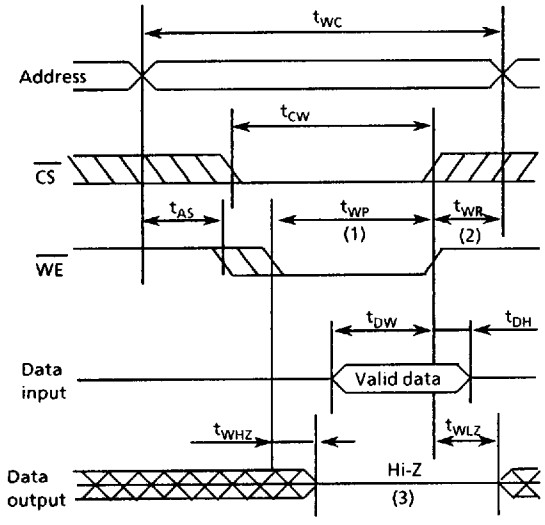


Figure 5

· Write cycle 2 : $\overline{CS}$ control

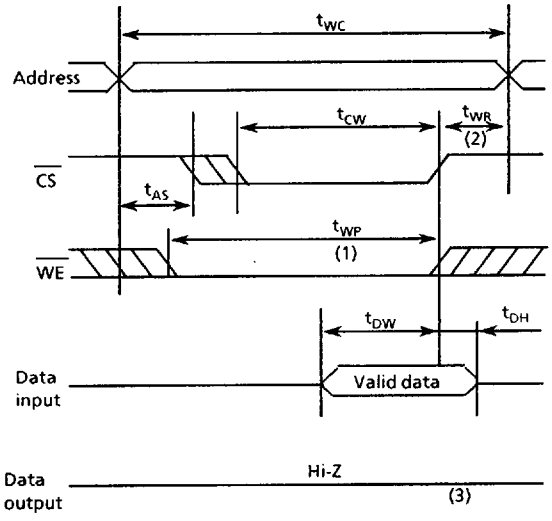


Figure 6

(1) The write cycle starts when both $\overline{CS}$ and $\overline{WE}$ are low.

(2) t_{WR} is the period of time from the rise of $\overline{CS}$ or $\overline{WE}$ whichever is the first to the end of write cycle.

(3) Output remains in high-impedance state when $\overline{CS}$ falls simultaneously with or after the fall of $\overline{WE}$.

3. Store cycle

Table 9

Item	Symbol	Min.	Typ.	Max.	Unit
Store time	t_{ST}	—	—	10	ms
Store pulse width	t_{STP}	200	—	—	ns
Store disable time	t_{STZ}	—	—	100	ns
Store enable time	t_{OST}	10	—	—	ns

Store operation starts at the falling of $\overline{\text{STORE}}$.

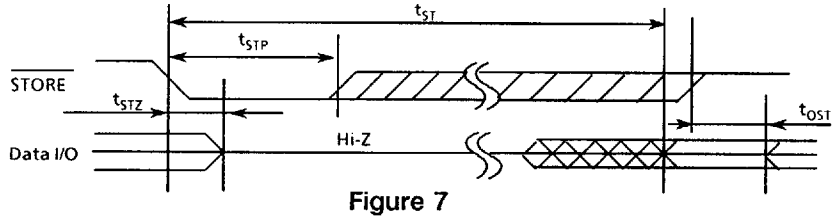


Figure 7

4. Recall cycle

Table 10

Item	Symbol	Min.	Typ.	Max.	Unit
Recall cycle time	t_{RCC}	1300	1000	—	ns
Recall pulse width	t_{RCP}	200	—	—	ns
Recall disable time	t_{RCZ}	—	—	100	ns
Recall enable time	t_{ORC}	10	—	—	ns
Recall data access time	t_{ARC}	—	—	1100	ns

Recall operation starts at the rise of $\overline{\text{RECALL}}$.
It can be repeated without limitation.

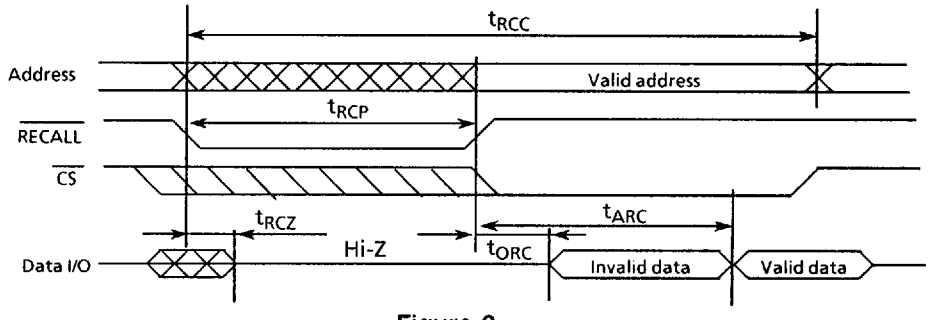


Figure 8

■ Operation Mode

Table 11

Mode	Input				Input/Output
	$\overline{CS}$	$\overline{WE}$	$\overline{RECALL}$	$\overline{STORE}$	
Standby mode	H	X	H	H	Output is high impedance
Read mode	L	H	H	H	Output data
Write mode	L	L	H	H	Input data
Recall mode	X	H	L	H	Output is high impedance
	H	X	L	H	
Store mode	X	H	H	L	Output is high impedance
	H	X	H	L	

X : don't care

Notes: · When $\overline{RECALL}$ and $\overline{STORE}$ are simultaneously input, $\overline{RECALL}$ is valid.
· When $\overline{RECALL}$ is low, $\overline{STORE}$ cannot be received.
· When power supply voltage (V_{CC}) is below store inhibition voltage V_{WI}, the store operation is inhibited.

■ Operation

1. Standby mode

When $\overline{CS}$ goes high, the S-22S12R/I enters into the standby mode: power consumption becomes lowest, and I/O1 to I/O4 are high impedance.

2. SRAM modes

2.1 Read mode

When $\overline{CS}$ is low and $\overline{WE}$ is high, the S-22S12R/I enters into the read mode: the SRAM data is output to I/O1 to I/O4.

2.2 Write mode

When $\overline{CS}$ and $\overline{WE}$ are low, the S-22S12R/I enters into the write mode: the data input in I/O1 to I/O4 is written to the SRAM.

3. SRAM⇆E²PROM mode

3.1 Store mode

When $\overline{\text{STORE}}$ goes V_{IL2}, the S-22S12R/I enters into the store mode: the SRAM data is copied to the E²PROM. The original data in the SRAM is effective. Since the copied data in the E²PROM is non-volatile, they are retained even if power turns off. When $\overline{\text{STORE}}$ falls, the store operation starts and finishes automatically. When store operation starts, I/O1 to I/O4 go to high impedance and other operations are inhibited until store operation is finished and $\overline{\text{STORE}}$ goes to high. During store operation, the CPU can access other instructions.

The store operation is inhibited if power supply voltage (V_{CC}) is under V_{WI} (≃ 3.5 V.)

The following two methods prevent erroneous store, caused by noise when power turns on or off:

- $\overline{\text{RECALL}}$ goes V_{IL2} when power turns on or off (see Figure 9).
- $\overline{\text{STORE}}$ connects to V_{CC} with pull-up resistor.

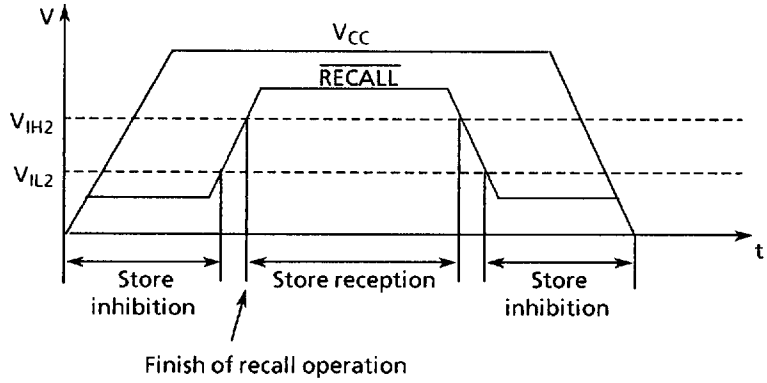


Figure 9 STORE inhibition period and reception period at power ON and OFF

3.2 Recall mode

When $\overline{\text{RECALL}}$ goes V_{IL2}, the S-22S12R/I enters into the recall mode: the data copied into the E²PROM is recopied to the SRAM. The recopied data can be read or written as SRAM data. Even if the data is copied repeatedly, the data in the E²PROM does not change. Other operations are inhibited during its operation.

■ Dimensions

1. S-22S12R/I (18-pin DIP)

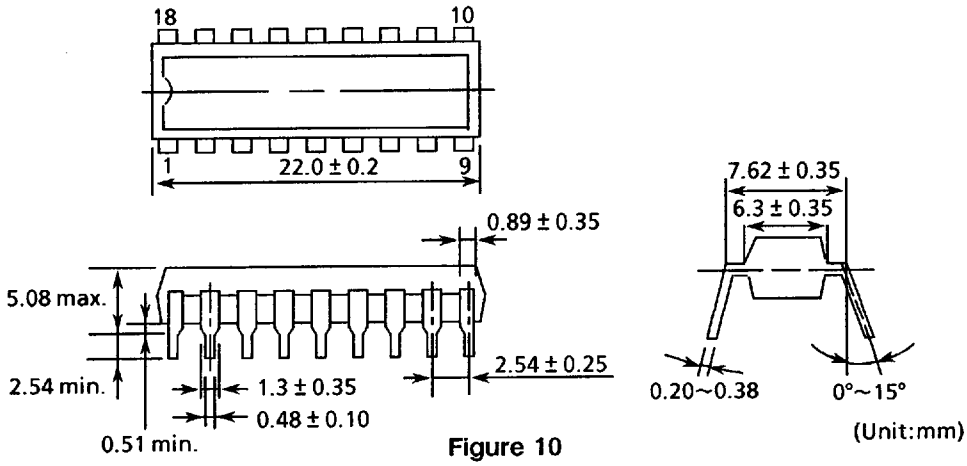


Figure 10

2. S-22S12RF/IF (18-pin SOP)

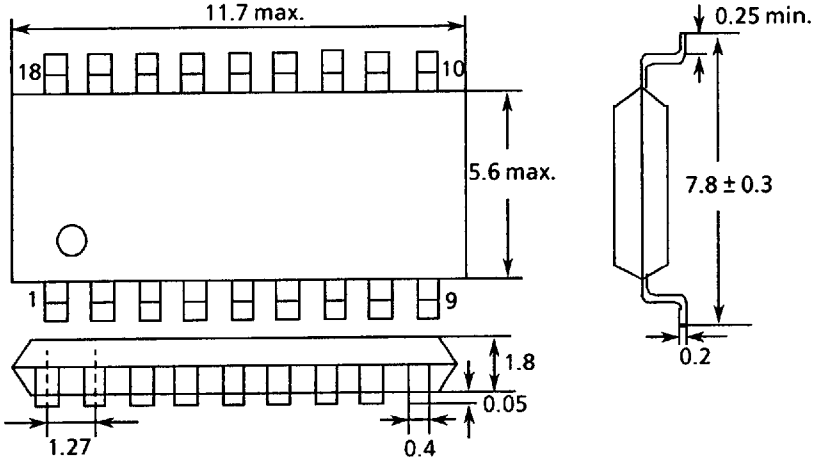


Figure 11

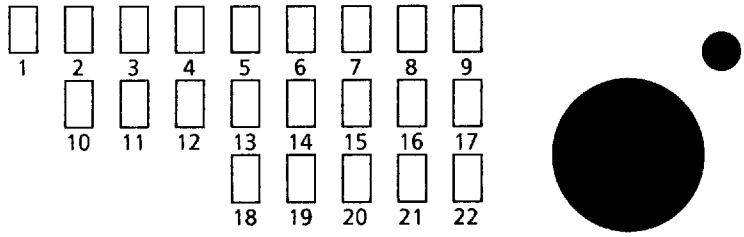
■ Ordering Information

Table 12

Product name	Store cycles	Store cycles per bit	Temperature	Package
S-22S12R 01/10	$10^4/10^5$	$10^4/10^5$	0°C to + 70°C	Plastic DIP
S-22S12I 01/10	$10^4/10^5$	$10^4/10^5$	– 40°C to + 85°C	Plastic DIP
S-22S12RF 01/10	$10^4/10^5$	$10^4/10^5$	0°C to + 70°C	Plastic SOP
S-22S12IF 01/10	$10^4/10^5$	$10^4/10^5$	– 40°C to + 85°C	Plastic SOP

■ Markings

1. S-22S12R/I (18-pin DIP)



1 to 9 : Product name

10 : Assembly code

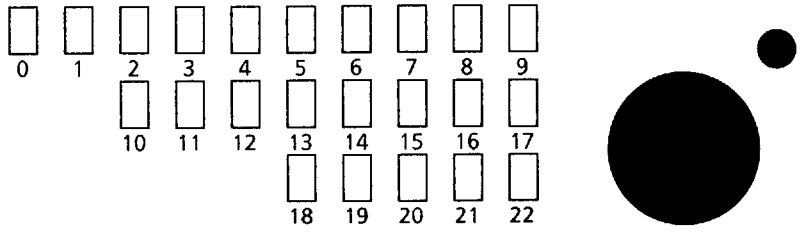
11 : Year of manufacturing (last digit)

12 : Month of manufacturing : January = 1, February = 2, March = 3, April = 4, May = 5, June = 6, July = 7, August = 8, September = 9, October = X, November = Y, December = Z

13 to 17 : Lot No.

18 to 22 : 『JAPAN』

2. S-22S12RF/IF (18-pin SOP)



0 to 9 : Product name

10 : Assembly code

11 : Year of manufacturing (last digit)

12 : Month of manufacturing : January = 1, February = 2, March = 3, April = 4, May = 5, June = 6, July = 7, August = 8, September = 9, October = X, November = Y, December = Z

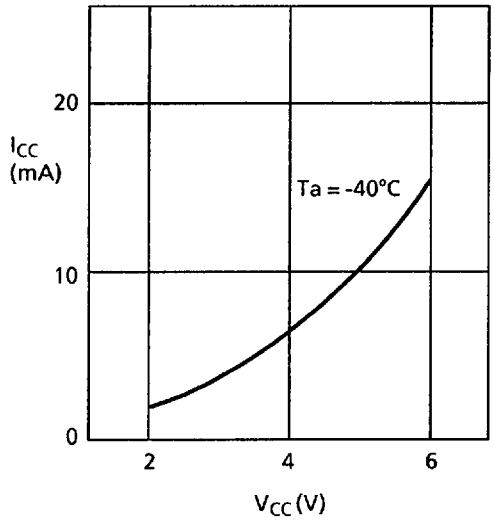
13 to 17 : Lot No.

18 to 22 : 『JAPAN』

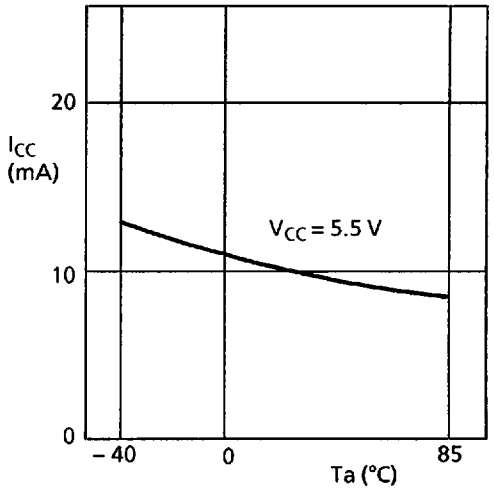
■ Characteristics

1. DC characteristics

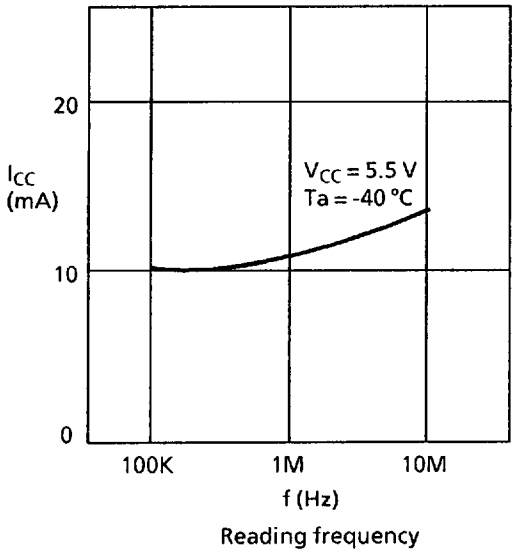
1.1 Operating current consumption I_{CC}
— Power supply voltage V_{CC}



1.2 Operating current consumption I_{CC}
— Ambient temperature Ta

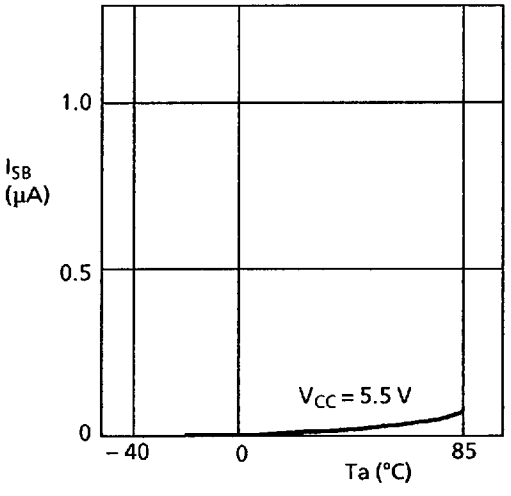


1.3 Operating current consumption I_{CC}
— Reading frequency

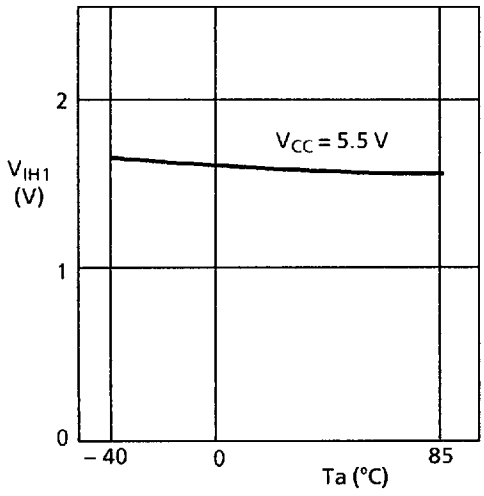


Reading frequency

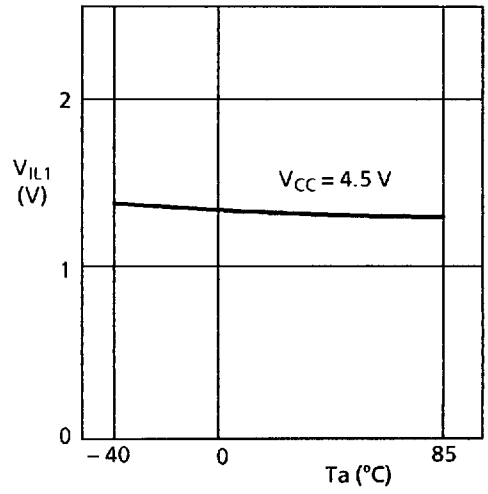
1.4 Standby current consumption I_{SB}
— Ambient temperature Ta



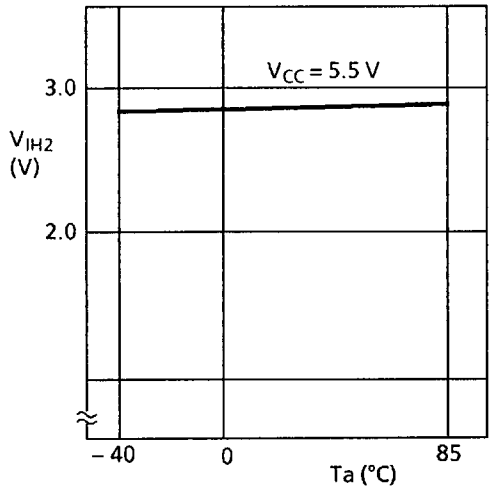
1.5 High level input voltabe V_{IH1} — Ambient temperature Ta



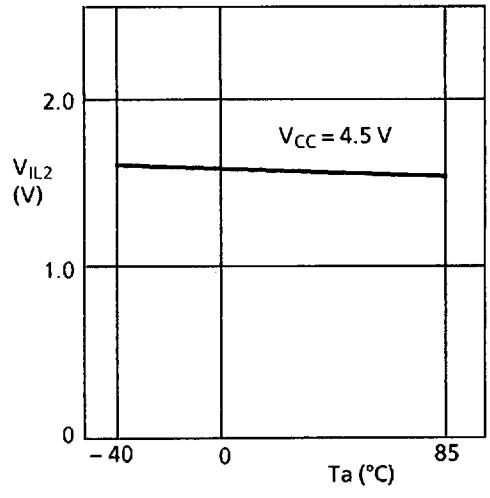
1.6 Low level input voltage V_{IL1} — Ambient temperature Ta



1.7 High level input voltabe V_{IH2} — Ambient temperature Ta

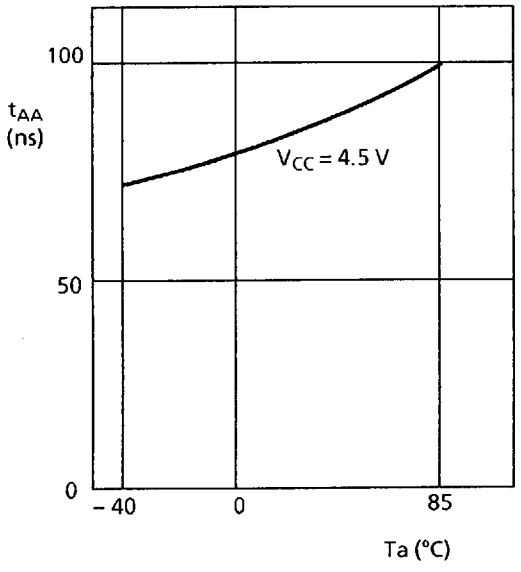


1.8 Low level input voltage V_{IL2} — Ambient temperature Ta

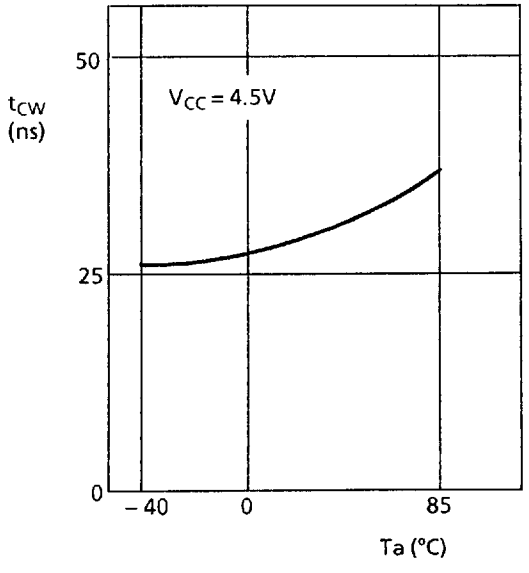


2. AC Characteristics

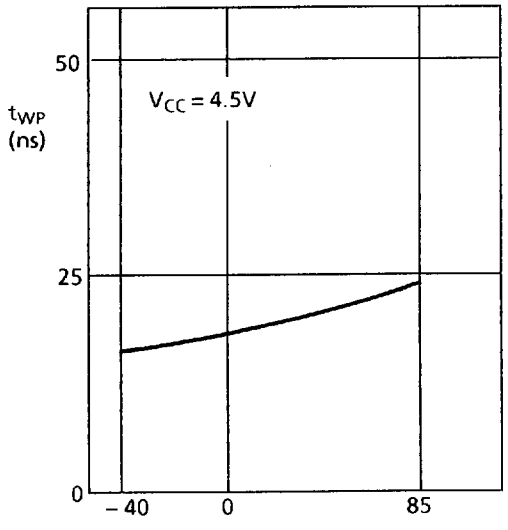
2.1 Address access time t_{AA} — Ambient temperature Ta



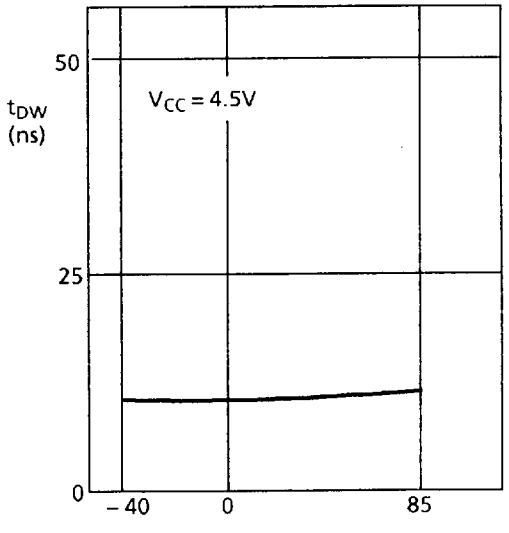
2.2 $\overline{CS}$ pulse width t_{CW} — Ambient temperature Ta



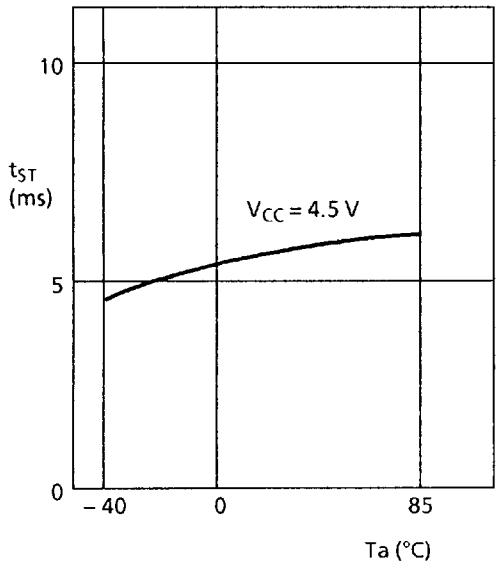
2.3 $\overline{WE}$ pulse width t_{WP} — Ambient temperature Ta



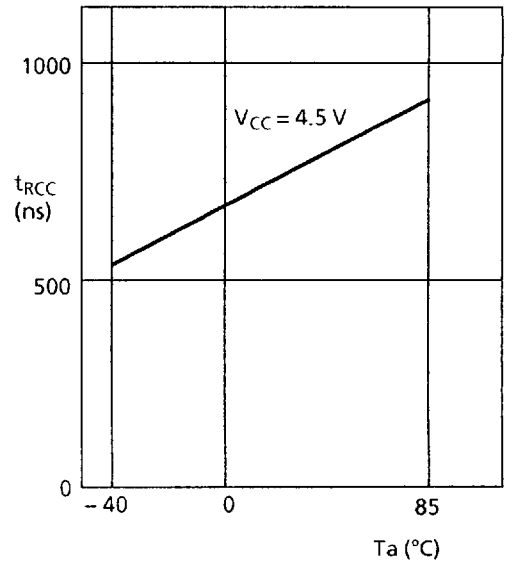
2.4 Input data setup time t_{DW} — Ambient temperature Ta



2.5 Store time t_{ST} — Ambient temperature Ta



2.6 Recall cycle time t_{RCC} — Ambient temperature Ta



3. Store Characteristic