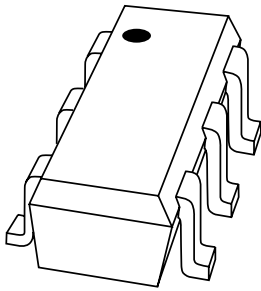


DATA SHEET



PUMD9 NPN/PNP resistor-equipped transistors

Product specification
Supersedes data of 1999 May 20

2001 Feb 16

NPN/PNP resistor-equipped transistors

PUMD9

FEATURES

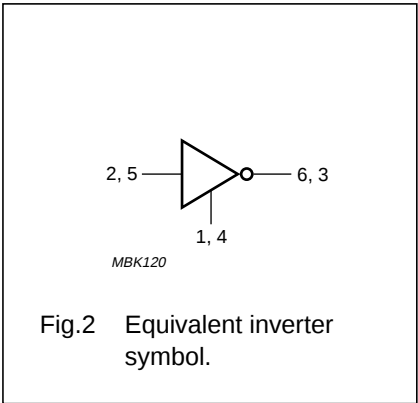
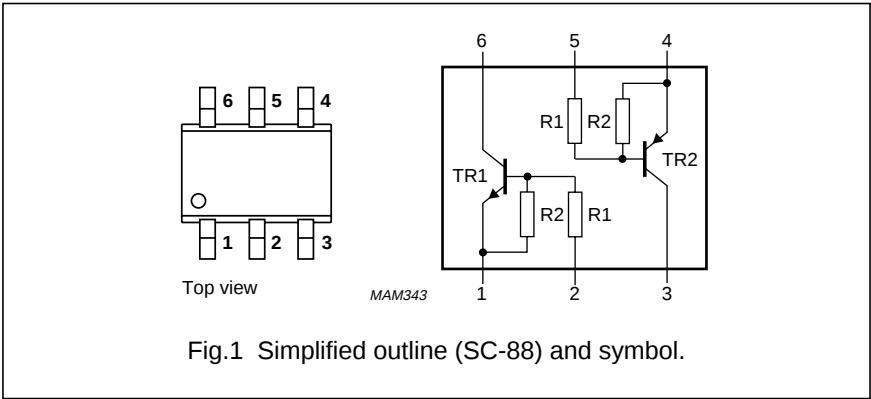
- Transistors with different polarity and built-in bias resistors
 - TR1 (NPN):
R1 = 10 kΩ; R2 = 47 kΩ
 - TR2 (PNP):
R1 = 10 kΩ; R2 = 47 kΩ
- No mutual interference between the transistors
- Simplification of circuit design
- Reduces number of components and board space.

APPLICATIONS

- Especially suitable for space reduction in portable equipment
- Inverter circuit configurations without use of external resistors.

DESCRIPTION

NPN/PNP resistor-equipped transistors in an SC-88 (SOT363) plastic package.



PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2

MARKING

TYPE NUMBER	MARKING CODE
PUMD9	Dt9

NPN/PNP resistor-equipped transistors

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity					
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	50	V
V_{EBO}	emitter-base voltage	open collector	–	10	V
V_i	input voltage				
	positive		–	+40	V
	negative		–	–6	V
I_o	output current (DC)		–	100	mA
I_{CM}	peak collector current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C
Per device					
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	300	mW

Note

1. Refer to SC-88 standard mounting conditions.

NPN/PNP resistor-equipped transistors

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	416	K/W

Note

1. Refer to SC-88 standard mounting conditions.

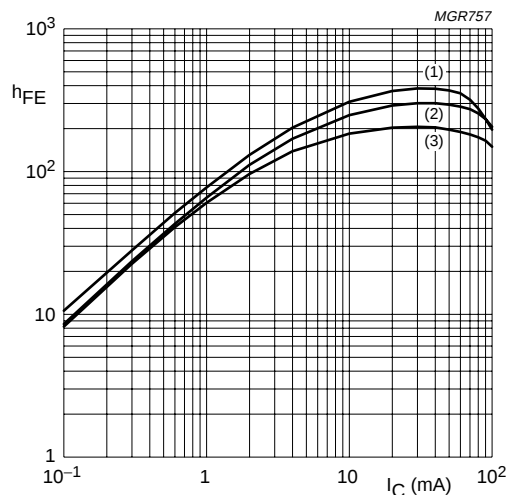
CHARACTERISTICS

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector cut-off current	$I_C = 0; V_{CB} = 50\text{ V}$	–	–	100	nA
I_{CEO}	collector cut-off current	$I_B = 0; V_{CE} = 30\text{ V}$	–	–	1	μA
		$I_B = 0; V_{CE} = 30\text{ V}; T_j = 150\text{ °C}$	–	–	50	μA
I_{EBO}	emitter cut-off current	$I_C = 0; V_{EB} = 5\text{ V}$	–	–	150	μA
h_{FE}	DC current gain	$I_C = 5\text{ mA}; V_{CE} = 5\text{ V}$	100	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 5\text{ mA}; I_B = 0.25\text{ mA}$	–	–	100	mV
$V_{i(off)}$	input-off voltage	$I_C = 100\text{ }\mu\text{A}; V_{CE} = 5\text{ V}$	–	0.7	0.5	V
$V_{i(on)}$	input-on voltage	$I_C = 1\text{ mA}; V_{CE} = 0.3\text{ V}$	1.4	0.8	–	V
$R1$	input resistor		7	10	13	k Ω
$\frac{R2}{R1}$	resistor ratio		3.7	4.7	5.7	
C_c	collector capacitance	$I_E = I_e = 0; V_{CB} = 10\text{ V}; f = 1\text{ MHz}$				
	TR1 (NPN)		–	–	2.5	pF
	TR2 (PNP)		–	–	3	pF

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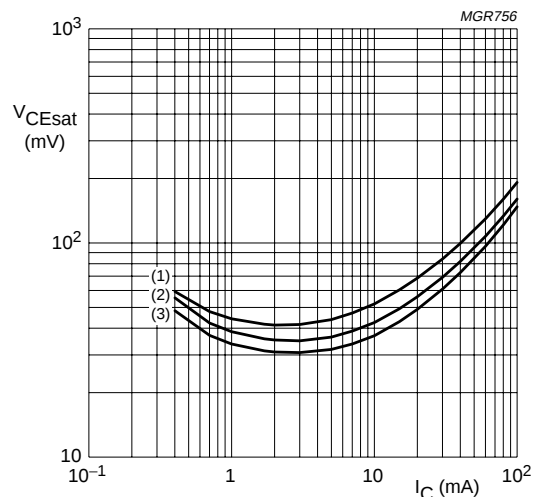
TR1 (NPN); $V_{CE} = 5$ V.

(1) $T_{amb} = 100$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = -40$ °C.

Fig.3 DC current gain as a function of collector current; typical values.



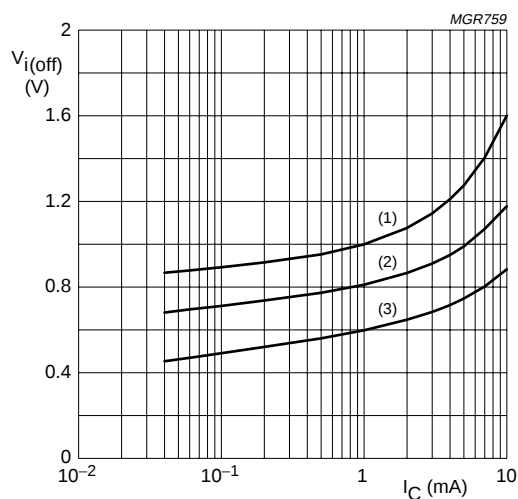
TR1 (NPN); $I_C/I_B = 20$.

(1) $T_{amb} = 100$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = -40$ °C.

Fig.4 Collector-emitter saturation voltage as a function of collector current; typical values.



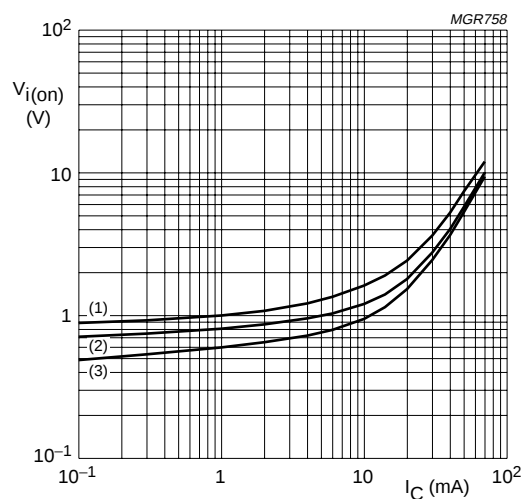
TR1 (NPN); $V_{CE} = 5$ V.

(1) $T_{amb} = -40$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = 100$ °C.

Fig.5 Input-off voltage as a function of collector current; typical values.



TR1 (NPN); $V_{CE} = 0.3$ V.

(1) $T_{amb} = -40$ °C.

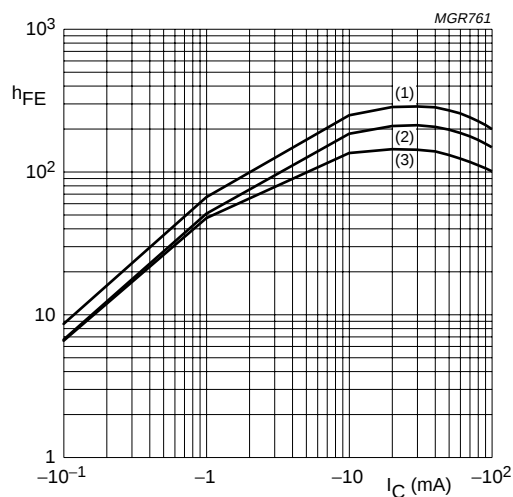
(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = 100$ °C.

Fig.6 Input-on voltage as a function of collector current; typical values.

NPN/PNP resistor-equipped transistors

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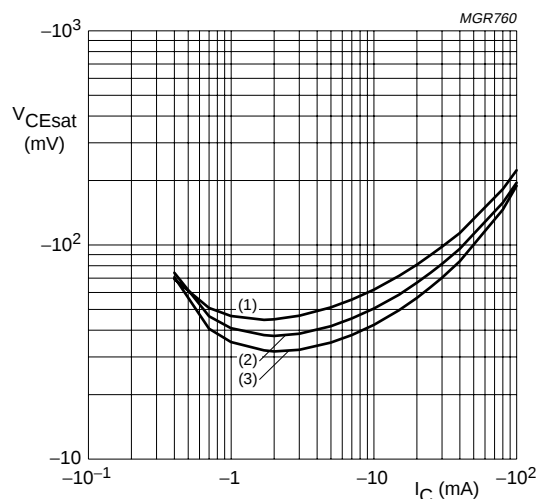
TR2 (PNP); $V_{CE} = -5$ V.

(1) $T_{amb} = 100$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = -40$ °C.

Fig.7 DC current gain as a function of collector current; typical values.



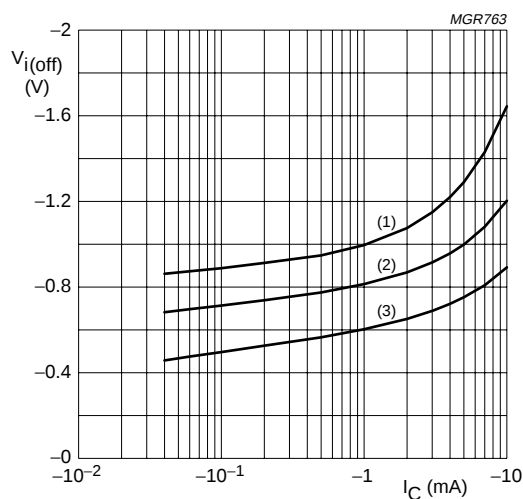
TR2 (PNP); $I_C/I_B = 20$.

(1) $T_{amb} = 100$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = -40$ °C.

Fig.8 Collector-emitter saturation voltage as a function of collector current; typical values.



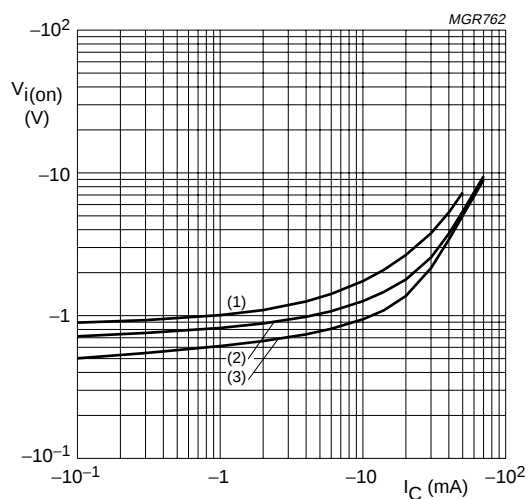
TR2 (PNP); $V_{CE} = -5$ V.

(1) $T_{amb} = -40$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = 100$ °C.

Fig.9 Input-off voltage as a function of collector current; typical values.



TR2 (PNP); $V_{CE} = -0.3$ V.

(1) $T_{amb} = -40$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = 100$ °C.

Fig.10 Input-on voltage as a function of collector current; typical values.

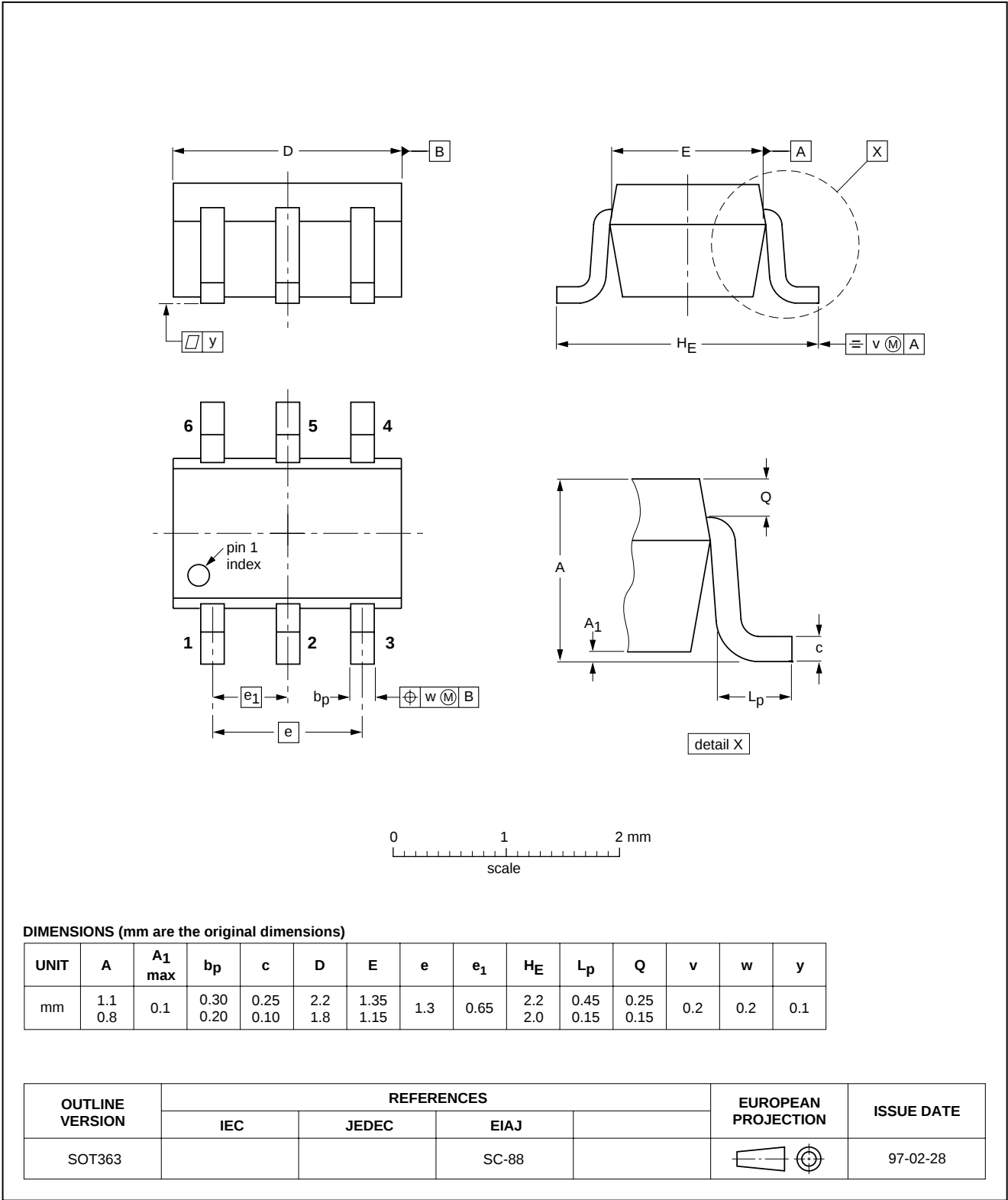
NPN/PNP resistor-equipped transistors

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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



NPN/PNP resistor-equipped transistors

PUMD9

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS ⁽¹⁾
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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NOTES

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Printed in The Netherlands

613514/03/pp12

Date of release: 2001 Feb 16

Document order number: 9397 750 08015

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